

THE NEXT GENERATION AMD ENTERPRISE SERVER PRODUCT ARCHITECTURE

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IMPROVING TCO FOR ENTERPRISE AND MEGA DATACENTER

Key Tenets of EPYC™ Processor Design

CPU Performance	<ul style="list-style-type: none">▪ “Zen” —high performance x86 core with Server features
Virtualization, RAS, and Security	<ul style="list-style-type: none">▪ ISA, Scale-out microarchitecture, RAS▪ Memory Encryption, no application mods: security you can use
Per-socket Capability	<ul style="list-style-type: none">▪ Maximize customer value of platform investment▪ MCM – allows silicon area > reticle area; enables feature set▪ MCM – full product stack w/single design, smaller die, better yield
Fabric Interconnect	<ul style="list-style-type: none">▪ Cache coherent, high bandwidth, low latency▪ Balanced bandwidth within socket, socket-to-socket
Memory	<ul style="list-style-type: none">▪ High memory bandwidth for throughput▪ 16 DIMM slots/socket for capacity
I/O	<ul style="list-style-type: none">▪ Disruptive 1 Processor (1P), 2P, Accelerator + Storage capability▪ Integrated Server Controller Hub (SCH)
Power	<ul style="list-style-type: none">▪ Performance or Power Determinism, Configurable TDP▪ Precision Boost, throughput workload power management

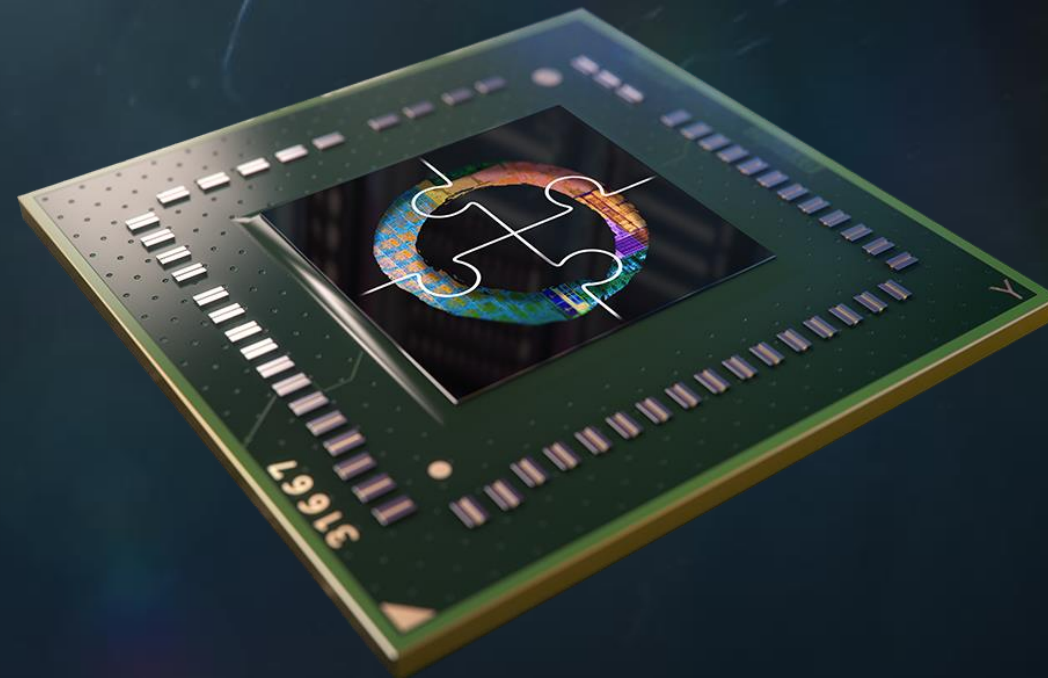
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“ZEN”

Designed from the ground up for optimal balance of performance and power for the datacenter



ZEN DELIVERS
GREATER THAN
(vs Prior AMD processors)

52% IPC*

Totally New
High-performance
Core Design

New High-Bandwidth,
Low Latency
Cache System

Simultaneous
Multithreading (SMT)
for High Throughput

Energy-efficient FinFET
Design for Enterprise-class
Products

Microarchitecture Overview in Hot Chips 2016

VIRTUALIZATION ISA AND MICROARCHITECTURE ENHANCEMENTS

ISA FEATURE	NOTES	“Bulldozer”	“Zen”
Data Poisoning	Better handling of memory errors		✓
AVIC	Advanced Virtual Interrupt Controller		✓
Nested Virtualization	Nested VMLOAD, VMSAVE, STGI, CLGI		✓
Secure Memory Encryption (SME)	Encrypted memory support		✓
Secure Encrypted Virtualization (SEV)	Encrypted guest support		✓
PTE Coalescing	Combines 4K page tables into 32K page size		✓

Microarchitecture Features

Reduction in World
Switch latency

Dual Translation
Table engines for
TLBs

Tightly coupled L2/L3
cache for scale-out
Private L2: 12 cycles
Shared L3: 35 cycles

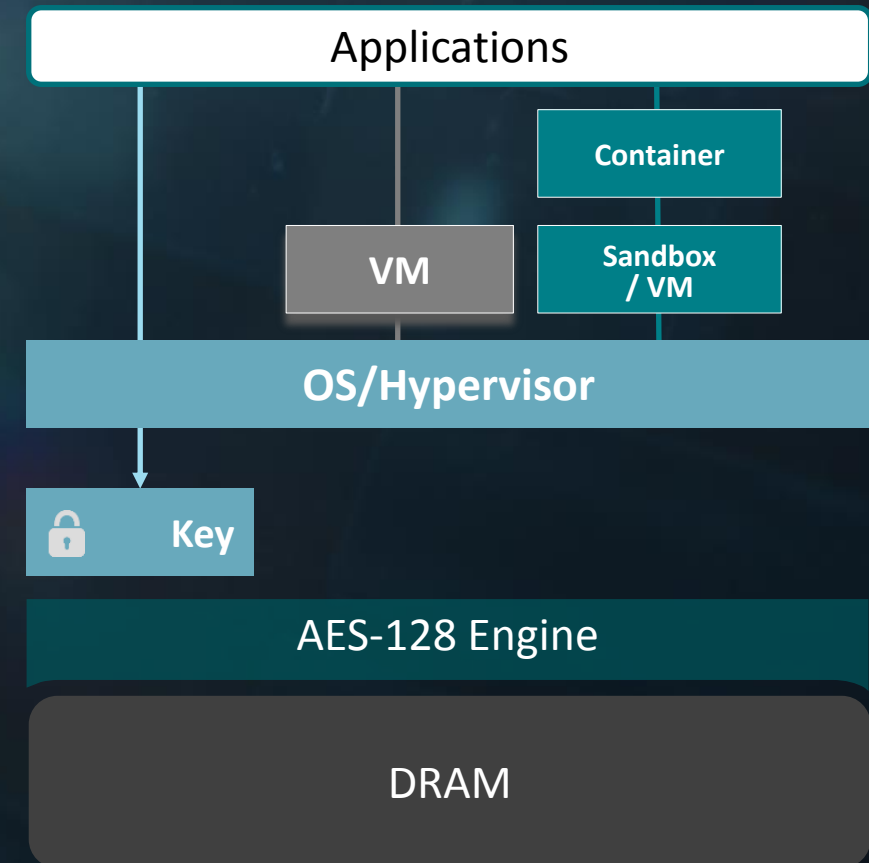
Cache + Memory
topology reporting
for Hypervisor/OS
scheduling

“Zen” Core built for the Data Center

HARDWARE MEMORY ENCRYPTION SECURE MEMORY ENCRYPTION (SME)

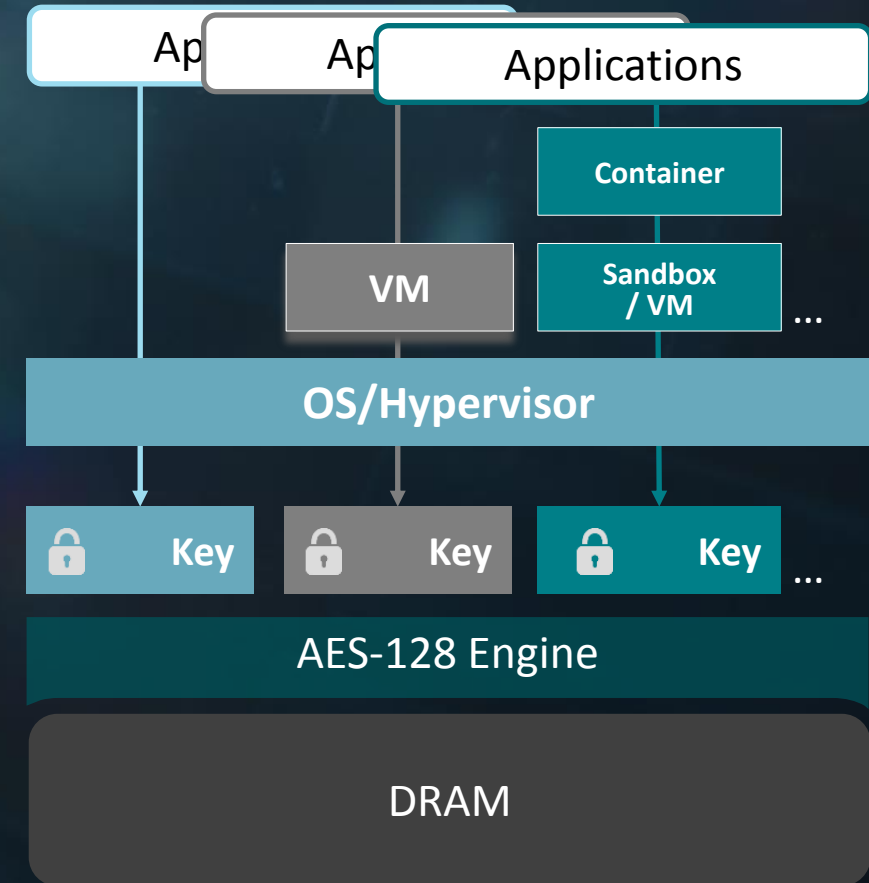
- Protects against physical memory attacks
- Single key is used for encryption of system memory
 - Can be used on systems with Virtual Machines (VMs) or Containers
- OS/Hypervisor chooses pages to encrypt via page tables or enabled transparently
- Support for hardware devices (network, storage, graphics cards) to access encrypted pages seamlessly through DMA
- No application modifications required

Defense Against Unauthorized
Access to Memory



HARDWARE MEMORY ENCRYPTION SECURE ENCRYPTED VIRTUALIZATION (SEV)

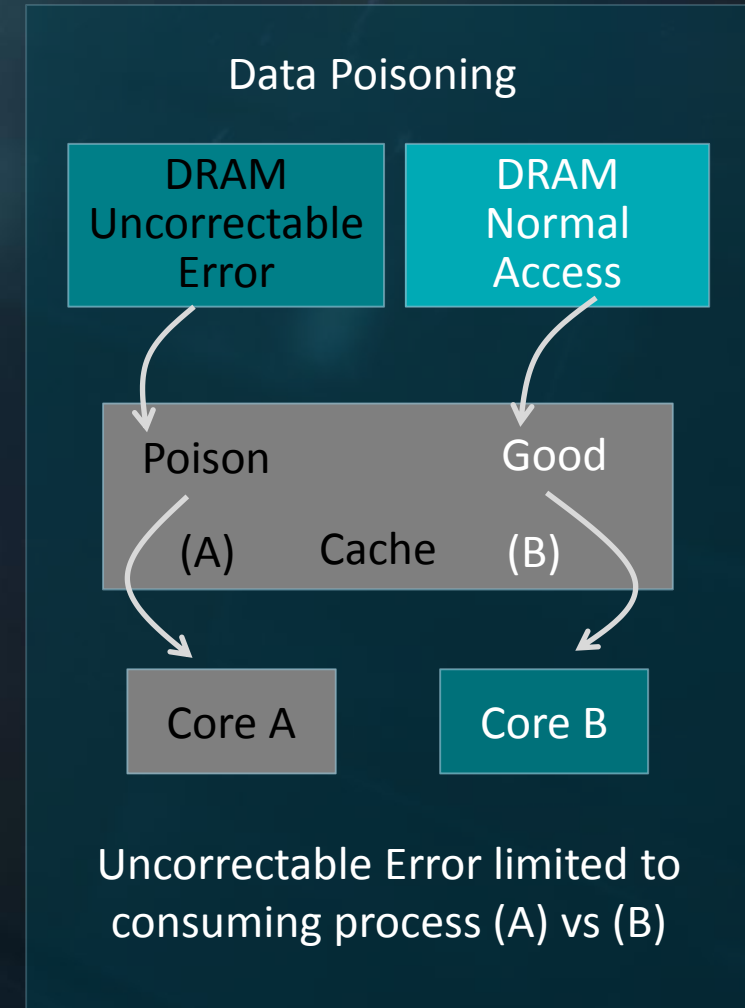
- Protects VMs/Containers from each other, administrator tampering, and untrusted Hypervisor
- One key for Hypervisor and one key per VM, groups of VMs, or VM/Sandbox with multiple containers
- Cryptographically isolates the hypervisor from the guest VMs
- Integrates with existing AMD-V technology
- System can also run unsecure VMs
- No application modifications required



BUILT FOR SERVER: RAS (RELIABILITY, AVAILABILITY, SERVICEABILITY)

- Caches
 - L1 data cache SEC-DED ECC
 - L2+L3 caches with DEC-TED ECC
- DRAM
 - DRAM ECC with x4 DRAM device failure correction
 - DRAM Address/Command parity, write CRC—with replay
 - Patrol and demand scrubbing
 - DDR4 post package repair
- Data Poisoning and Machine Check Recovery
- Platform First Error Handling
- Infinity Fabric link packet CRC with retry

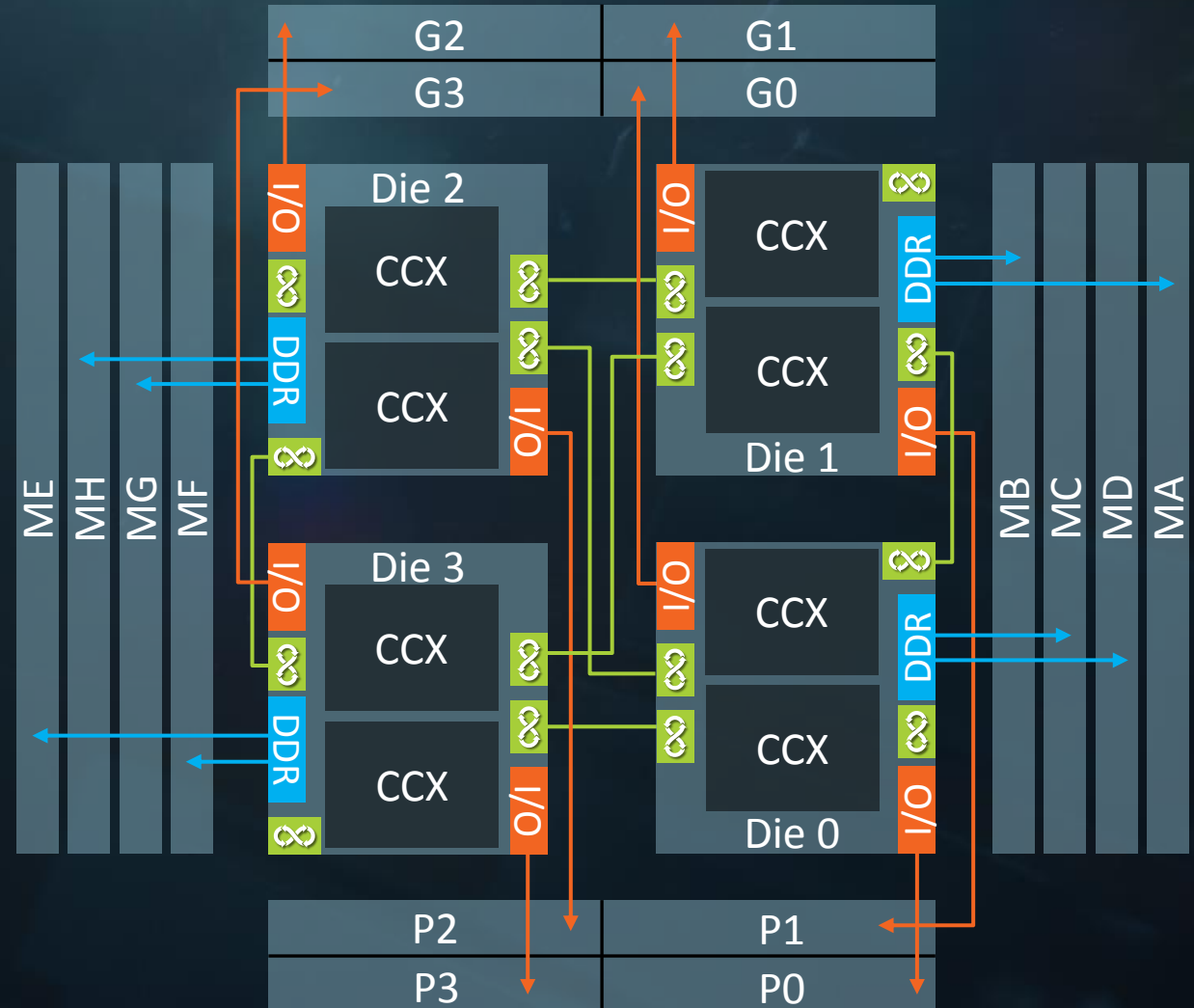
Enterprise RAS Feature Set



ADVANCED PACKAGING

- 58mm x 75mm organic package
- 4 die-to-die Infinity Fabric links/die
 - 3 connected/die
- 2 SERDES/die to pins
 - 1/die to “top” (G) and “bottom” (P) links
 - Balanced I/O for 1P, 2P systems
- 2 DRAM-channels/die to pins

Die-to-Package Topology Mapping



Purpose-built MCM Architecture

G[0-3], P[0-3] : 16 lane high-speed SERDES Links

M[A-H] : 8 x72b DRAM channels

∞ : Die-to-Die Infinity Fabric links

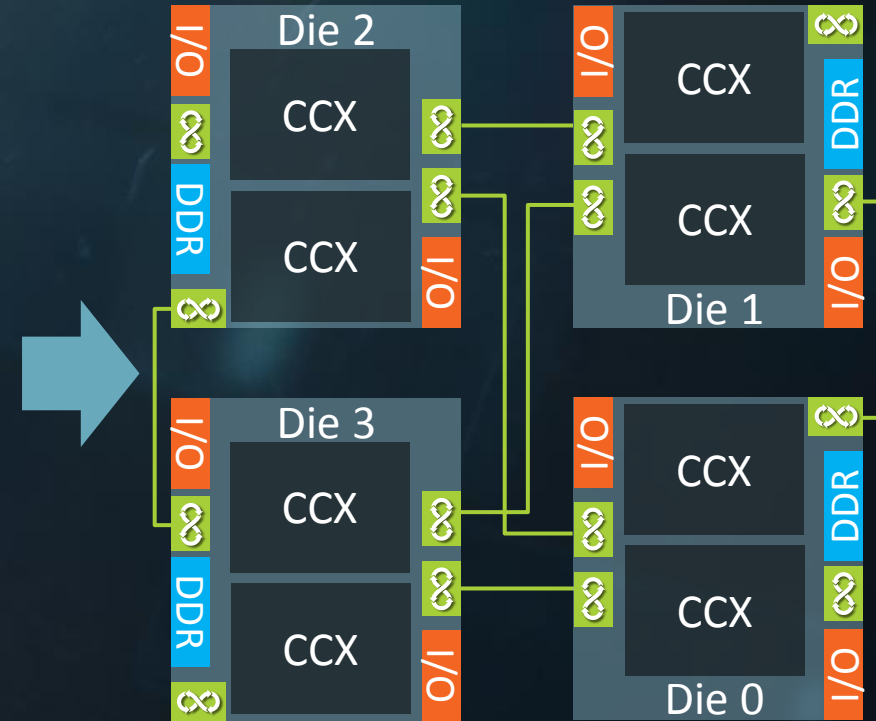
CCX: 4Core + L2/core + shared L3 complex

MCM VS. MONOLITHIC

- MCM approach has many advantages
 - Higher yield, enables increased feature-set
 - Multi-product leverage
- EPYC™ Processors
 - 4x 213mm² die/package = 852mm² Si/package*
- Hypothetical EPYC Monolithic
 - ~777mm²*
 - Remove die-to-die Infinity Fabric PHYs and logic (4/die), duplicated logic, etc.
 - 852mm² / 777mm² = ~10% MCM area overhead
- Inverse-exponential reduction in yield with die size
 - Multiple small dies has inherent yield advantage



32C Die Cost
1.0X

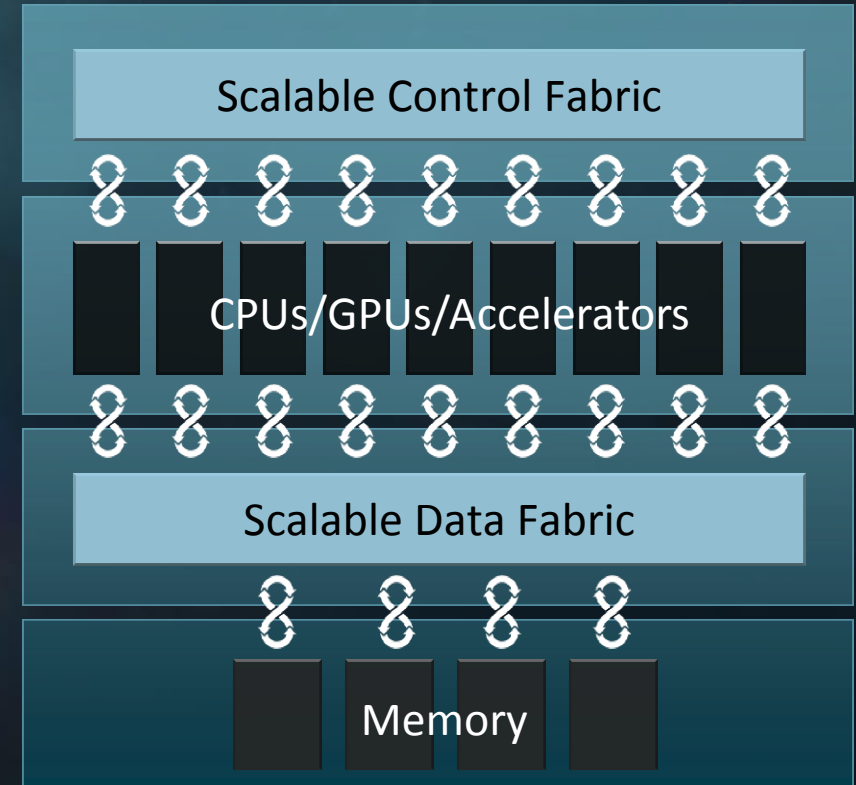


32C Die Cost
0.59X¹

MCM Delivers Higher Yields, Increases Peak Compute, Maximizes Platform Value

INFINITY FABRIC: ARCHITECTURE

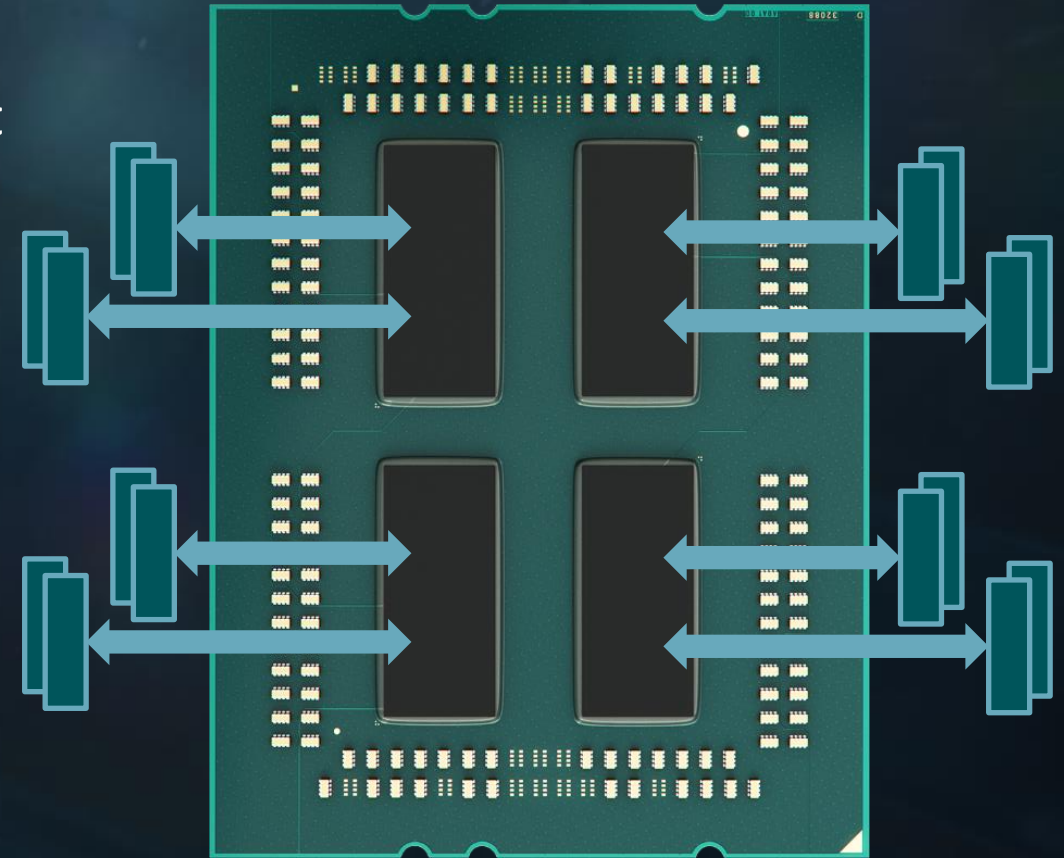
- Infinity Fabric
 - Data and Control plane connectivity within-die, between-die, between packages
 - Physical layer, protocol layer
- Revamped internal architecture for low latency, scalability, extensibility
 - Cross-product leverage for differentiated solutions
- 2 Planes
 - Scalable Control Fabric: SCF
 - Scalable Data Fabric: SDF
 - Strong data and control backbone for enhanced features



INFINITY FABRIC: MEMORY SYSTEM

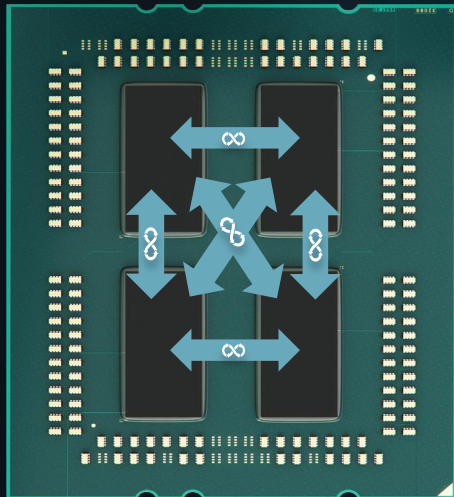
- 8 DDR4 channels per socket
- Up to 2 DIMMs per channel, 16 DIMMs per socket
- Up to 2667MT/s, 21.3GB/s, 171GB/s per socket
 - Achieves 145GB/s per socket, 85% efficiency*
- Up to 2TB capacity per socket (8Gb DRAMs)
- Supported memory
 - RDIMM
 - LRDIMM
 - 3DS DIMM
 - NVDIMM-N

Optimized Memory Bandwidth
and Capacity per Socket



INFINITY FABRIC: DIE-TO-DIE INTERCONNECT

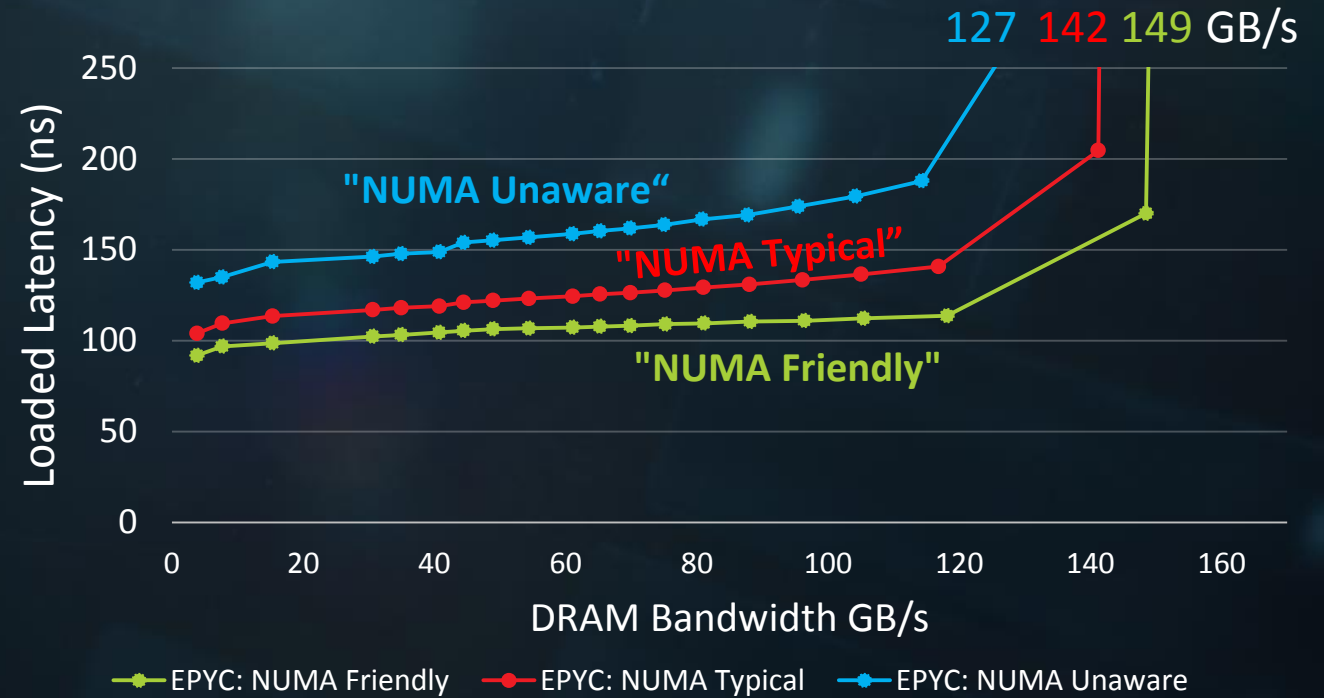
- Fully connected Coherent Infinity Fabric
- Optimized low power, low latency MCM links
- 42GB/sec bi-dir bandwidth per link, ~2pJ/bit TDP
- Single-ended, low power zero transmission
- Achieves 145GB/s DRAM bandwidth/socket STREAM TRIAD*
 - 171GB/s peak bisection BW; ~2x required
 - Overprovisioned for performance scaling



Latency of Isolated Request vs. System DRAM

Bandwidth, DRAM Page Miss*

1-Socket, RD-only Traffic, SMT Off, All cores active



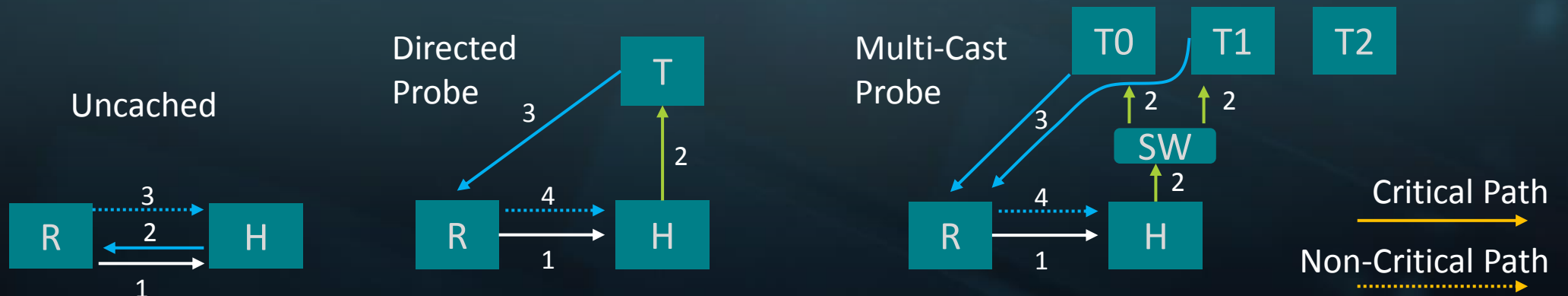
Purpose-built MCM Links, Over-provisioned Bandwidth

INFINITY DATA FABRIC: COHERENCE SUBSTRATE

- Enhanced Coherent HyperTransport
- 7-state coherence protocol: MDOEFSI
 - D: Dirty, migratory sharing optimization
- Probe Filter
 - SRAM-based for minimum indirection latency
 - No-probe, directed-probe, multi-cast probe, and broadcast probe flows
 - Probe response combining
- Coherence substrate key for performance scaling
 - Requester = Source CCX, Home = Coherence Controller (co-located with DRAM), Target = Caching CCX

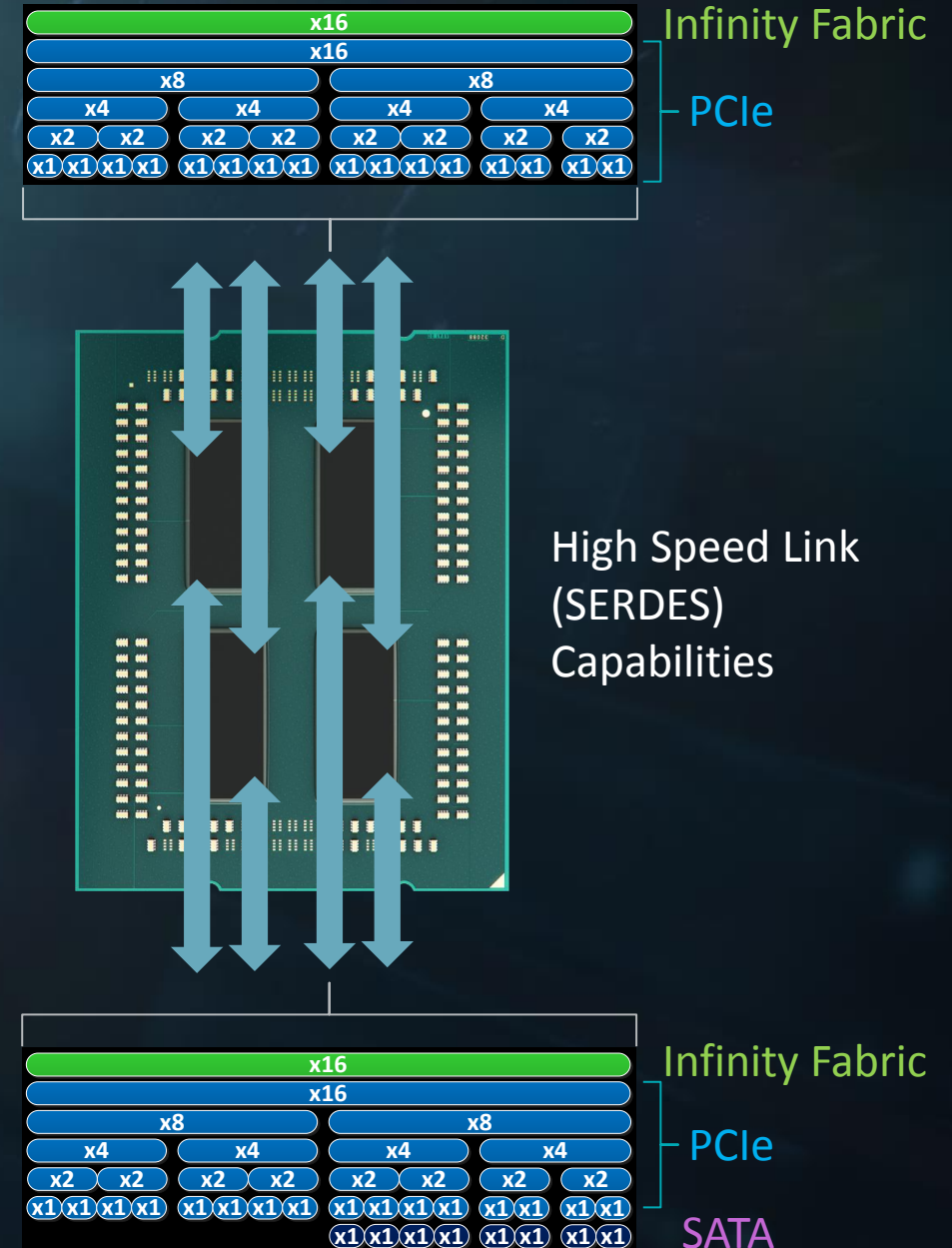
Request
Probe
Response
(R)equester
(H)ome
(T)arget
(SW) = Switch

Processor Cache Fill Request Flows



I/O SUBSYSTEM

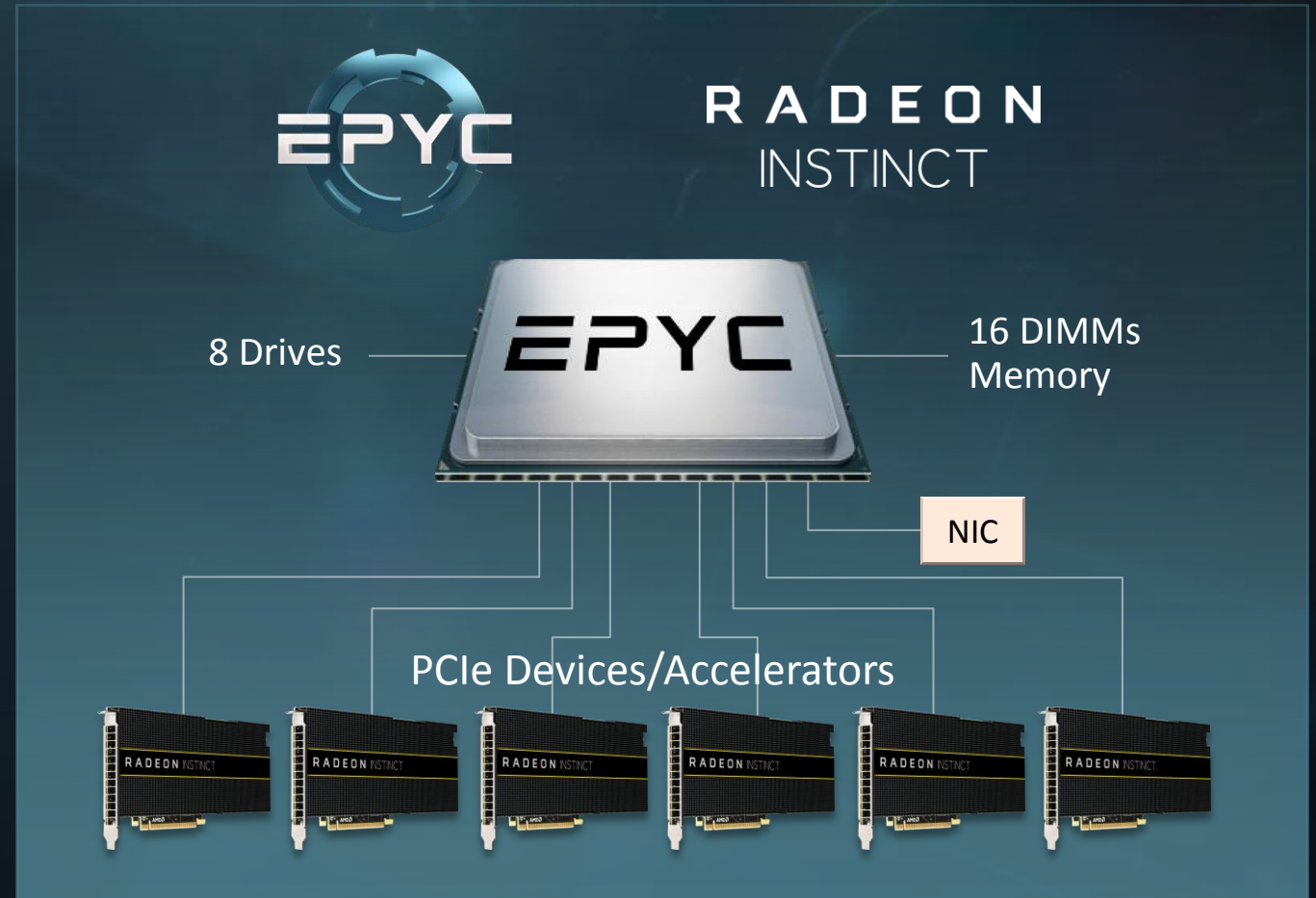
- 8 x16 links available in 1 and 2 socket systems
 - Link bifurcation support; max of 8 PCIe® devices per x16
 - Socket-to-Socket Infinity Fabric, PCIe, and SATA support
- 32GB/s bi-dir bandwidth per link, 256GB/s per socket
- PCIe Features*
 - Advanced Error Reporting (AER)
 - Enhanced Downstream Port Containment (eDPC)
 - Non-Transparent Bridging (NTB)
 - Separate RefClk with Independent Spread support (SRIS)
 - NVMe and Hot Plug support
 - Peer-to-peer support
- Integrated SATA support



Architected for Massive I/O Systems with
Leading-edge Feature Set, Platform Flexibility

EPYC™ — 1P I/O CAPABILITY

- 128 PCIe® links/processor
 - Removes PCIe switches
- All links can be used for I/O
 - Links are Infinity Fabric, PCIe, and SATA capable
- 4 I/O-hubs/processor
- PCIe peer-to-peer (P2P) support
- 8 DRAM channels + 16 DIMMs
- 32Cores/system for I/O and compute balance
 - Strong I/O connectivity and bandwidth with single high-performance CPU



Massive 1P I/O Connectivity for Accelerators or High-Speed Storage

EPYC™ — 1P I/O PERFORMANCE

- High bandwidth, high efficiency PCIe®
 - Local DMA, Peer-to-Peer (P2P)

	Achieved 1x16 PCIe Bandwidth* (Efficiency vs 16GB/s per direction)	Local DRAM (GBs / Efficiency ¹)	Die-to-Die Infinity Fabric (1-hop) (GBs / Efficiency ¹)
DMA	Read	12.2 / 76%	12.1 / 76%
	Write	13.0 / 81%	14.2 / 88%
	Read + Write	22.8 / 71%	22.6 / 70%
P2P	Write	NA	13.6 / 85%

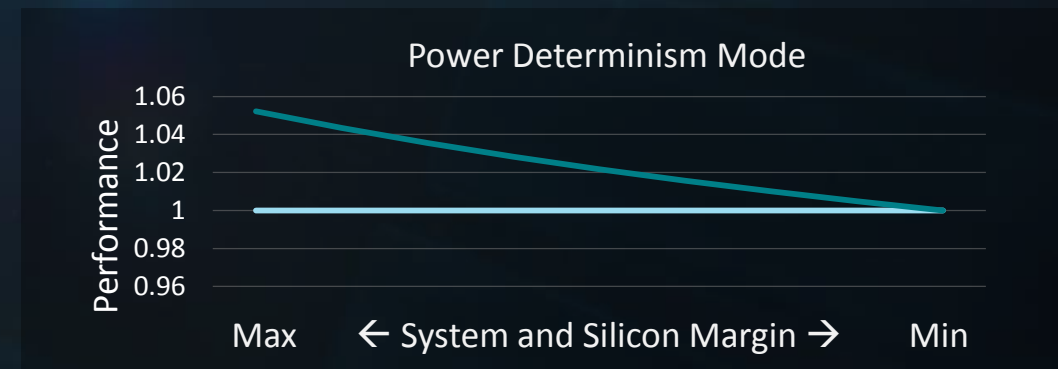
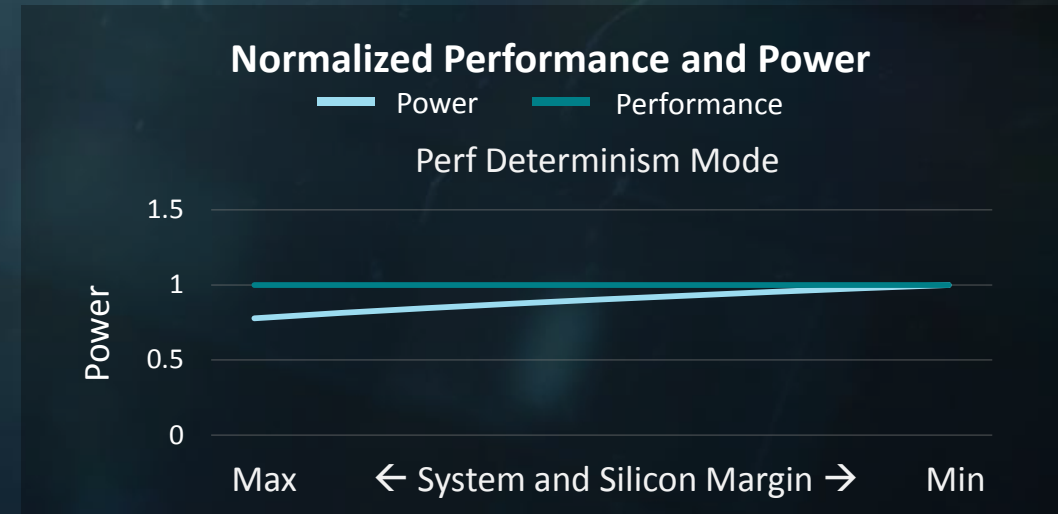
- High performance storage
 - ~285K IOPs/Core with 32 cores
 - 1P direct-connect 24 drives x4 (no PCIe switches)

EPYC™ 7601 1P
 16 x Samsung pm1725a NVMe, Ubuntu 17.04,
 FIO v2.16, 4KB 100% Read Results
9.2M IOPs*

High Performance I/O and Storage

POWER: PERFORMANCE-DETERMINISM, POWER-DETERMINISM, CONFIGURABLE TDP

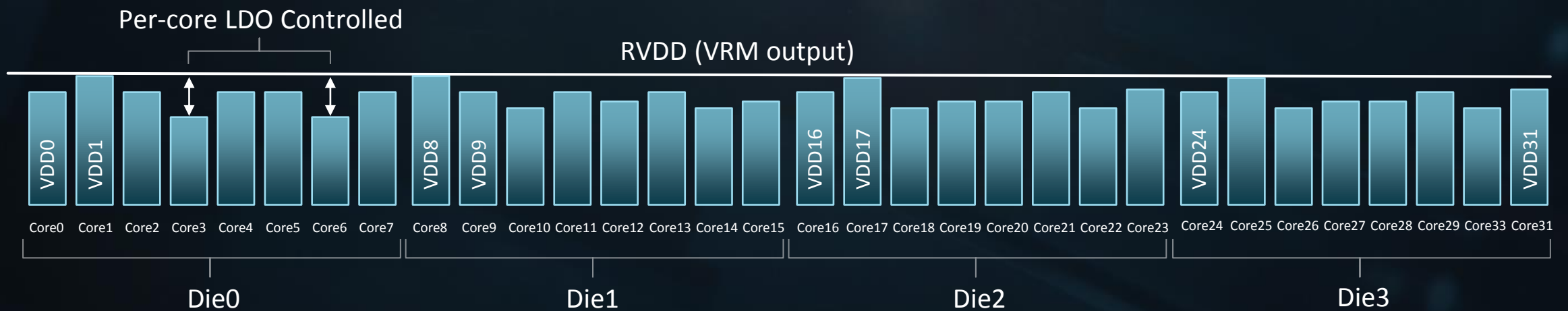
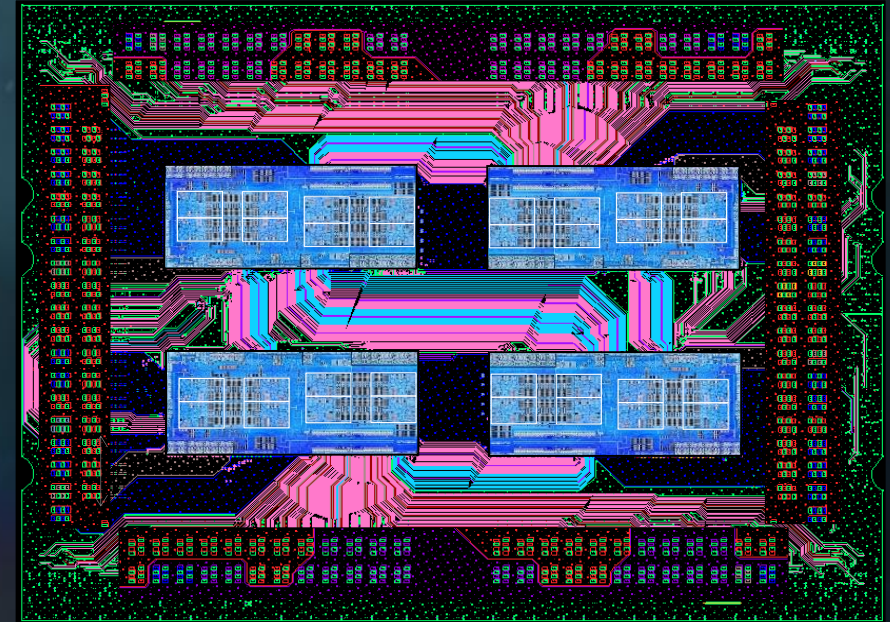
- Server systems and environments vary
- Silicon varies
 - Faster / higher leakage parts
 - Slower / lower leakage parts
- Some customers demand repeatable, deterministic performance for all environments
 - In this mode, power consumption will vary
- Others may want maximum performance with fixed power consumption
 - In this mode, performance will vary
- EPYC™ CPUs allow boot-time choice of either mode
- EPYC allows configurable TDP for TCO and peak performance vs performance/Watt optimization



Product TDP	Low range	High range
180W	165W	200W
155W	135W	170W
120W	105W	120W

PER-CORE LINEAR VOLTAGE REGULATION

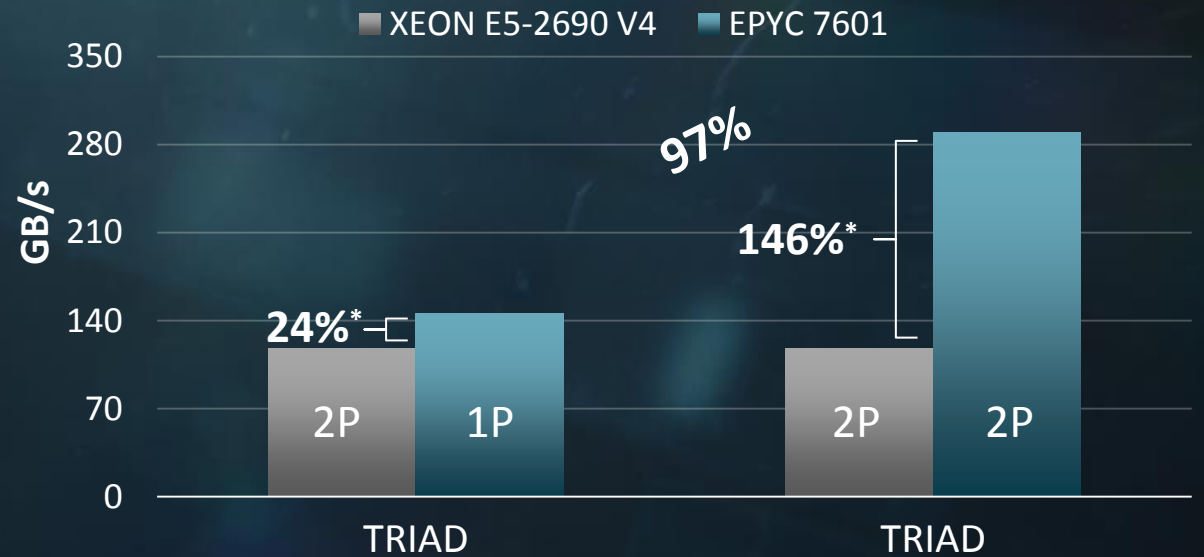
- Running all dies/cores at the voltage required by the slowest wastes power
- Per-core voltage regulator capabilities enable each core's voltage to be optimized
 - Significant core power savings and variation reduction



DELIVERED CPU PERFORMANCE

- Memory bandwidth and scaling
 - 97% Bandwidth scaling 1P->2P
 - Bandwidth for Disruptive 1P and 2P performance
- INT and FP performance
 - Memory bandwidth for demanding FP applications
 - Compiler-neutral 47% 2P Integer performance improvement

STREAM Memory Bandwidth (EPYC 7601 1P/2P vs E5-2690V4 2P)



EPYC™ Processors
 Deliver Compelling
 Performance
 and Memory
 Bandwidth

	Optimizing Compiler (See endnotes for calculations)	AMD EPYC 7601 64 CORES, 2.2 GHz, Open64	INTEL XEON E5-2699A V4 44 CORES, 2.4 GHz, ICC	EPYC Uplift
2P	SPECINT®_RATE2006	2360	1890	25%
	SPECFP®_RATE2006	1840	1160	59%
1P	SPECINT®_RATE2006	1200	909	32%
	SPECFP®_RATE2006	943	568	66%
Standard Compiler (GCC-O2)				
2P	SPECINT®_RATE2006	1390	943	47%

AMD EPYC™ 7000 SERIES PROCESSOR

Architected for Enterprise and
Datacenter Server TCO

Up to 32 High-Performance “Zen” Cores

8 DDR4 Channels per CPU

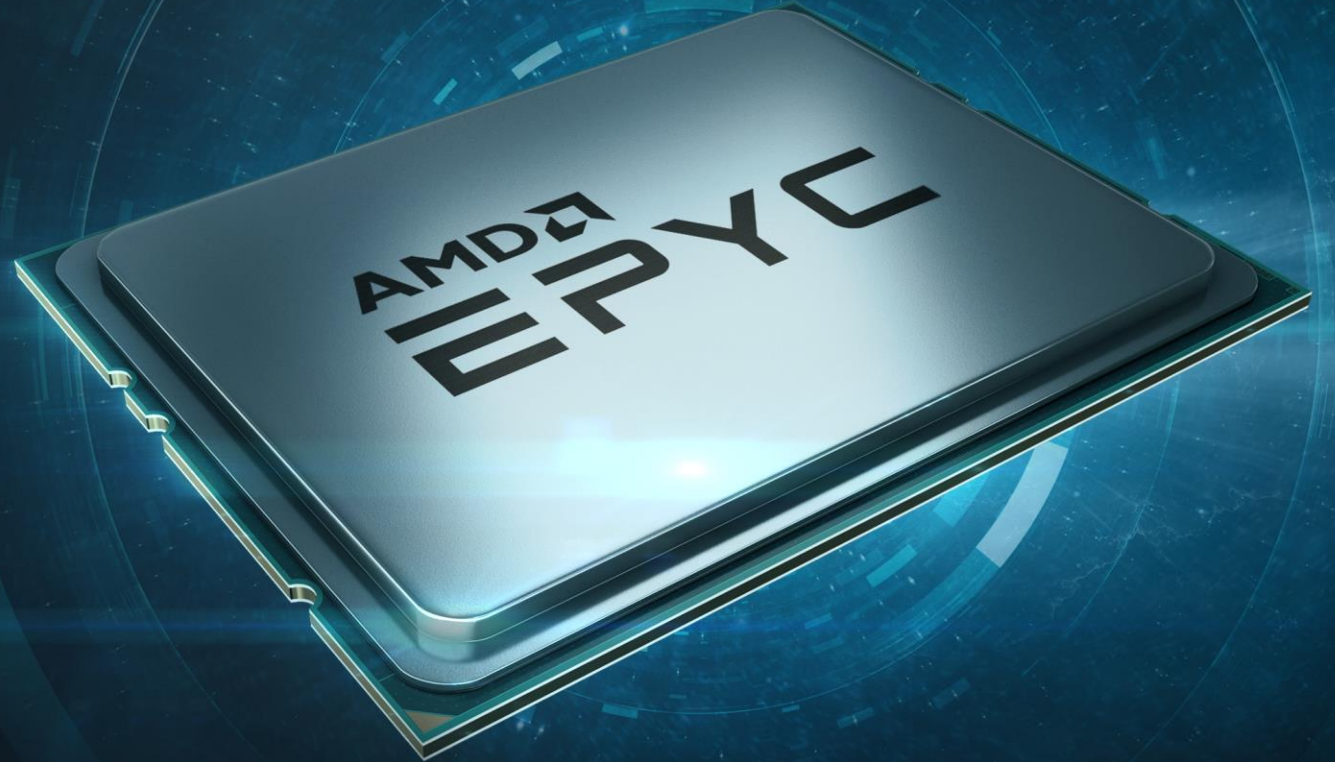
Up to 2TB Memory per CPU

128 PCIe® Lanes

Dedicated Security Subsystem

Integrated Chipset for 1-Chip Solution

Socket-Compatible with Next Gen EPYC
Processors



GLOSSARY OF TERMS

“Bulldozer” = AMD’s previous family of high performance CPU cores

CCX = Tightly Coupled Core + Cache Complex

4Core + L2 cache/core + Shared L3 cache complex

CLGI = Clear Global Interrupt

DIMM = Dual Inline Memory Module

ECC = Error Checking and Correcting

SEC-DED = Single Error Correct, Double Error Detect

DEC-TED = Double Error Correct, Triple Error Detect

GPU = Graphics Processing Unit

IPC = Instructions Per Clock

LDO = Low Drop Out, a linear voltage regulator

MCM = Multi-Chip Module

NUMA = Non-Uniform Memory Architecture

OS = Operating System

Post Package Repair = Utilize internal DRAM array redundancy to map out errant locations

PSP = Platform Security Processor

RAS = Reliability, Availability, Serviceability

SATA = Serial ATA device connection

SCH = Server Controller Hub

SCM = Single Chip Module

Scrubbing = Searching for, and proactively correcting, ECC errors

SERDES = Serializer/Deserializer

STGI = Set Global Interrupt

TCO = Total Cost of Ownership

TDP = Thermal Design Power

Topology Reporting = Describing cache and memory layout via ACPI/Software structures for OS/Hypervisor task scheduling optimization

VM = Virtual Machine

VRM = Voltage Regulator Module

World Switch = Switch between Guest Operating System and Hypervisor

ENDNOTES

SLIDE 5

Updated Feb 28, 2017: Generational IPC uplift for the “Zen” architecture vs. “Piledriver” architecture is +52% with an estimated SPECint_base2006 score compiled with GCC 4.6 -O2 at a fixed 3.4GHz. Generational IPC uplift for the “Zen” architecture vs. “Excavator” architecture is +64% as measured with Cinebench R15 1T, and also +64% with an estimated SPECint_base2006 score compiled with GCC 4.6 -O2, at a fixed 3.4GHz. System configs: AMD reference motherboard(s), AMD Radeon™ R9 290X GPU, 8GB DDR4-2667 (“Zen”)/8GB DDR3-2133 (“Excavator”)/8GB DDR3-1866 (“Piledriver”), Ubuntu Linux 16.x (SPECint_base2006 estimate) and Windows® 10 x64 RS1 (Cinebench R15). SPECint_base2006 estimates: “Zen” vs. “Piledriver” (31.5 vs. 20.7 | +52%), “Zen” vs. “Excavator” (31.5 vs. 19.2 | +64%). Cinebench R15 1t scores: “Zen” vs. “Piledriver” (139 vs. 79 both at 3.4G | +76%), “Zen” vs. “Excavator” (160 vs. 97.5 both at 4.0G | +64%). GD-108

SLIDE 11

Based on AMD internal yield model using historical defect density data for mature technologies.

SLIDE 13

In AMD internal testing on STREAM Triad, 2 x EPYC 7601 CPU in AMD “Ethanol” reference system, Ubuntu 16.04, Open64 v4.5.2.1 compiler suite, 512 GB (16 x 32GB 2Rx4 PC4-2666) memory, 1 x 500 GB SSD scored 290. NAP-22

SLIDE 14

In AMD internal testing on STREAM Triad, 2 x EPYC 7601 CPU in AMD “Ethanol” reference system, Ubuntu 16.04, Open64 v4.5.2.1 compiler suite, 512 GB (16 x 32GB 2Rx4 PC4-2666) memory, 1 x 500 GB SSD scored 290. NAP-22

SLIDE 14

AMD testing conducted by AMD Performance Labs on an AMD Grandstand reference platform configured with 2 x EPYC 7601 processors fixed at 2.2 GHz, 16 x 32GB DDR4 2666MHz DIMMs, Ethanol BIOS version “TSW1000C” and Ubuntu Server 16.04.2 LTS-kernel 4.10.0-22. Using AMD internal loaded latency test and estimations with 1 latency thread per die, and 7 load threads per die (1 thread per core). Loaded latencies are based on targeting all threads to their local memory access (NUMA Aware), all threads uniformly across remote memory accesses (NUMA Unware), or a weighted average of these latencies (Typical).

SLIDE 18

In AMD internal testing on IO Bandwidth benchmarks. 2x EPYC 7601 in AMD “Ethanol” reference systems, BIOS “TDL0080F” (default settings), Ubuntu 15.04.2, 512GB (16 x 32GB 2Rx4 PC4-2666) memory. Read and Write tests used AMD FirePro W7100 GPUs, 256B payload size, Driver “amdgpu-pro version 17.10-450821”. Read + Write tests used Mellanox IB 100Gbps Adapter, 512B payload size, Driver “OFED 3.3-1.04”. Read and Write DMA tests performance using AMD SST (System Stress Tool). Write peer-to-peer (P2P) tests performance using AMD P2P (Peer to Peer) tool. Read + Write DMA tests performance using OFED qperf tool.

1 x EPYC 7601 CPU in HPE Cloudline CL3150, Ubuntu 17.04 4.10 kernel (Scheduler changed to NOOP, CPU governor set to performance), 256 GB (8 x 32GB 2Rx4 PC4-2666) memory, 24 x Samsung pm1725a NVMe drives (with only 16 enabled): FIO v2.16 (4 Jobs per drive, IO Depth of 32, 4K block size) Average Read IOPs 9,178,000 on 100% Read Test (Average BW 35.85 GB/s); FIO (4 jobs per drive, IO depth of 10, 4K block size) Average Write IOPs 7,111,000 on 100% Write Test (Average BW 27.78 GB/s Each run was done for 30 seconds with a 10 second ramp up using 16 NVMe drives. NAP-24

ENDNOTES

SLIDE 21

AMD EPYC™ 7601 CPU-based 2-socket system delivers up to 47% higher performance-for up to 14% less power as Intel Xeon E5-2699A v4-based 2-socket system using estimated SPECint®_rate_base2006 results AMD EPYC 7601-based 2-socket system scored 1390 (measured wall power 1479Whr over 3.39 hrs), and Intel E5-2699A v4-based 2-socket system scored 943 (measured wall power 1687Whr over 3.73 hrs), using estimated scores based on internal AMD testing as of 6 June 2017. 2 x EPYC 7601 CPU in Supermicro AS-1123US-TR4, Ubuntu 16.04, GCC-02 v6.3 compiler suite, 512 GB (16 x 32GB 2Rx4 PC4-2666 running at 2400) memory, 1 x 500 GB SSD; versus 2 x E5-2699A v4 CPU in Intel Server System R1208WT2GSR, Ubuntu 16.04, GCC-02 v6.3 compiler suite, 512 GB (16 x 32GB 2Rx4 PC4-2666 running at 2133) memory, 1 x 500 GB SSD. SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. See www.spec.org. NAP-06

1-socket AMD EPYC 7601 delivers up to 24% more bandwidth than a 2P Intel E5-2690 v4 In AMD internal testing on STREAM Triad, 1 x EPYC 7601 CPU in AMD “Ethanol” reference system, Ubuntu 16.04, Open64 v4.5.2.1 compiler suite, 256 GB (8 x 32GB 2Rx4 PC4-2666) memory, 1 x 500 GB SSD scored 147; versus 2 x E5-2690 v4 CPU in Intel Server System R1208WT2GSR, Ubuntu 16.04, GCC-02 v6.3 compiler, 256 GB (8 x 32GB 2Rx4 PC4-2666 running at 2400) memory, 1 x 500 GB SSD scored 118. NAP-21

2-socket AMD EPYC 7601 delivers up to 146% more memory bandwidth than 2-socket Intel E5-2690 v4 In AMD internal testing on STREAM Triad, 2 x EPYC 7601 CPU in AMD “Ethanol” reference system, Ubuntu 16.04, Open64 v4.5.2.1 compiler suite, 512 GB (16 x 32GB 2Rx4 PC4-2666) memory, 1 x 500 GB SSD scored 290; versus 2 x E5-2690 v4 CPU in Intel Server System R1208WT2GSR, Ubuntu 16.04, GCC-02 v6.3 compiler, 256 GB (8 x 32GB 2Rx4 PC4-2666 running at 2400) memory, 1 x 500 GB SSD scored 118. NAP-22

AMD EPYC™ 7601 CPU-based system scores up to 25% higher than Intel Xeon E5-2699A v4-based system on SPECint®_rate2006 AMD EPYC 7601-based system scored 2360 in AMD internal testing, and Intel E5-2699A v4-based system scored 1890 based on www.spec.com as of 29 May 2017. 2 x EPYC 7601 CPU in Supermicro AS-1123US-TR4, Ubuntu 16.04, x86 Open64 v4.5.2.1 Compiler Suite, 512 GB (16 x 32GB 2Rx4 PC4-2666) memory, 1 x 500 GB SSD; versus 2 x E5-2699A v4 CPU in Huawei RH2288H V3, Red Hat Enterprise Linux Server release 7.2, ICC v16.0.0.101 compiler suite, 512 GB (16 x 32GB 2Rx4 PC4-2400T-R) memory, 1 x 1000 GB SATA, 7200. SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. See www.spec.org. NAP-13

AMD EPYC™ 7601 CPU-based system scores up to 59% higher than Intel Xeon E5-2699A v4-based system on SPECfp®_rate2006 AMD EPYC 7601-based system scored 1840 in AMD internal testing, and Intel E5-2699A v4-based system scored 1160 based on www.spec.com as of 29 May 2017. 2 x EPYC 7601 CPU in, Supermicro AS-1123US-TR4, Ubuntu 16.04, x86 Open64 v4.5.2.1 Compiler Suite, 512 GB (16 x 32 GB 2Rx4 PC4-2666) memory, 1 x 500 GB SSD; versus 2 x E5-2699A v4 CPU in, Lenovo System x3650 M5, SUSE Linux Enterprise Server 12, ICC v17.0.0.098 compiler suite, 256 GB (16 x 16 GB 2Rx4 PC4-2400T-R), 1 x 800 GB SATA SSD. SPEC and SPECfp are registered trademarks of the Standard Performance Evaluation Corporation. See www.spec.org. NAP-14

ENDNOTES

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AMD EPYC 7601-based 1-socket system scored 1200 on SPECint_rate2006, higher than any other traditional 1-socket x86-based system score published at www.spec.org as of 29 May 2017. In AMD internal testing, 1 x EPYC 7601 CPU in HPE Cloudline CL3150, Ubuntu 16.04, x86 Open64 v4.5.2.1 Compiler Suite, 256 GB (8 x 32GB 2Rx4 PC4-2666) memory, 1 x 500 GB SSD scored 1200 on SPECint_rate2006; versus E5-2699 v4-based SuperMicro Storage Server score of 909 published May 2016 at www.spec.org. Record comparison excludes Intel Xeon Phi accelerators. SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. See www.spec.org for more information. NAP-09

AMD EPYC™ 7601 CPU-based 2-socket system delivers up to 47% higher performance-for up to 14% less power as Intel Xeon E5-2699A v4-based 2-socket system using estimated SPECint®_rate_base2006 results AMD EPYC 7601-based 2-socket system scored 1390 (measured wall power 1479Whr over 3.39 hrs), and Intel E5-2699A v4-based 2-socket system scored 943 (measured wall power 1687Whr over 3.73 hrs), using estimated scores based on internal AMD testing as of 6 June 2017. 2 x EPYC 7601 CPU in Supermicro AS-1123US-TR4, Ubuntu 16.04, GCC-02 v6.3 compiler suite, 512 GB (16 x 32GB 2Rx4 PC4-2666 running at 2400) memory, 1 x 500 GB SSD; versus 2 x E5-2699A v4 CPU in Intel Server System R1208WT2GSR, Ubuntu 16.04, GCC-02 v6.3 compiler suite, 512 GB (16 x 32GB 2Rx4 PC4-2666 running at 2133) memory, 1 x 500 GB SSD. SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. See www.spec.org. NAP-06

AMD EPYC 7601-based 1-socket system scored 943 on SPECfp_rate2006, higher than any other 1-socket system score published at www.spec.org as of 29 May 2017. In AMD internal testing, 1 x EPYC 7601 CPU in HPE Cloudline CL3150, Ubuntu 16.04, x86 Open64 v4.5.2.1 Compiler Suite, 256 GB (8 x 32GB 2Rx4 PC4-2666) memory, 1 x 500 GB SSD scored 943 on SPECfp_rate2006; versus E5-2699 v4-based HPE ProLiant ML350 score of 568 published May 2016 at www.spec.org. SPEC and SPECfp are registered trademarks of the Standard Performance Evaluation Corporation. See www.spec.org for more information. NAP-10