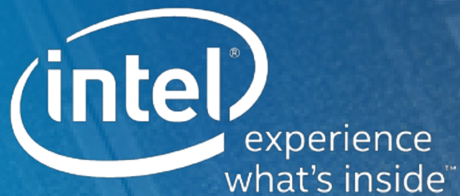
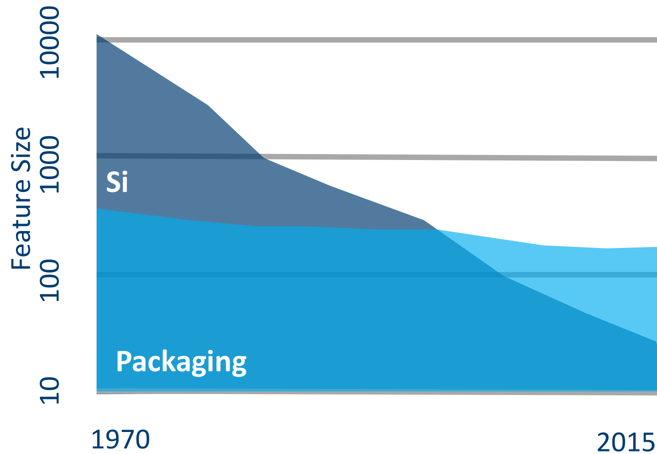


Heterogeneous Modular Platform

Sergey Shumarayev

CTO Office, Programmable Solution Group, Intel® Corporation

Motivations



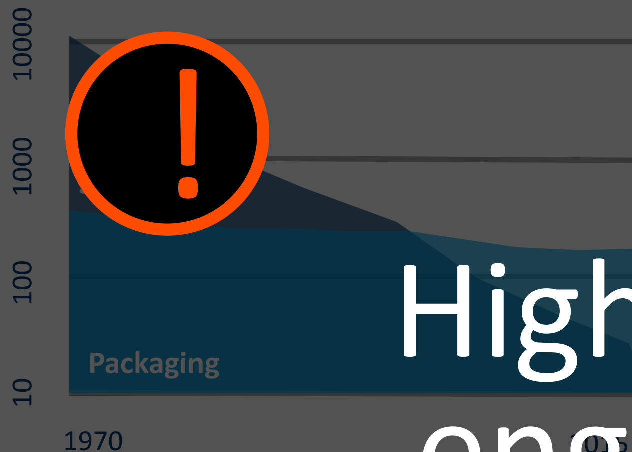
Disparity between silicon and package/board technologies

- Drove SERDES needs to connect the dies
- Increase in serialization requirements
- SERDES up to ~30% area and ~30% power in high end system

Manufacturing cost increase and yields decrease with significant non-reparable die size for analog

- Increased complexity, system latency, and power
- Long coupled development cycles for analog + digital on same monolithic die

Motivations



Disparity between silicon and package/board technologies

- Drove SERDES needs to connect the dies
- Increase in serialization requirements
- SERDES takes ~30% and ~30% power in high end system

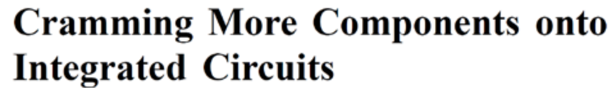
Manufacturing increase and yields decrease with significant non-reparable die size for analog

High non-recurring engineering (NRE) and longer Time To Market (TTM)

! Increased complexity, system latency and power

! Long coupled development cycles for analog + digital on same monolithic die

High Density Packaging Technology Enables Heterogeneous Integration

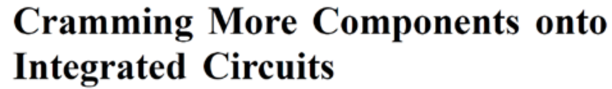

Cramming More Components onto Integrated Circuits

GORDON E. MOORE, LIFE FELLOW, IEEE

VIII. Day of Reckoning

Clearly, we will be able to build such component crammed equipment. Next, we ask under what circumstances we should do it. The total cost of making a particular system function must be minimized. To do so, we could amortize the engineering over several identical items, or evolve flexible techniques for the engineering of large functions so that no disproportionate expense need be borne by a particular array…

…It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.


Cramming More Components onto Integrated Circuits

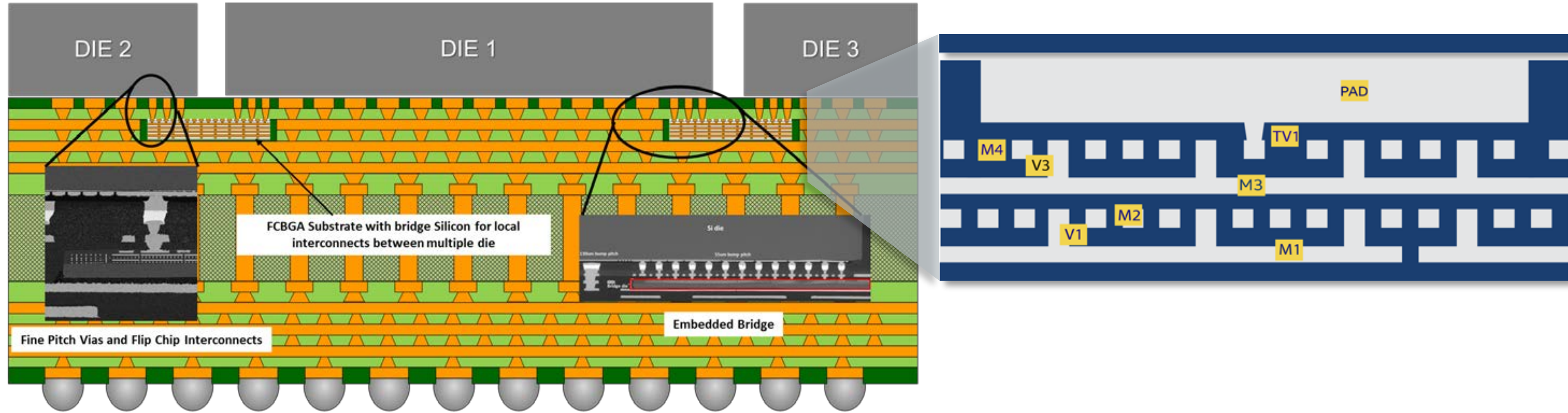
GORDON E. MOORE, LIFE FELLOW, IEEE

…It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.

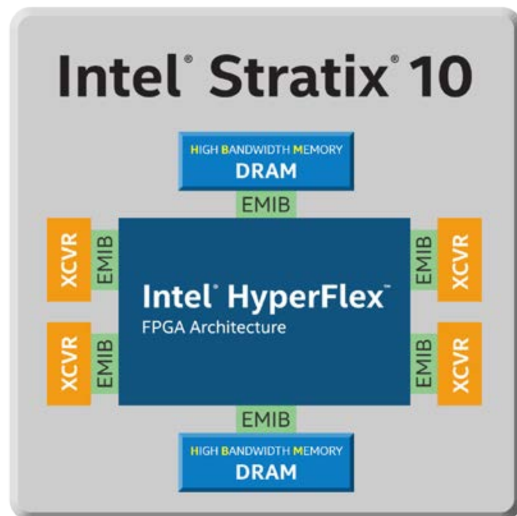
Heterogeneous is part of Moore’s law

More of Moore

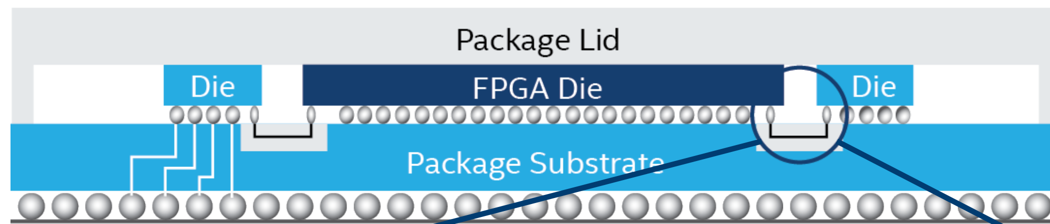
Intel® Embedded Multi-Die Interconnect Bridge (EMIB) Technology

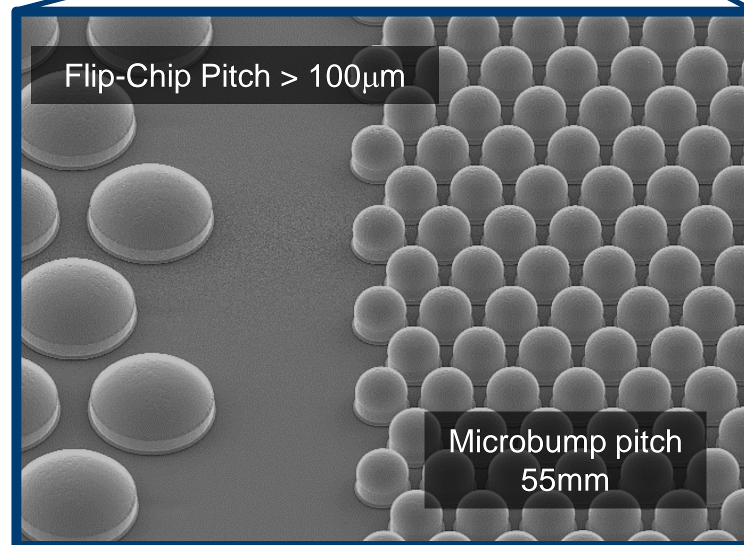


Intel® Embedded Multi-Die Interconnect Bridge (EMIB) Technology

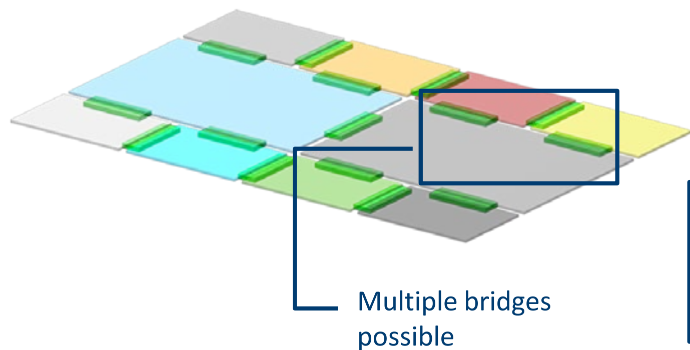


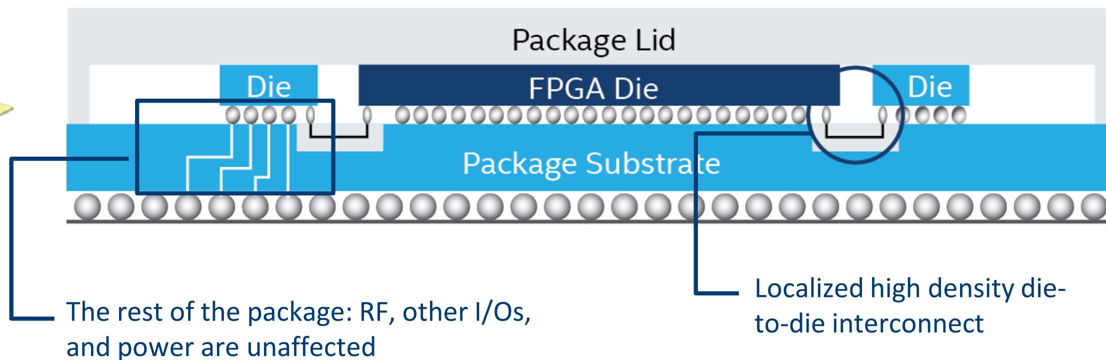
Intel® Stratix® 10 FPGAs and SoCs with Intel EMIB





High Density Package Technology Offerings

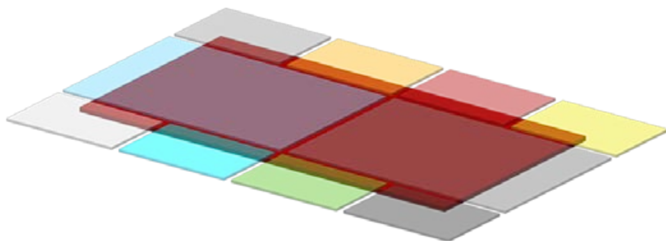


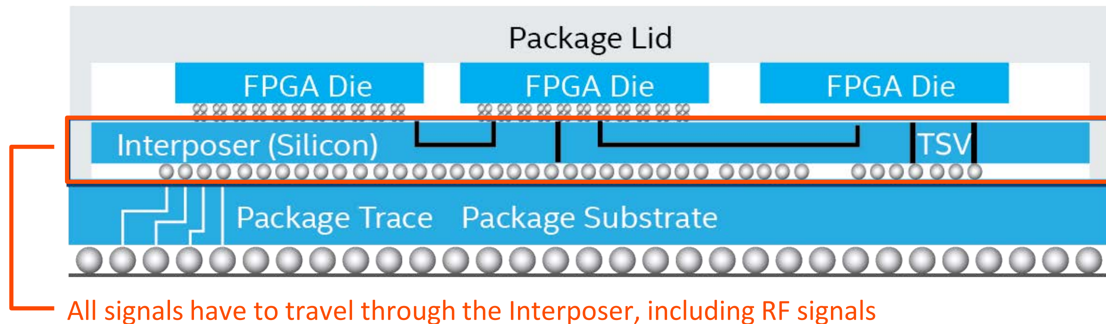


Multiple bridges possible

The rest of the package: RF, other I/Os, and power are unaffected

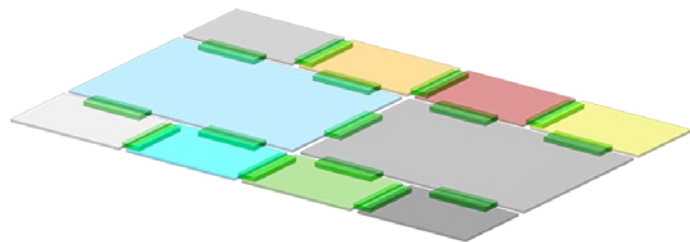
Localized high density die-to-die interconnect

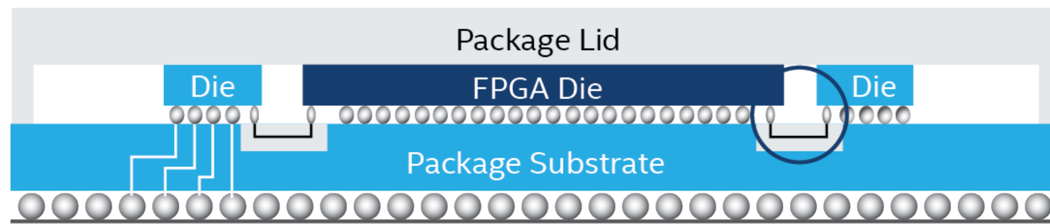




All signals have to travel through the Interposer, including RF signals

Intel® Embedded Multi-Die Interconnect Bridge (EMIB) Technology



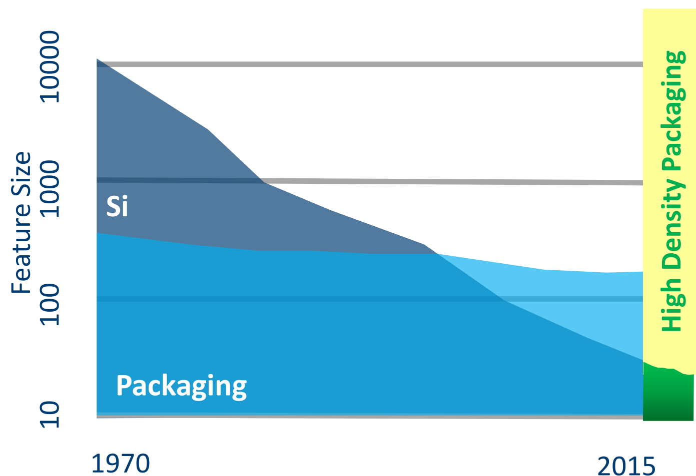


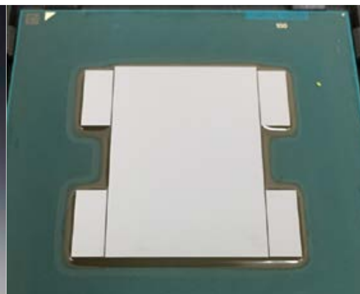
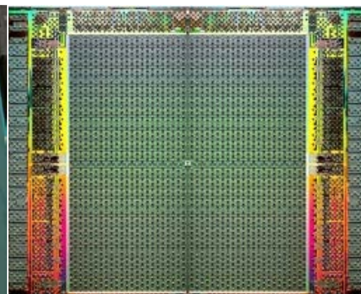
Reduced Fabrication and Assembly

Cost Effective, High Performance Solution

No Reticle Size Limitations

Optimized Interface PPA



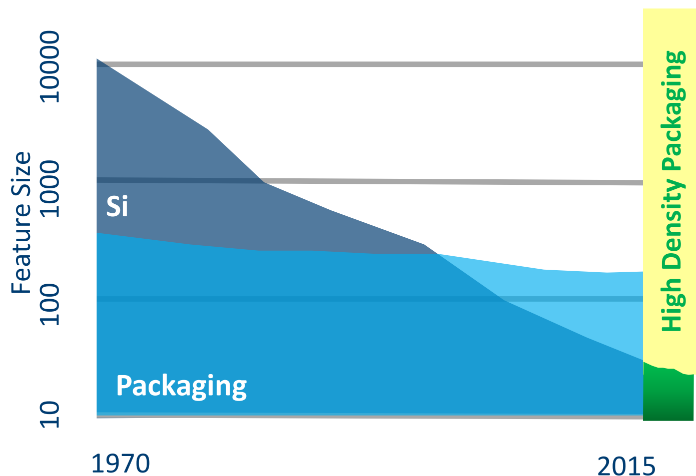



	On-Board	On-Package	On-Die
Distance	meter	~1mm	~0.1mm
Power (pJ/b)	20	<1	0.1
Standard	PCI-E, DDR, …	UIB, *AIB*	IOSF, AMBA, …

20x Decrease
Interface Power

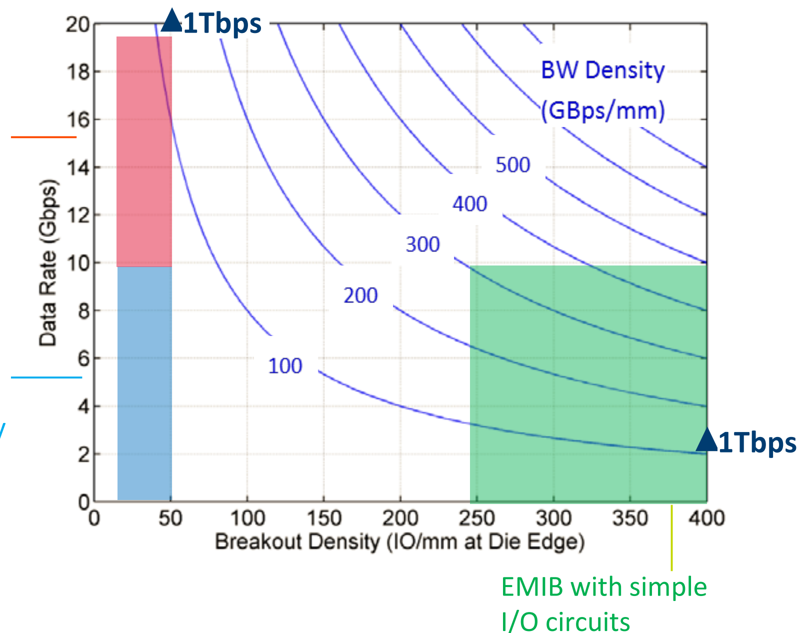
~OR~ ≈ Near Monolithic Capability

Choosing Die to Die Signaling



More and more complicated I/O circuits

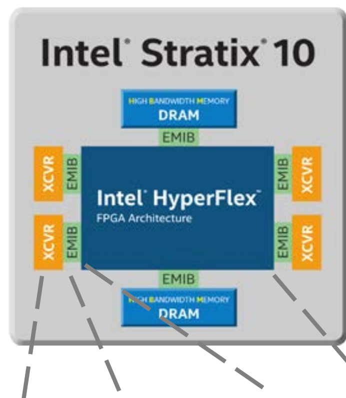
Organic substrate with very low bandwidth density



- ✓ Disparity Gap is addressed by High Density Packaging

- ✓ EMIB with Simple parallel IO circuitry is preferred over serial signaling:
- ✓ power↓ + latency↓ + scalability↑

Intel® Stratix® A New Class of Product = Platform

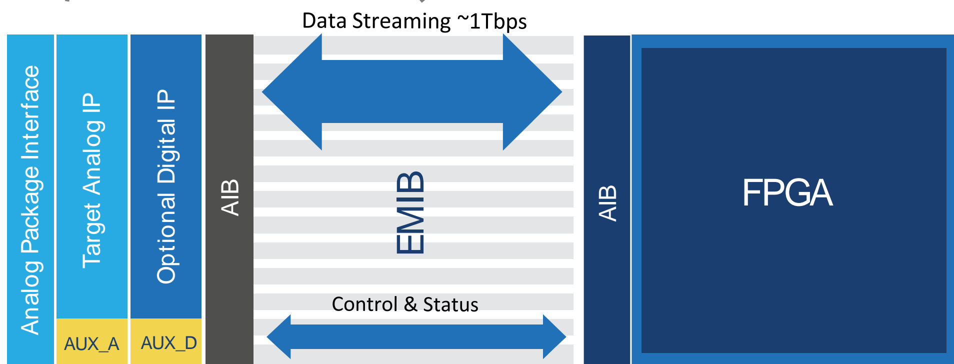


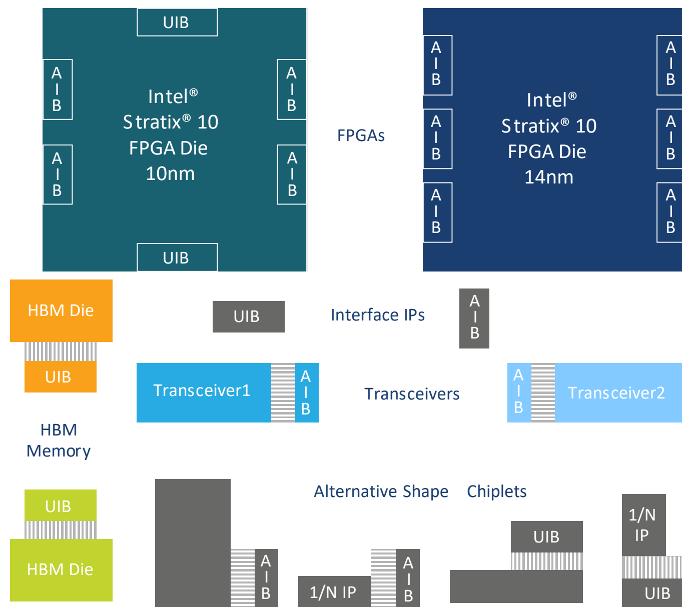
Mixes process nodes and system functions into a single device

Superior noise isolation for analog vs. monolithic

FPGA + transceivers (XCVRs) + High-Bandwidth Memory (HBM)

= 3 foundries on 6 technology nodes





Decouples ASIC / FPGA / Analog/RF design cycles

Chiplets, Platforms, and SiP?

A chiplet is a functional, verified, re-usable physical IP block

- Realized in physical form, i.e. in effect a building block

  (e.g. processor, converters, memory, waveform generators, filters, etc.)

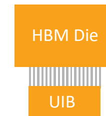
High performance (based on 2.5D/3D) system in package (SiP) :

- Created through integration of chiplets vs. monolithically
- Platform provides framework governing composition rules

Intel® PSG SiP Interface Options: AIB and UIB

Two types of interfaces for two types of applications use cases

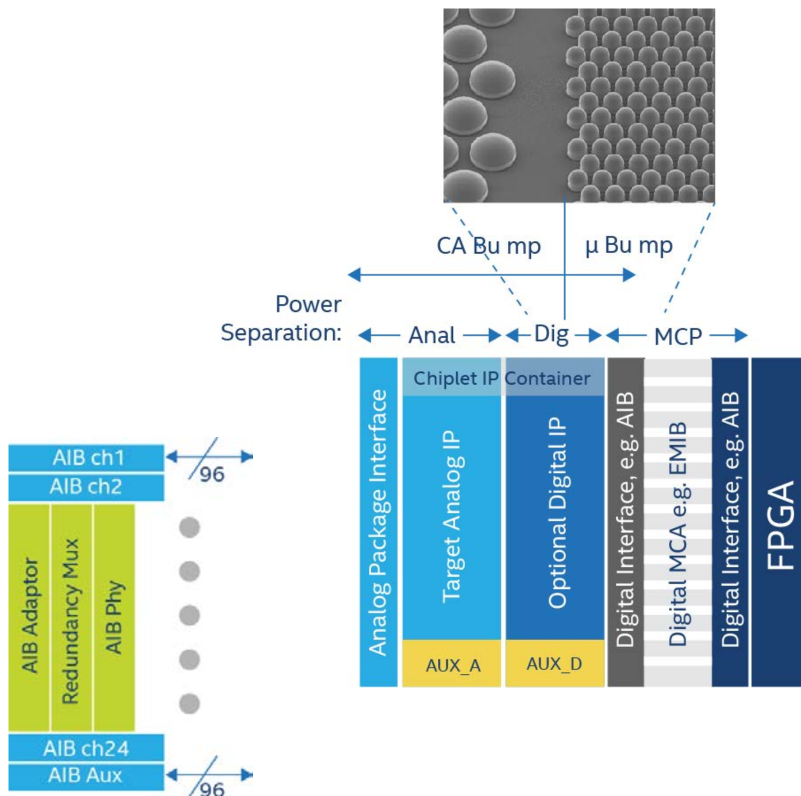
UIB general purpose SiP interface for HBM and ASIC



AIB was created for TRCVer and generalized to other use cases, e.g. analog, RF

Programmable Data Rate of up to 2Gbps per physical line

Intel® PSG AIB Architecture Overview



Power separation for improved flexibility and PI

The AIB is subdivided into 25 logical channels:

- 24 are user channels + aux to handshake

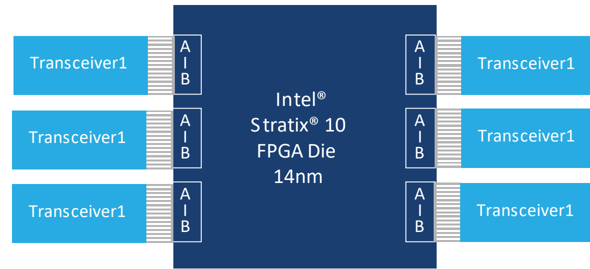
Adaptor for light weight data streaming

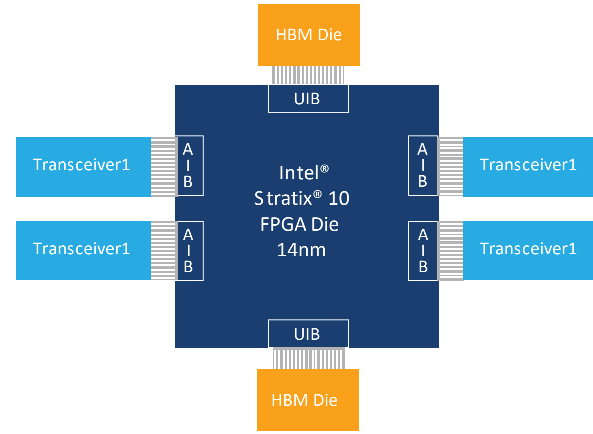
- Abstract Phy details from target IP provider

AIB Phy redundancy steering:

- Invisible to IP designer

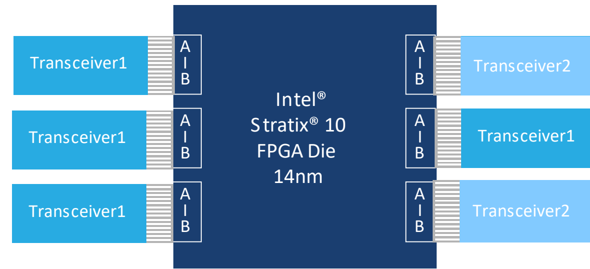
Modular Platform Enables Heterogeneous Systems

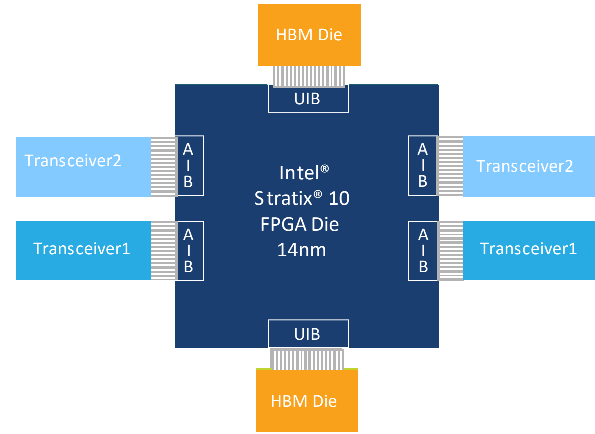




- Decouples ASIC / FPGA / Analog design cycles
- Improved TTM
- Reduced deployment and development cost

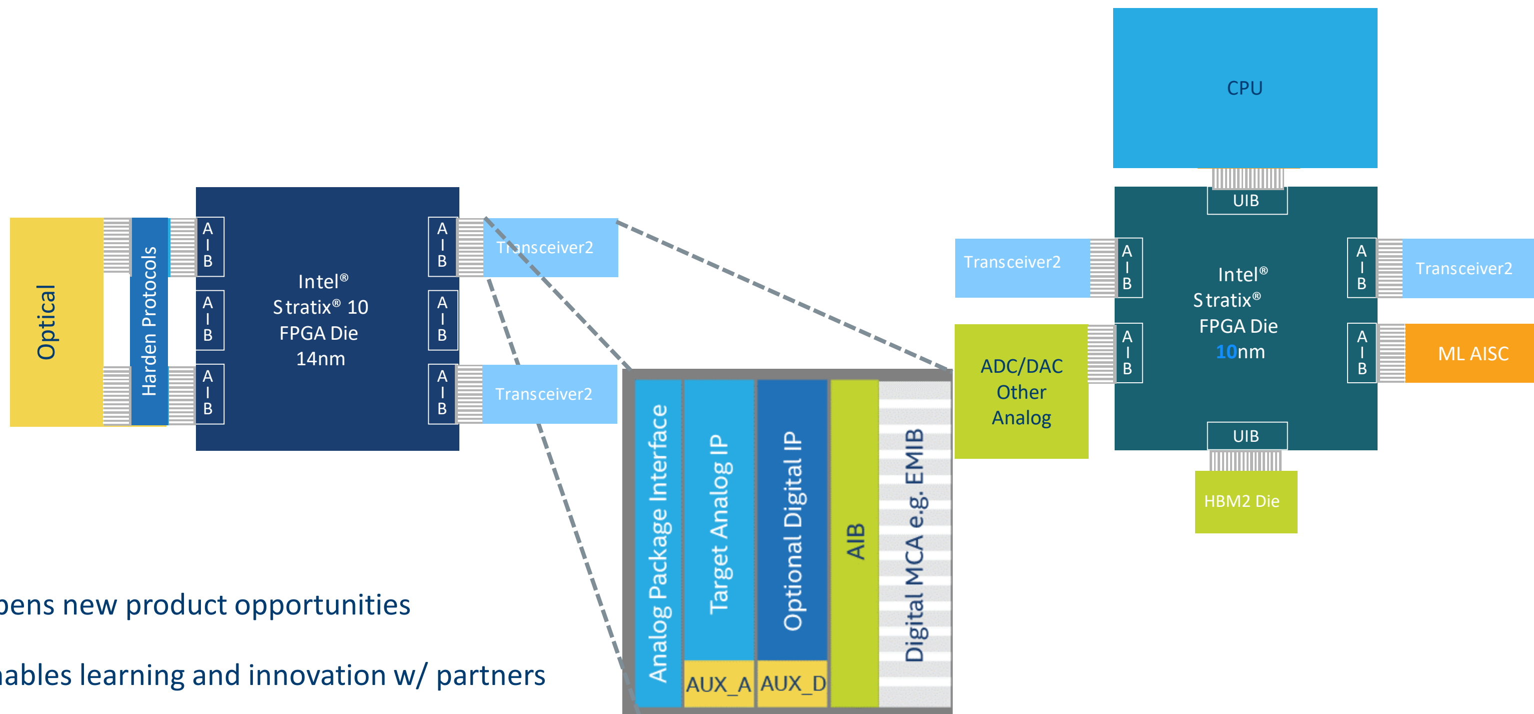
Modular Platform Enables Cost-Effective Upgrades





- Facilitate revolutionary capability for best-of-breed technology selection
- Expedited time to market
- AIB & UIB provides flexible HBM and TRCVers attachment

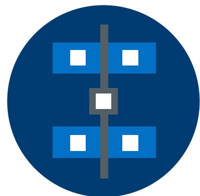
Modular Platform Endless Possibilities for Next Gen



- Opens new product opportunities
- Enables learning and innovation w/ partners
- Accelerates transformative market deployment

Heterogeneous 3D System-in-Package (SiP) Integration

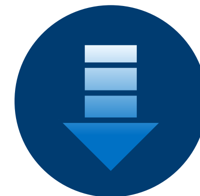
Efficient and Scalable Integration Using Intel® EMIB



Convergence of process nodes and system functions into a **Multi Chip Package (MCP).** Mix and match process nodes

Enables higher efficiency and flexibility.

>20K EMIB connections up to 2 Gbps each



Reduces size, weight, and power

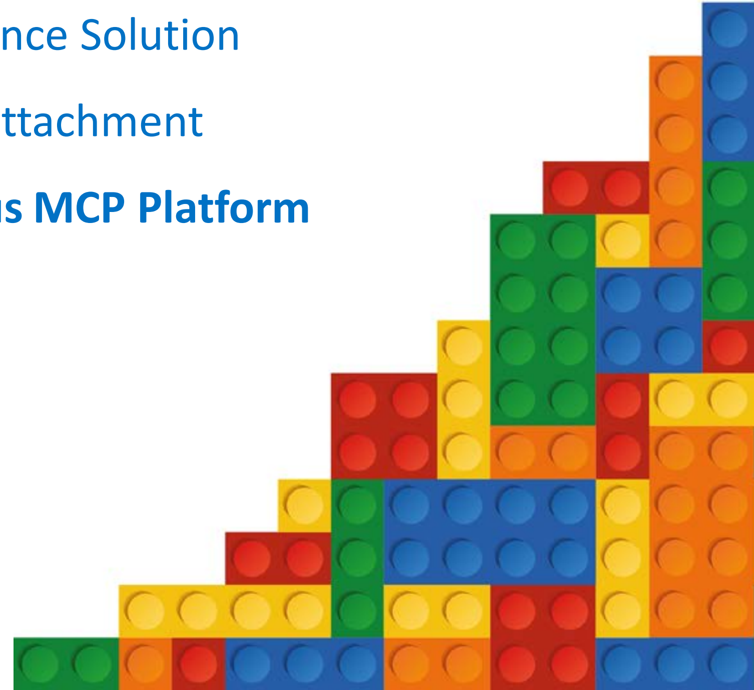
Summary

Heterogeneous Integration For More of Moore

Intel® EMIB Technology is Cost Effective, High Performance Solution

Programmable interface (e.g. UIB and AIB) for flexible attachment

Intel® Stratix® A New Class of Product = Heterogeneous MCP Platform



Heterogeneous Integration
=
Innovation with partners

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