Reconfigure Your RTL with EFLX

Join the SoC Revolution

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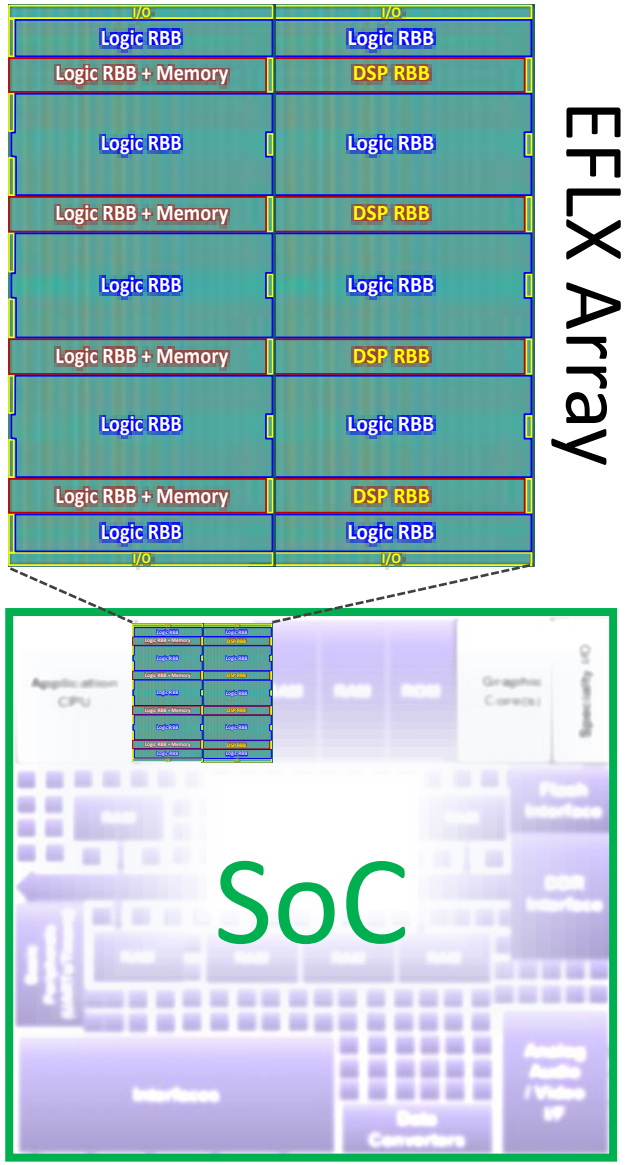
August 22-23, 2016



Why Put an FPGA in Your SoC?

EFLX = Embedded Flexible Logic

- Reconfigure critical RTL
  - up-to-date protocols, encryption, filters, interfaces, …
- Reconfigurable accelerators
- Create new architectures!

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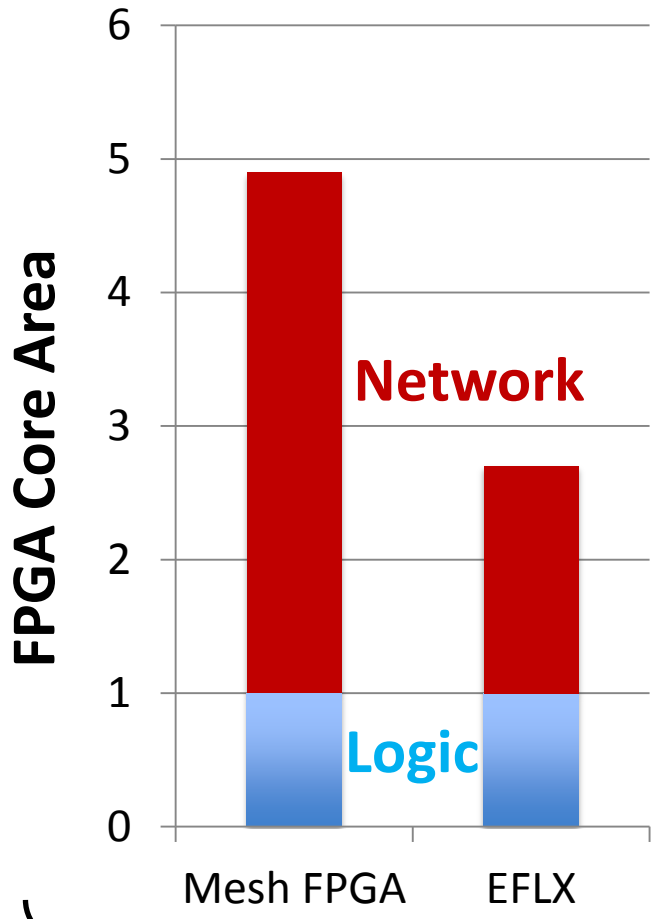
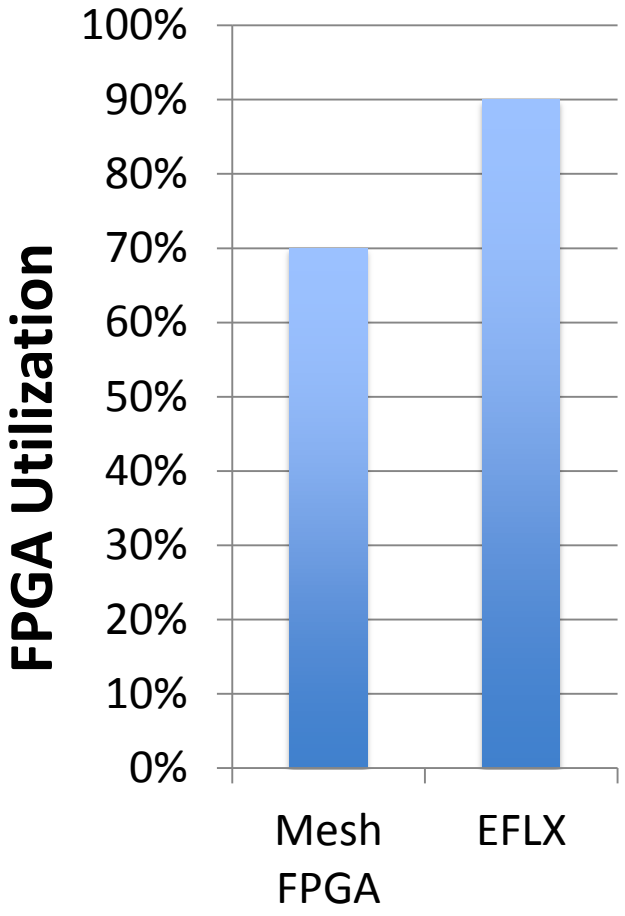
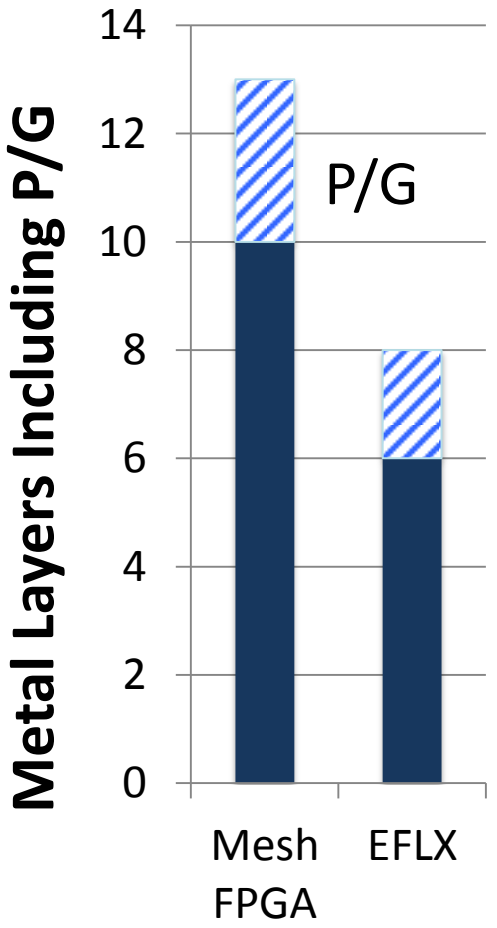
Highly Efficient Network Enables Embedded FPGA







~2x higher utilization of LUTs/mm^2

Compatible with **SoC metal stack**

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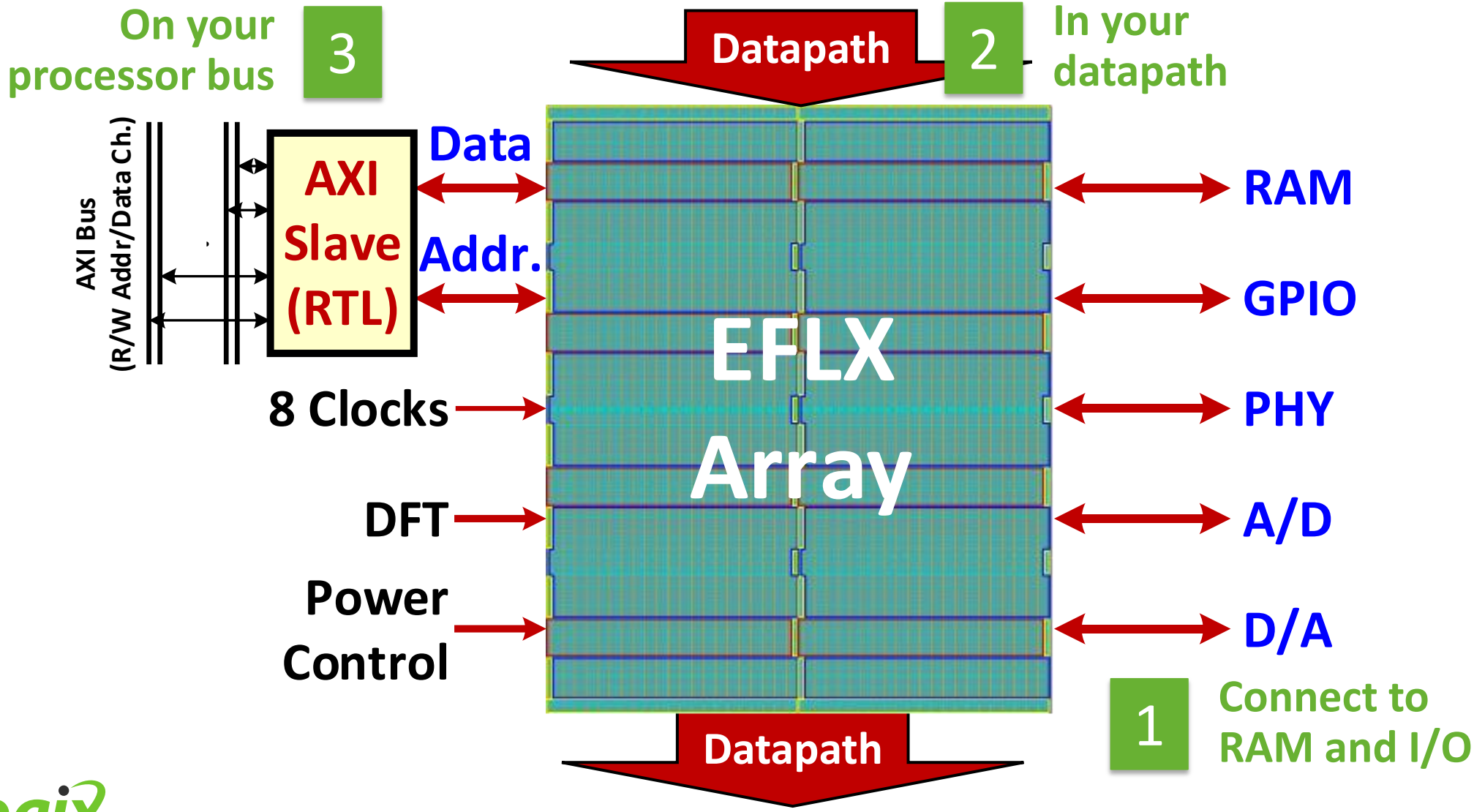
Integrate EFLX with I/O, Datapath &/or Processor



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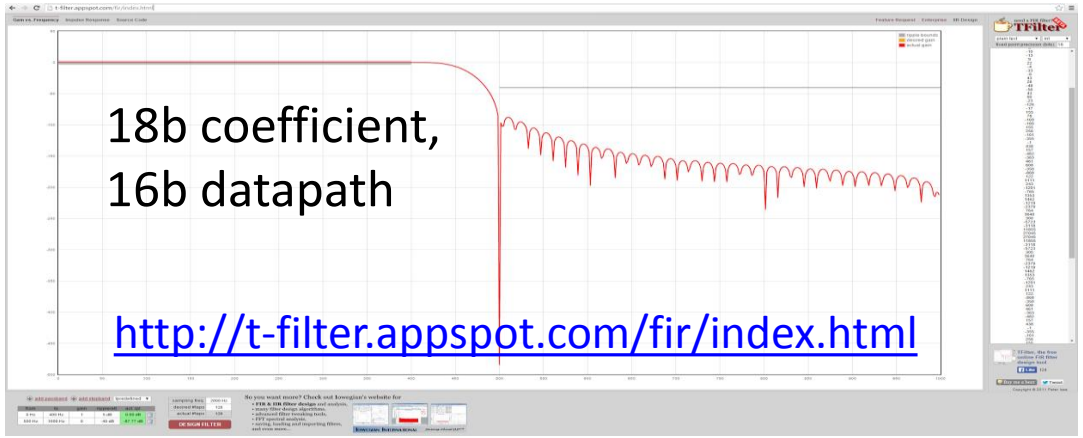
2 3 Example: A 128-tap Programmable FIR

Reconfigure parts or all of RTL in EFLX

- Can **reconfigure coefficients** in EFLX
- EFLX DSP is only 3x larger than ASIC



Design	ASIC RTL mapped to ASIC gates	Same RTL in EFLX Logic LUTs	Optimized RTL in EFLX Logic LUTs	Optimized RTL in EFLX DSP LUTs
LUTs	-	31,775	9,839	0
DSPs	-	0	0	64
2.5K Cores (mm^2)	$0.16mm^2$	12 ($14.28mm^2$)	4 ($4.76mm^2$)	2 ($2.38mm^2$)
Effective area	**$0.16mm^2$**	**$14.28mm^2$**	**$4.65mm^2$**	**$0.476mm^2$**
Relative area	**1**	89	29	**3**

(TSMC 28HPM/C)

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Stop by our demo at the booth