Encoder Logic for Reducing Serial I/O Power in Sensors and Sensor Hubs

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I. Introduction

Sensors such as accelerometers and gyroscopes enable features ranging from step counting in wearables, to gaze tracking in augmented reality applications. Communicating data from these sensors to processors typically occurs over printed circuit board traces and costs between 2 pJ/bit and 40 pJ/bit [2, 5, 6, 7], or up to 40 μW at 1 Mb/s. For systems with many sensors, these costs add up and become comparable to power dissipated in state-of-the-art power-optimized microcontrollers. Encoding sensor data can reduce signal transitions and hence reduce the dynamic power dissipation of sensor data communication. But encoding techniques typically add overhead both on the sender and receiver and require adoption by both sensor and processor vendors.

Value-deviation-bounded serial (VDBS) encoding [9] reduces sensor communication power dissipation by lossy encoding on the sender side, without requiring explicit decoder hardware. It can be deployed over existing serial interface standards such as SPI and I2S, and can be applied to interfaces such as I2C with minor modifications. We present VDBS2RTL, a tool for generating register transfer level (RTL) implementations of the theoretically-optimal transition-reducing VDBS encoders in both VHDL and Verilog. The RTL implementations that VDBS2RTL generates use as few as 61 LUTs for an encoder of 8-bit data when mapped to the iCE40 FPGA, a state-of-the-art small-footprint programmable logic device targeted at sensor applications such as sensor hubs [4].

VDBS2RTL-generated RTL can be incorporated into the digital interfaces of sensors to provide settings that trade lower sensor communication power dissipation for data fidelity. VDBS-enhanced sensors can be deployed with unmodified existing processors and can leverage existing serial interface standards. Because many algorithms that use sensor data can still operate correctly under a wide range of lossy encoding settings [8], system designers can use VDBS2RTL-generated hardware to dynamically adapt the power efficiency of sensor-driven systems. Such dynamic adaptation can prolong battery life for users in cases where they need it the most.

II. Encoder generator

Figure 1 shows the organization of VDBS2RTL. VDBS2RTL takes as input a list of encoding settings which hardware designers specify. It generates as output encoder RTL modules in either VHDL or Verilog, as well as RTL for an encoder configuration selection interface.

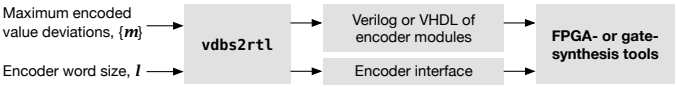

Fig. 1. Organization of VDBS2RTL.

III. Results

We evaluate the RTL generated by VDBS2RTL using the iCECube2 toolchain from Lattice Semiconductor, as well as by using the open-source Yosys tools [10], configured to target the iCE40 FPGA. An 8-bit encoder generated by VDBS2RTL for a maximum output error of 3.9% synthesizes to 61 LUTs using iCECube2 and to 111 LUTs using Yosys. A 12-bit encoder with a maximum output error of 4.9% synthesizes to 100 LUTs using iCECube2 and to 282 LUTs using Yosys. These resource utilizations are only a small fraction of the logic required for a sensor hub controller reference design on the iCE40 [3]. These results show that VDBS2RTL-generated encoders can be effectively incorporated into sensor hubs implemented in programmable logic devices like the iCE40.

We also evaluate synthesizing VDBS2RTL-generated encoders using Yosys for synthesis to gates, and using the Berkeley ABC [1] tools for logic optimization. We then perform technology mapping to a technology library consisting of NOT, NAND, and NOR gates. Using this flow, the 8- and 12-bit encoders synthesize to 865 and 12868 gates, respectively. These gate counts illustrate the feasibility of integrating VDBS encoders into the digital communication interfaces of next-generation sensor integrated circuits.

References

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Abstract

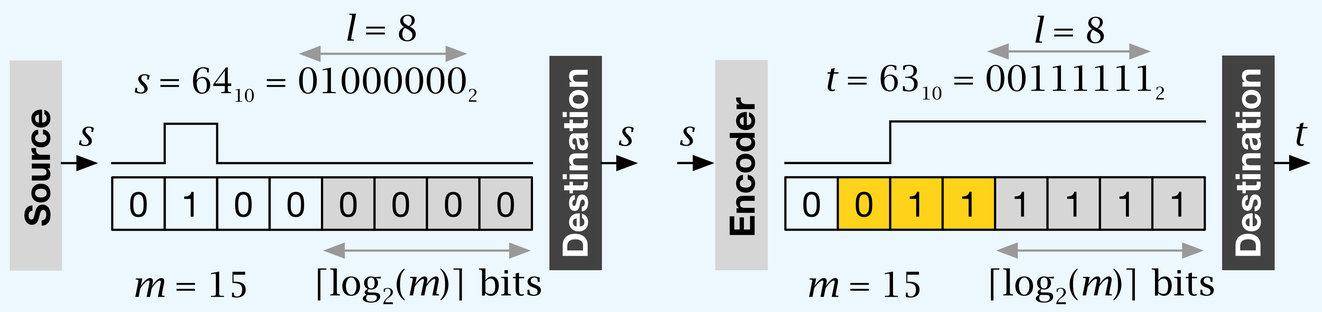
Communicating data from sensors such as gyroscopes and accelerometers, to processors, typically occurs over printed circuit board traces. This communication can cost up to 40 µW at data rates of 1 Mb/s.

VDBS encoding reduces signal transitions and thus reduces the dynamic power dissipation of sensor communication. Because they require no decoder logic, VDBS-enhanced sensors can be used with unmodified existing processors and can leverage existing serial interface standards.

We present `vdbs2rtl`, a tool for generating RTL for the optimal VDBS encoders in both VHDL and Verilog.

① Value-deviation-bounded serial (VDBS) encoding

significantly reduces signal transitions between bits of a single serialized word, trading power efficiency for accuracy.



② VDBS: Analytic Formulation

Let $\#_\delta(s)$ be count of serial transitions in **s**:

$$\#_\delta^l(s) = \sum_{i=0}^{l-2} s_i \oplus s_{i+1}, \quad \textbf{and let } \Delta_{s,t}^l = |\#_\delta^l(s) - \#_\delta^l(t)|$$

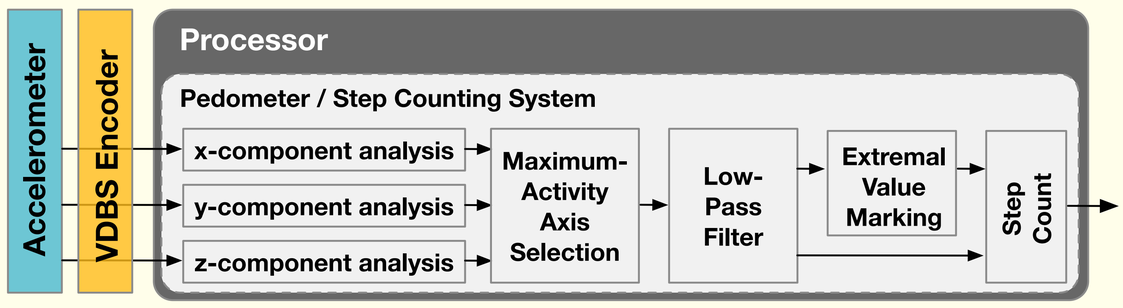
We define a predicate P in terms of $\#_\delta(s)$:

$$\mathrm{P}_{s,t,m} = (|s - t| \leq m) \wedge \left(\left(\#_\delta^l(s) - \#_\delta^l(t)\right) \geq 0\right)$$

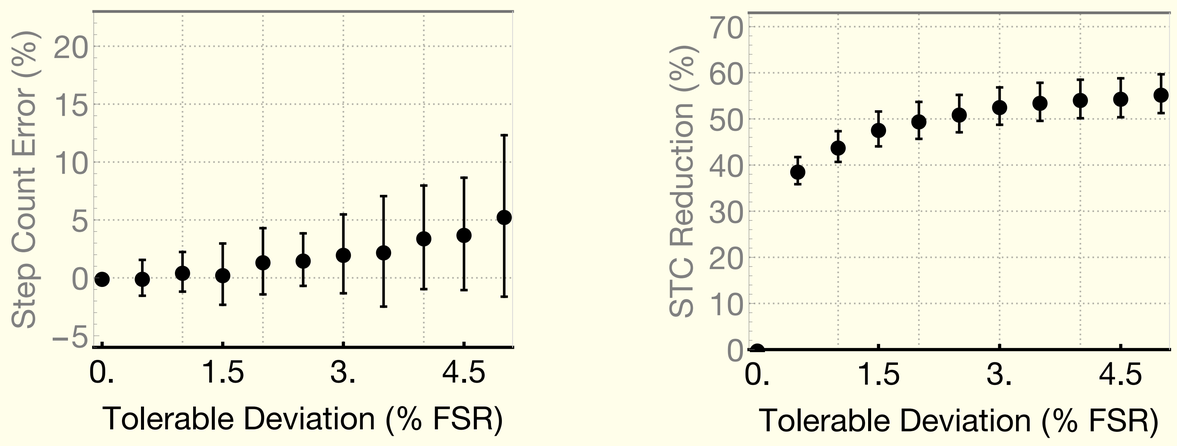
Encoder satisfying predicate that maximally reduces transitions:

$$\mathrm{e}_4^l(s,m) = \left(\tau \;\; \text{s.t.} \;\; \mathrm{P}_{s,\tau,m} \wedge \left(\Delta_{s,\tau}^l = \max_{0<i<2^l-1} \Delta_{s,i}^l\right)\right)$$

③ End-to-End Example: Pedometer

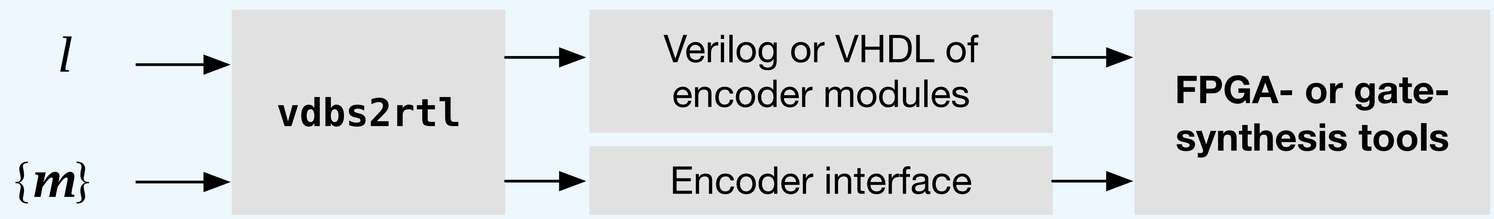


54% dynamic power reduction with only 5% step count error



④ `vdbs2rtl` Tool Flow

Input to **`vdbs2rtl`** is the desired encoder word size, ***l***, and a list of maximum tolerable deviations, {***m***}. The tool outputs RTL for encoders for each setting of maximum tolerable deviation.



⑤ Generated RTL

8-bit encoder RTL generated by `vdbs2rtl` synthesizes to 61 LUTs for iCE40 FPGA (iCECube2) and to 865 gates (Yosys).

12-bit encoder RTL generated by `vdbs2rtl` synthesizes to 100 LUTs for iCE40 FPGA (iCECube2) and to 12868 gates (Yosys).

⑥ Simulating Generated RTL ($l = 8$, $m = 10$)

Contributions

`vdbs2rtl` is a tool for generating RTL for the optimal VDBS encoders in both VHDL and Verilog. The 8-bit encoder RTL generated by **`vdbs2rtl`** synthesizes to 61 LUTs for the iCE40 FPGA and to 865 gates using Yosys for synthesis and technology mapping.

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