An Intelligent ADAS Processor with Real-Time Semi-Global Matching and Intention Prediction for 720p Stereo Vision

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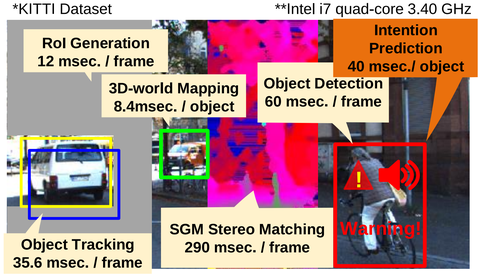
Motivation and Requirements of Intelligent ADAS[1)]

< High-Performance ADAS Function >

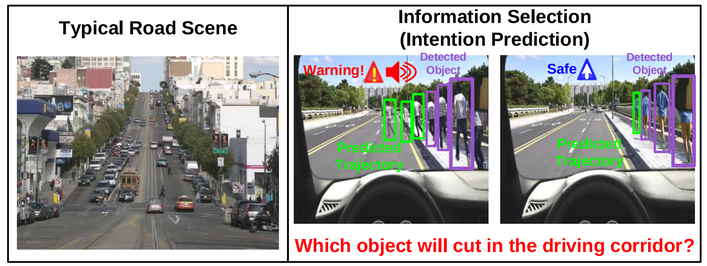
*KITTI Dataset **Intel i7 quad-core 3.40 GHz



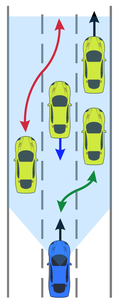
- Several algorithms are executed simultaneously
- Must meet Real-time constraint (> 30fps)
- Global/Dense Stereo-vision is essential (SGM) is essentially required for high-accuracy depth map
- High resolution camera for high-accuracy detection (> 720p)
- Thermal-Design Power constraint due to absence of cooling fans (< 4W)

➔ **High-Performance & Energy-Efficient**

< Intention-Prediction for Selective Information >



- Numerous objects on the road, but providing excessive information to the driver disturbs driving
- Most objects are not risky, but only some are risky to the driver
- Detected objects should be ***intelligently selected & provided*** to the driver
- For advanced functions such as ACC[2)], AEB[3)], or ICE[4)], ***Behavior Analysis*** is essential

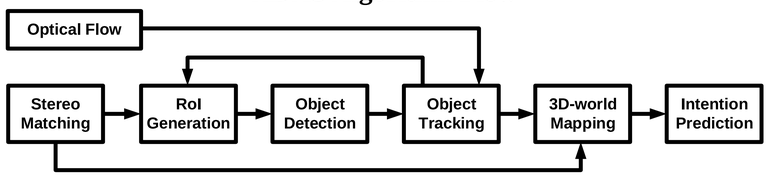


➔ **Objects' Intention-Prediction**

1) ADAS: Advanced Driver Assistance System 2) ACC: Adaptive Cruise Control 3) AEB: Autonomous Emergency Braking 4) ICE: Intelligent Collision Evasion

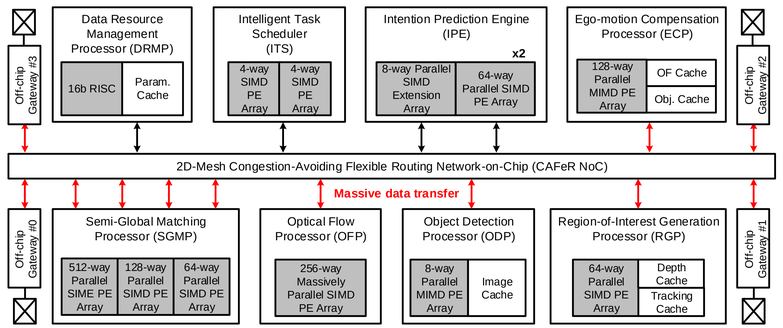
Algorithm-Hardware Mapping and Overall SoC Architecture

< ADAS Algorithm Flow >



- Stereo Matching (SGM) for depth extraction
- Optical Flow for feature tracking
- *Region-of-Interest* generation to reduce computation
- 3D-world Mapping for ego-motion compensation & unit conversion
- Intention Prediction for behavior analysis

< Overall ADAS SoC Architecture >



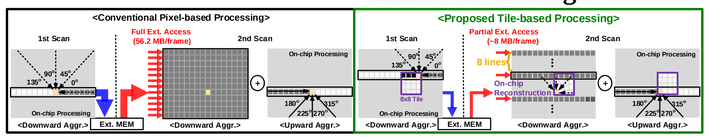
- Many SIMD/MIMD Core Architecture
- Different Parallelism
  1. High Pixel-Parallel Processing
  2. Moderate Pixel-/Task-Parallel Proc.
  3. Complex Task-Parallel Processing

  ➔ DRMP for 3-domain DVFS control
- ITS for workload-prediction & NoC BW Regulation
- *CAFeR* NoC[1] for network congestion reduction

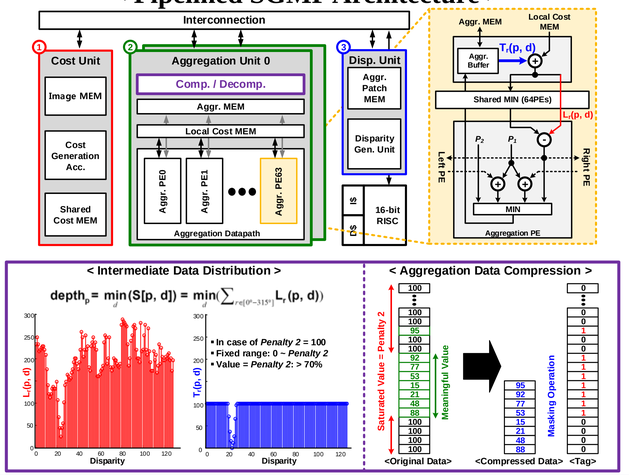
[1] K. Lee, ESSCIRC 2015, "Intelligent Task Scheduler with High Throughput NoC for Real-Time Mobile Object Recognition SoC"

Semi-Global Matching Processor

< Conventional vs. Tile-based Processing >



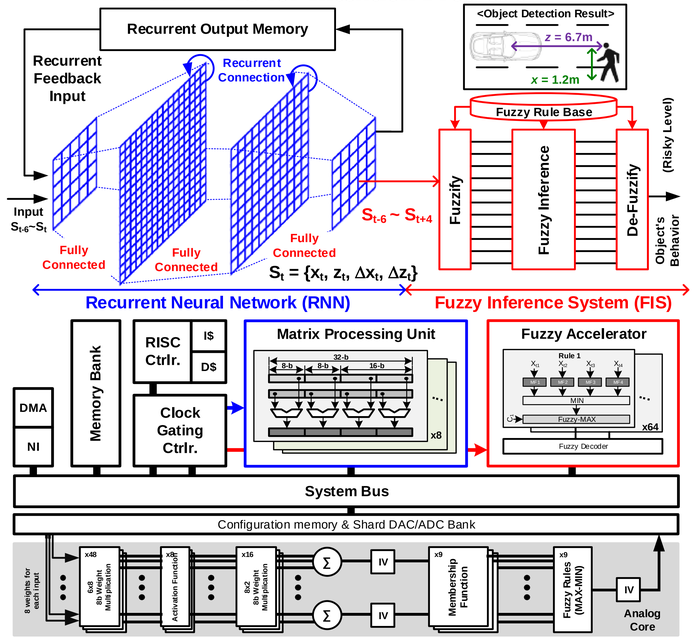
< Pipelined SGMP Architecture >



- In case of *Penalty 2* = 100
- Fixed range: 0 ~ *Penalty 2*
- Value = *Penalty 2*: > 70%

Intention Prediction Processor

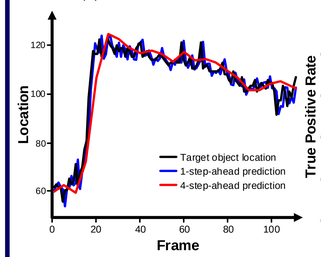
< RNN-FIS for Intention Prediction >



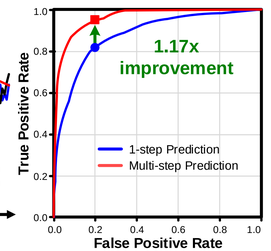
Chip and ADAS Implementation Results

< Measurement & Evaluation Results >

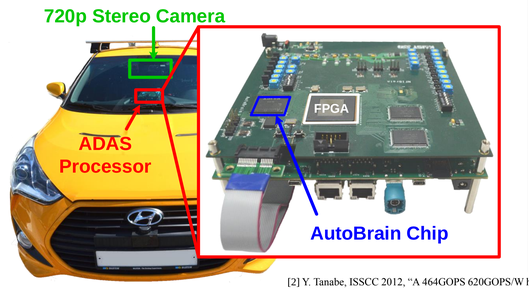
(1) RNN Prediction



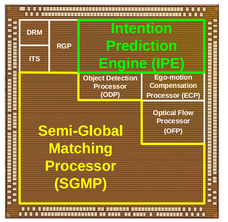
(2) Intention Prediction



< System Implementation >



< Chip Implementation and Spec. >



Process	65nm 1P8M Logic CMOS	
Chip Size	4.0mm x 4.0mm	
Supply Voltage	Nominal	1.2V
	DVFS	0.65 - 1.2V
Clock Frequency	Nominal	250MHz
	DVFS	50 - 250MHz
Power	Average	330mW
	Peak	582mW
Peak Performance	502 GOPS	
Power Efficiency	862 GOPS/W	
Area Efficiency	31.4 GOPS/mm^2	

< Performance Comparison >

	[2] ISSCC'12	[3] ISSCC'13	[4] ISSCC'15	This Work	
				Driving-mode	Parking-mode
Function	Object Detection	Object Detection	Object Detection	Object Detection + Intention Prediction	Intention Prediction + Surveillance Record Trigger
Process	40nm	130nm	40nm	65nm	
Area (mm^2)	45	25	106	16	
Core Voltage (V)	1.1	1.2	1.1	1.2	0.8
Operating Frequency (MHz)	266	200	266	250	20
Power (mW)	749	260	3368	330	0.984
Performance (GOPS)	464	271	1900	502	1.80
Energy Efficiency (GOPS/W)	620	646	564	862	918
Area Efficiency (GOPS/mm^2)	10.3	10.8	17.9	31.4	0.1125
Stereo Matching	Local + Sparse	X	N/A	Global + Dense	Not Used
Intelligence	X	X	X	O	O

[2] Y. Tanabe, ISSCC 2012, "A 464GOPS 620GOPS/W heterogeneous multi-core SoC for image-recognition applications"
[3] J. Park, ISSCC 2013, "A 646GOPS/W multi-classifier many-core processor with cortex-like architecture for super-resolution recognition"
[4] J. Tanabe, ISSCC 2015, "A 1.9TOPS and 564GOPS/W heterogeneous multicore SoC with color-based object classification accelerator for image-recognition applications"

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