A 16nm 256-bit Wide 89.6GByte/s Total Bandwidth In-Package Interconnect with 0.3V Swing and 0.062pJ/bit Power in InFO Package

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Taiwan Semiconductor Manufacturing Company, Ltd.
DTP
Taiwan

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TSMC Property

Outline

- **Motivation**
  - In-Package Interconnect Applications
  - Advance Package Solutions
- **Introduction**
  - InFO Process
  - Low Power Design Concept (2013-VLSI)
- **System Architecture**
- **Circuit Descriptions**
- **Experimental Results**
- **Conclusion**

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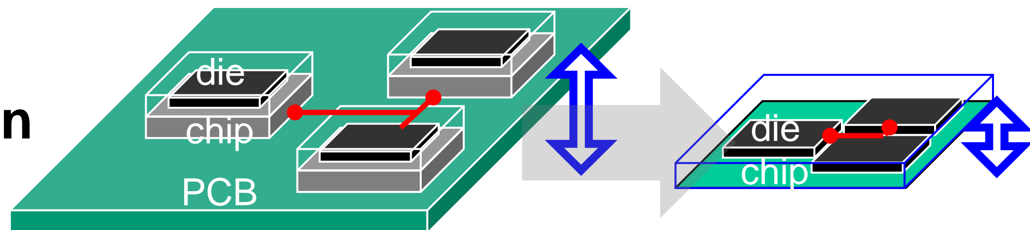
In-Package Interconnect Applications

TSMC Property

- **LIPINCON**™: **L**ow-voltage-**I**n-**P**ackage-**IN**ter-**CON**nect
  - **High performance computing**
    - Limit die size for yield
  - **In package memory**
    - Higher level cache
  - **Heterogeneous integration**
    - High speed SERDES



✓ **Smaller form factor**
✓ **Shorter interconnect trace**

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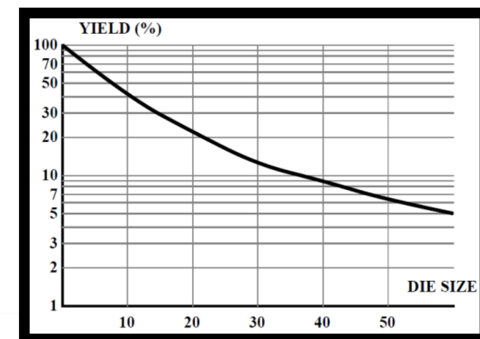
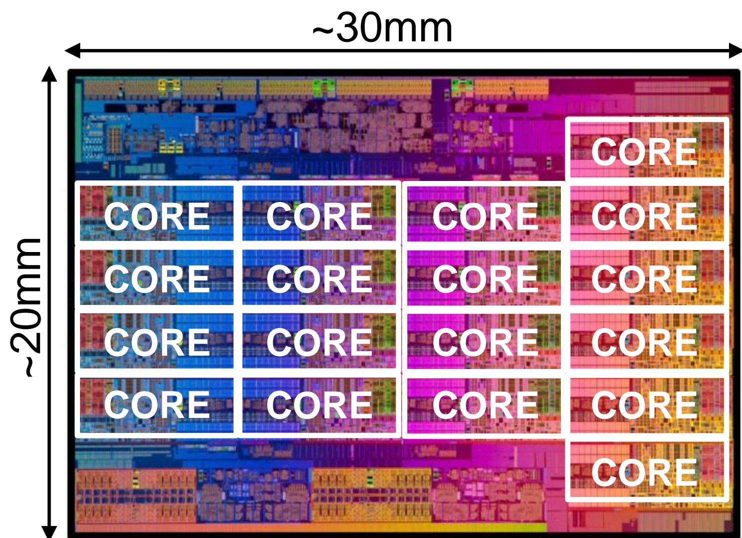
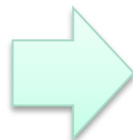
High Performance Computing (HPC)

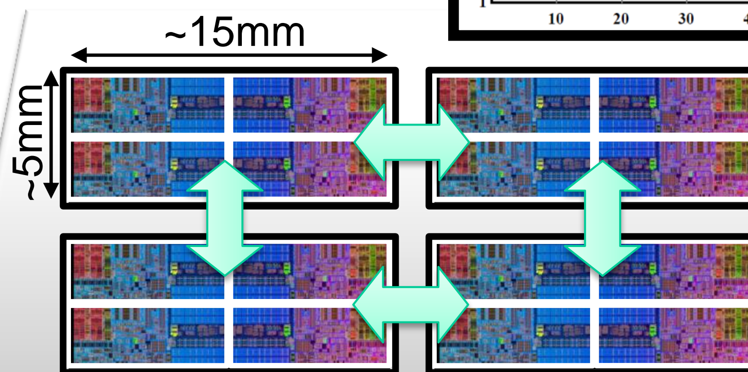
TSMC Property

- Yield goes down exponentially as die size gets large
  - Building large dice is quite difficult and very costly









[1] Intel, 2015-ISSCC, "The Xeon Processor.."

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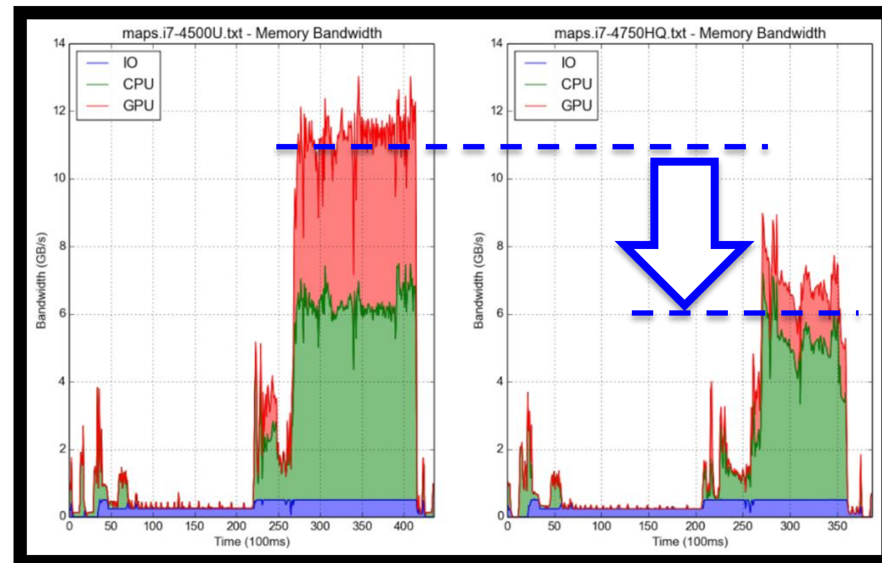
In Package Memory (IPM)

TSMC Property

- Additional memory hierarchy between on-chip SRAM and off-chip DDR
  - Smaller capacity; higher bandwidth; faster latency
- **Advantages**
  - DRAM is more cost-effective than eDRAM
  - Non-TSV allows fine pitch RDL and shorten trace between AP and IPM
  - Short trace enable termination-less IO design



[2] Google, 2015-VLSI, “System Challenges..”

✓ **Save main DRAM bandwidth by 60%**

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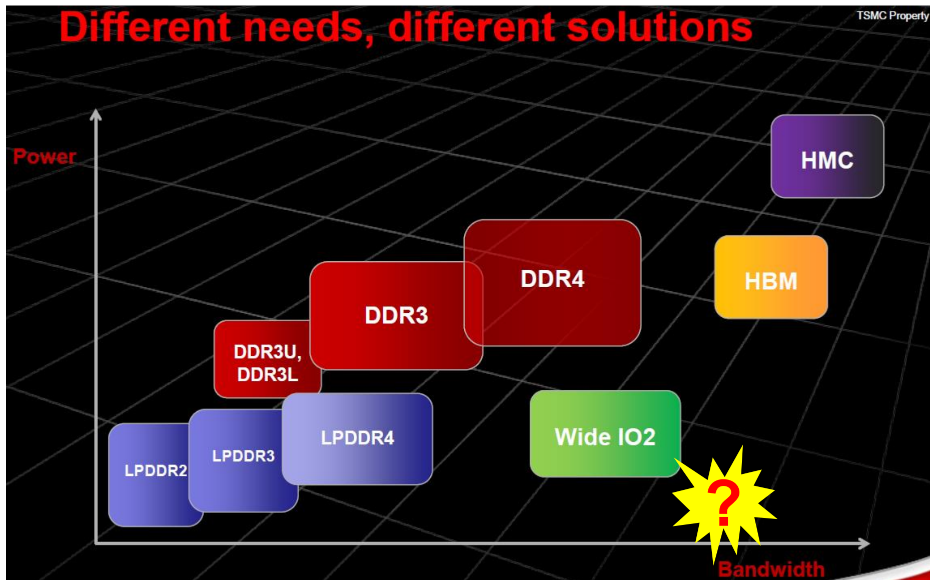
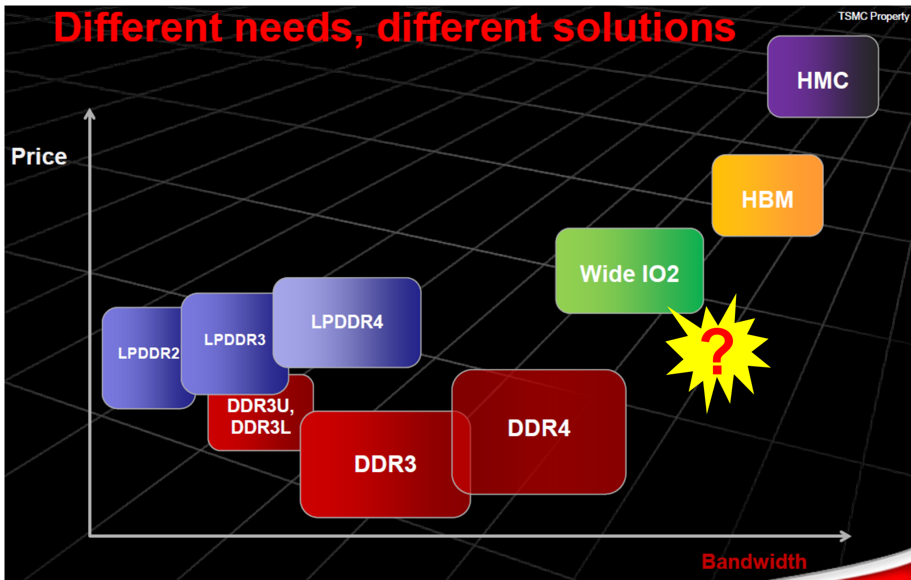
Memory Interface Development Trend

- Higher Bandwidth; Lower Power; Lower Cost (TSV-less)?





[3] TSMC, 2013-OIP "SoC Memory.."

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TSMC Property
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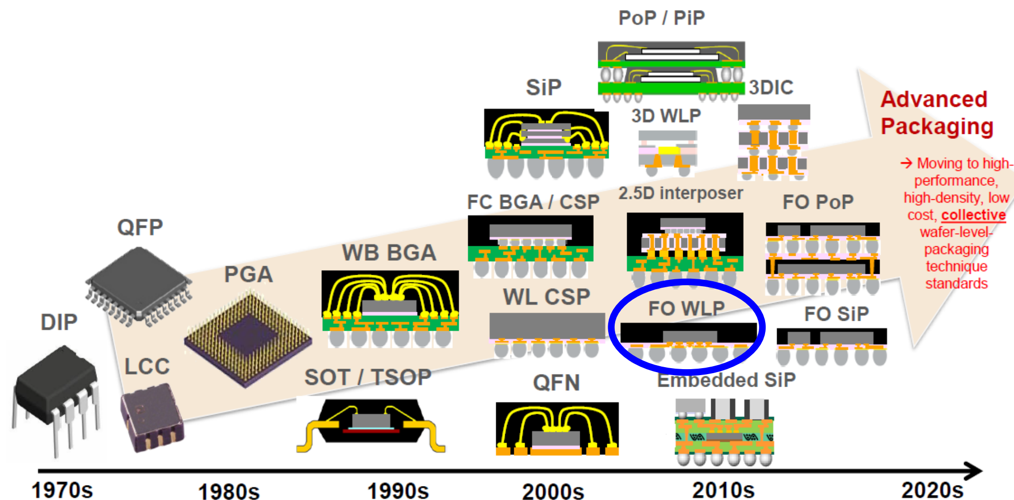
Advanced Package Solutions

TSMC Property

- Why we choose FO-WLP?
  - Ultra-fine pitch RDL (W/S < 5um/5um)
  - Ultra-thin package (~0.6mm including BGA)
  - Smaller die size (no-TSV)
  - Suit for smartphones, tablets, and wearables



[4] 2012 Business Update "3DIC & TSV interconnects"

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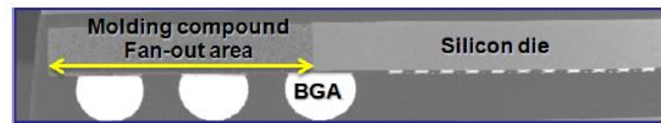
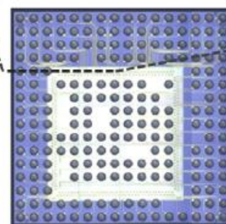
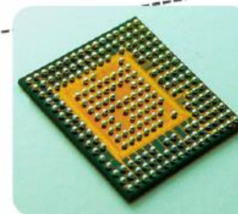
TSMC Package Solution

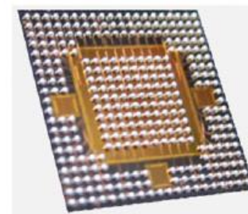
TSMC Property

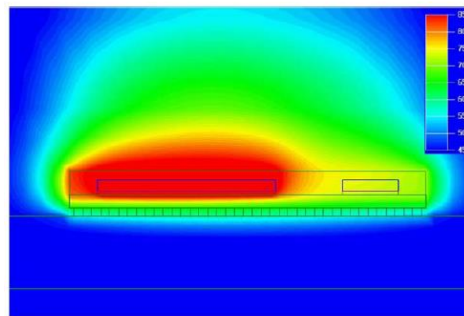
- InFO-WLP (**IN**tegrated **F**an-**O**ut **W**afer-**L**evel-**P**ackage) vs FC-BGA
  - More pin counts with smaller die size
  - Lower parasitic resistance (thicker copper traces)
  - Lower substrate loss (molding compound)
  - Better thermal behavior (smaller form factor)



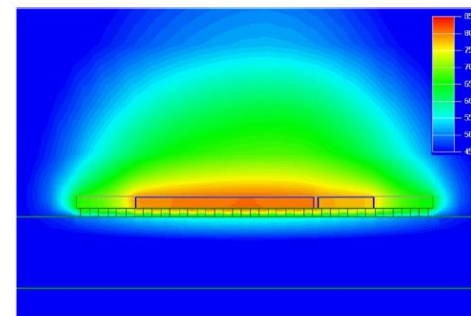








(a) Multi-Chip Module (MCM).



(b) InFO-WLP.

[5] TSMC, 2012-IEDM, "High-Performance.."

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Project Target

TSMC Property

- Demonstrate an in-package interconnect for in-package memory in InFO package
  - Less capable of memory process is considered
- Low-Power ➔ Low-Latency ➔ Small Area
  - Try to be transparent as possible
- 2Gbit/s/pin; 64Gbyte/s total bandwidth
- Power efficient IO
- Prompt and automatic timing-calibration scheme

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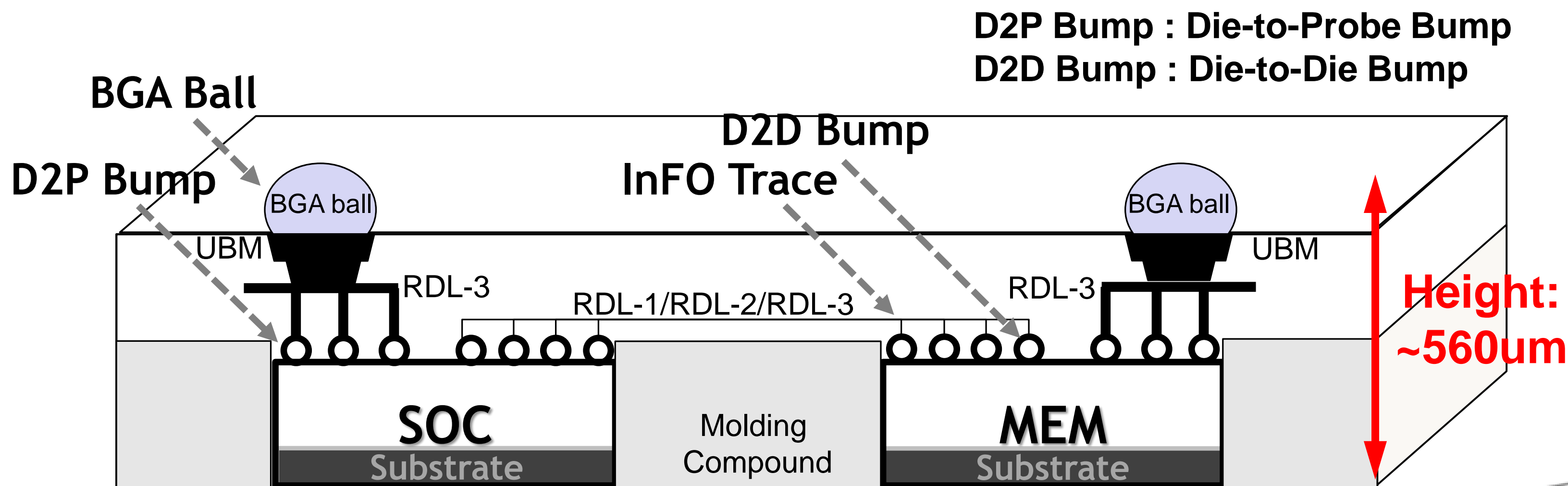
Introduction

TSMC Property

- TSMC InFO side-by-side
  - 560um thickness of packaged chip including 3*RDL & BGA



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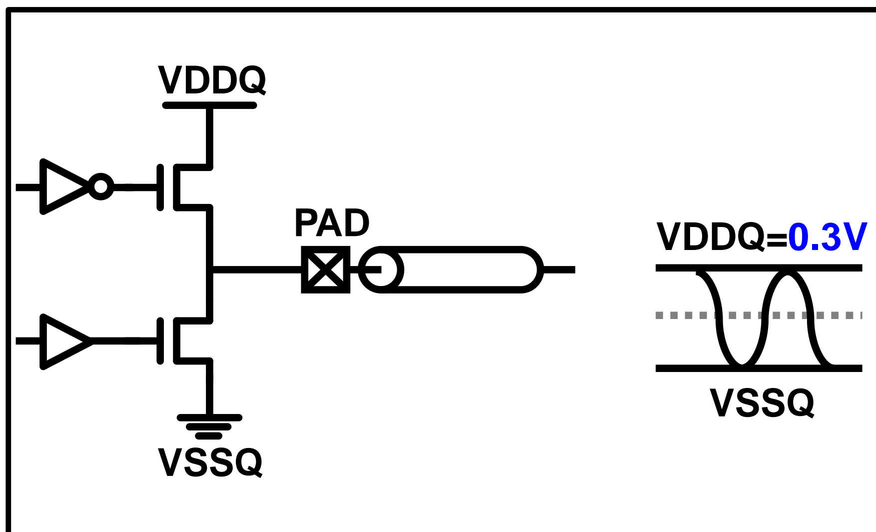
Introduction

TSMC Property

- Low power design concept **2013-VLSI by TSMC**

Reduced-power TX

- Low swing with lower VDDQ
- Termination-less
- Dynamic power only



[6] TSMC, 2013-VLSI, "An extra low-power.."
[7] JESD8-28

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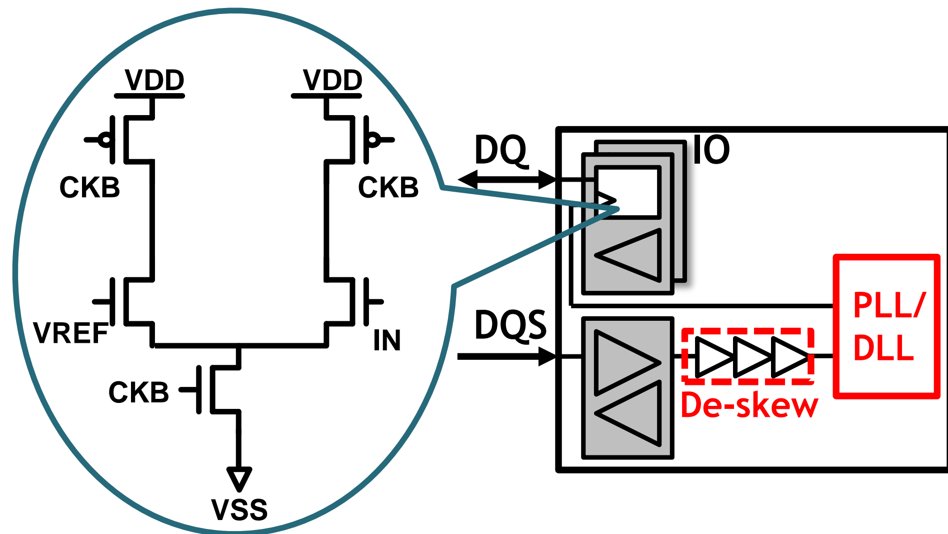
Introduction

TSMC Property

- Low power design concept **2013-VLSI by TSMC**

Reduced-power RX

- Clock-based sense amplifier
- No balance buffer
- Termination-less
- Dynamic power only



[6] TSMC, 2013-VLSI, “An extra low-power..”

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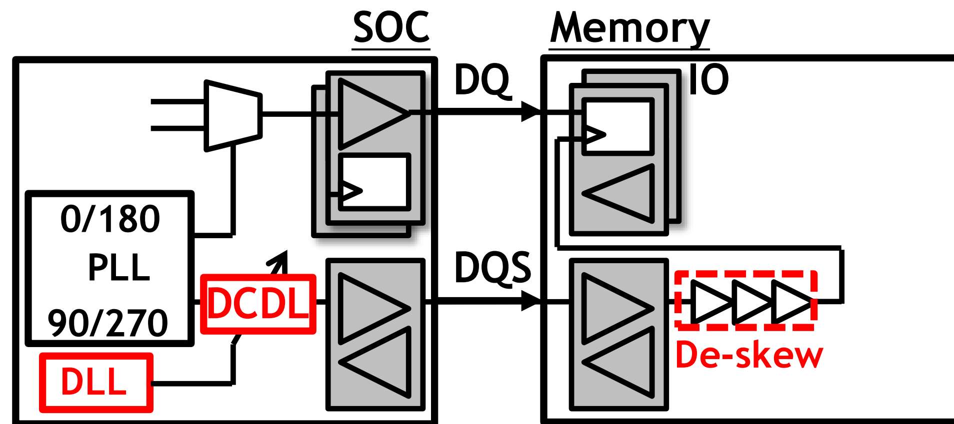
The Proven Path to Success℠

Introduction

- Low power design concept **2013-VLSI by TSMC**

Simplified design in DRAM

- Get rid of DLL/PLL in DRAM



[6] TSMC, 2013-VLSI, “An extra low-power..”

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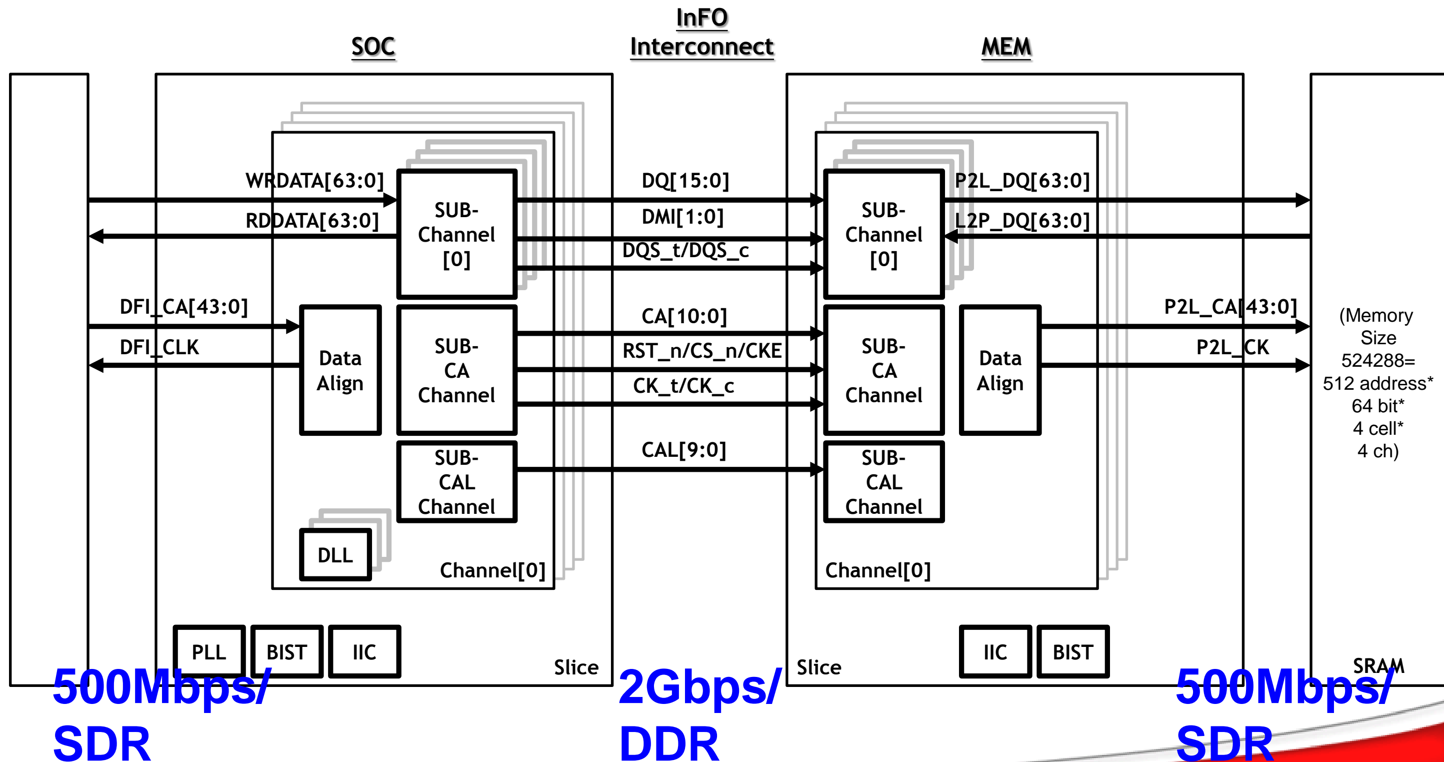
System Architecture

TSMC Property

- 64GByte/s
- 256-DQ
- Bi-directional DQ/DQS
- Modular design
- Easily scalable
- Physical balance



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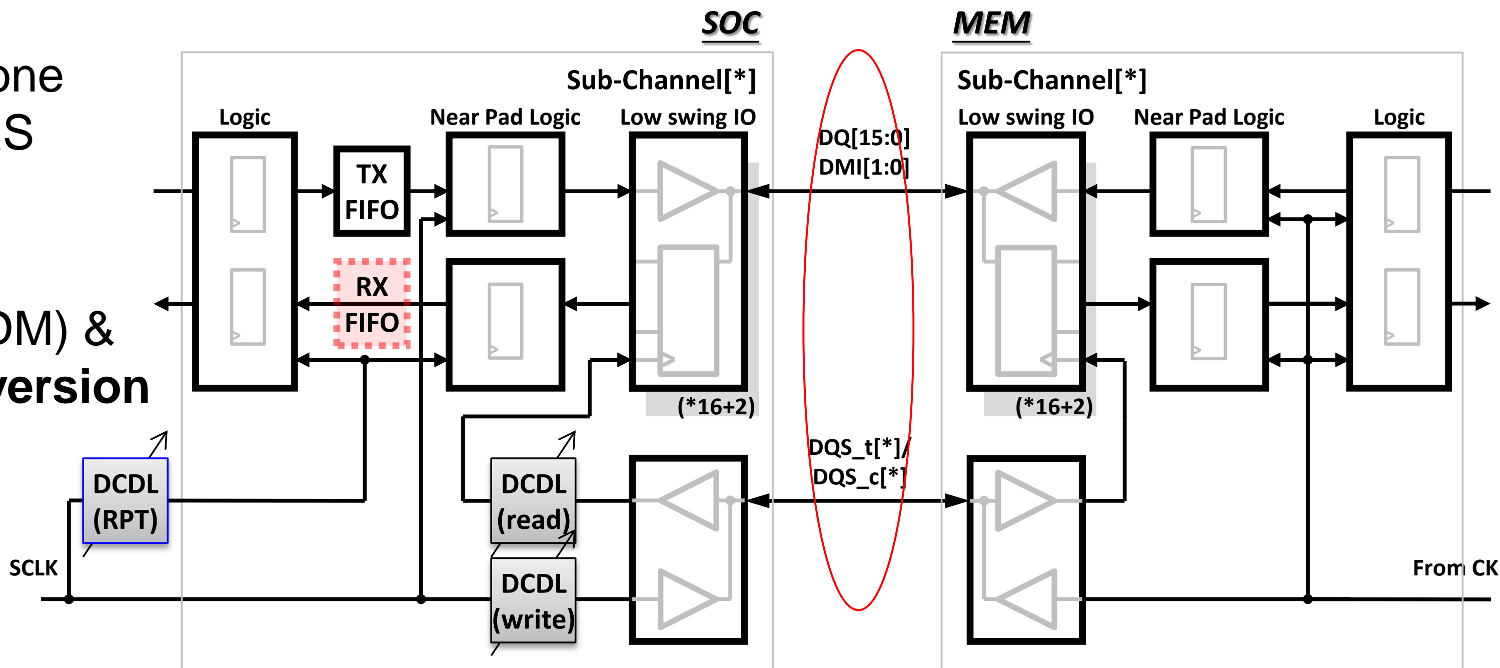
Circuit Description

- Sub-DQ-channel architecture
  - 16-DQ share one differential DQS
  - Per byte DMI combines **Data_mask** (DM) & **Data_bus_inversion** (DBI)



TSMC Property

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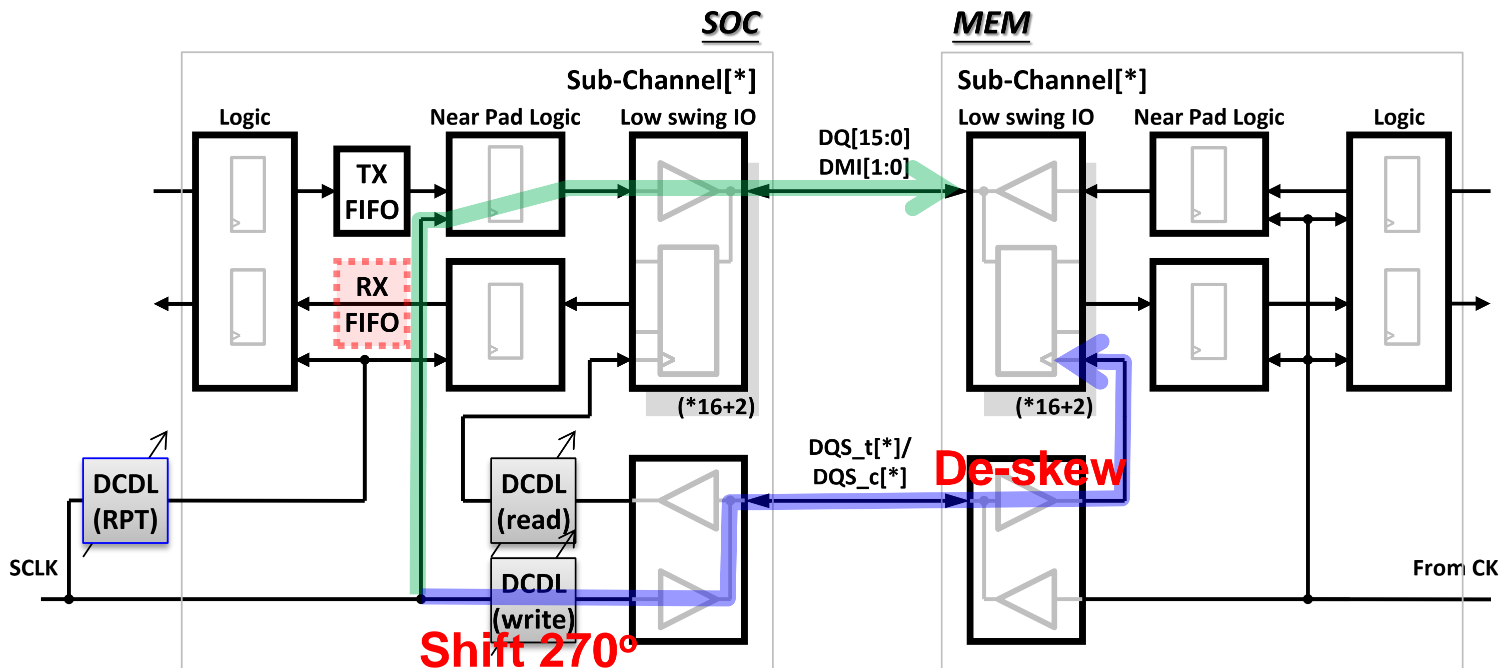
Circuit Description

- Sub-DQ-channel architecture



- WRITE-path
  - DLL-TX [6]

[6] TSMC, 2013-VLSI, “An extra low-power..”

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TSMC Property
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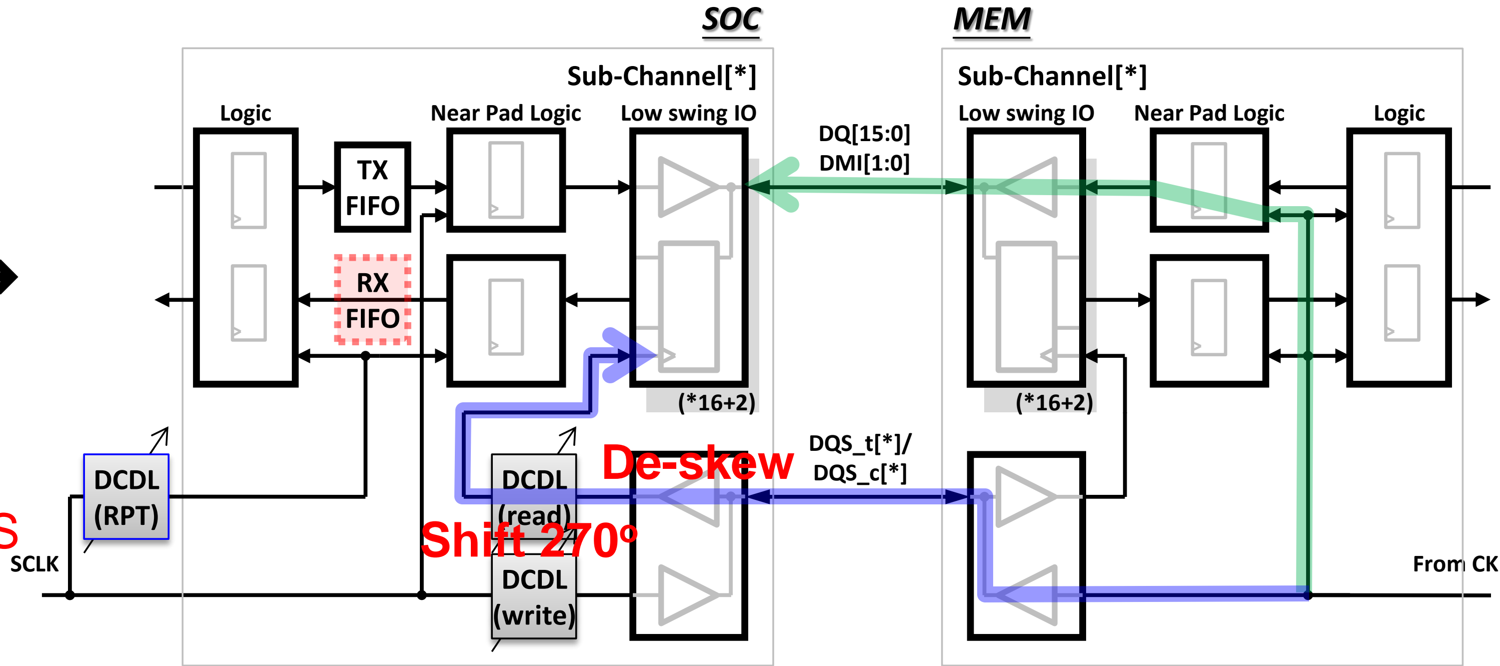
Circuit Description

TSMC Property

- Sub-DQ-channel architecture

- READ-path
  - DLL-RX [6]
  - ~~RXFIFO~~ → DLL-RPT
- Asynchronous clock between SCLK & RDQS



[6] TSMC, 2013-VLSI, "An extra low-power.."

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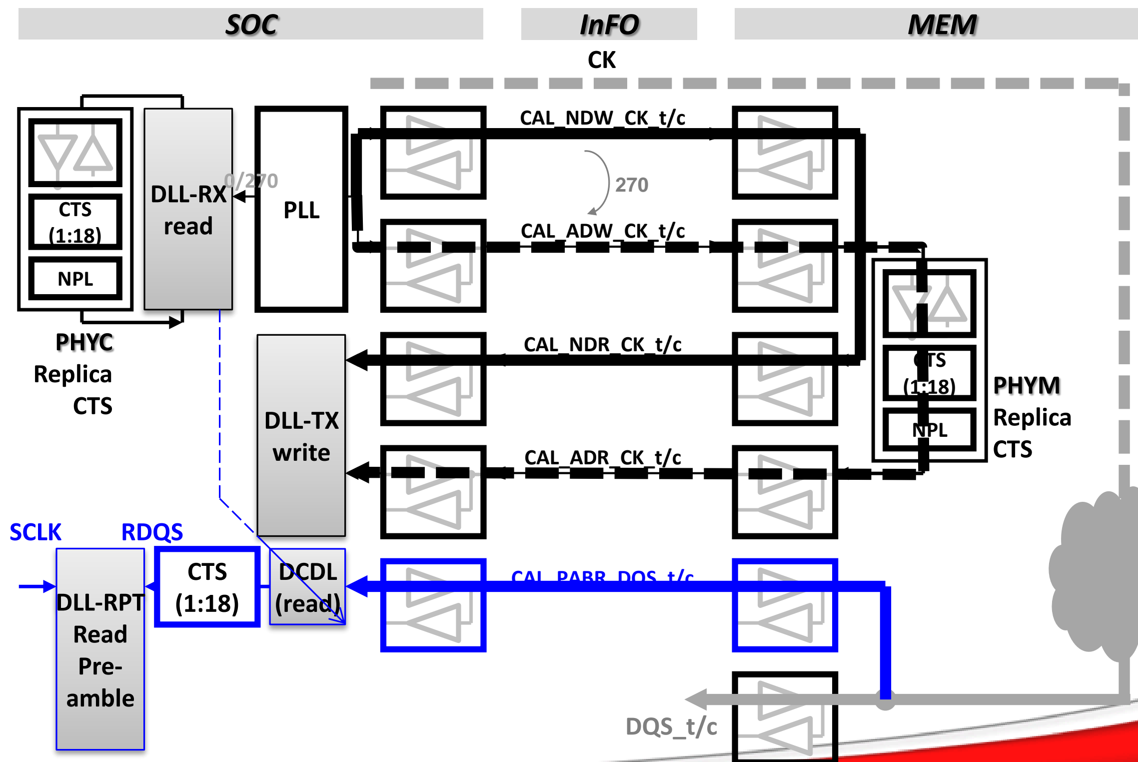
Circuit Description

- Sub-CAL(calibration)-channel architecture

  - 3 DLLs (TX/RX/**RPT**)
  - Prompt and automatic
    - Lock time < **1us**
  - 10-pin overhead shared by 64-DQ
    - But scalable



Note: "RPT"="Read-Preamble-Training"

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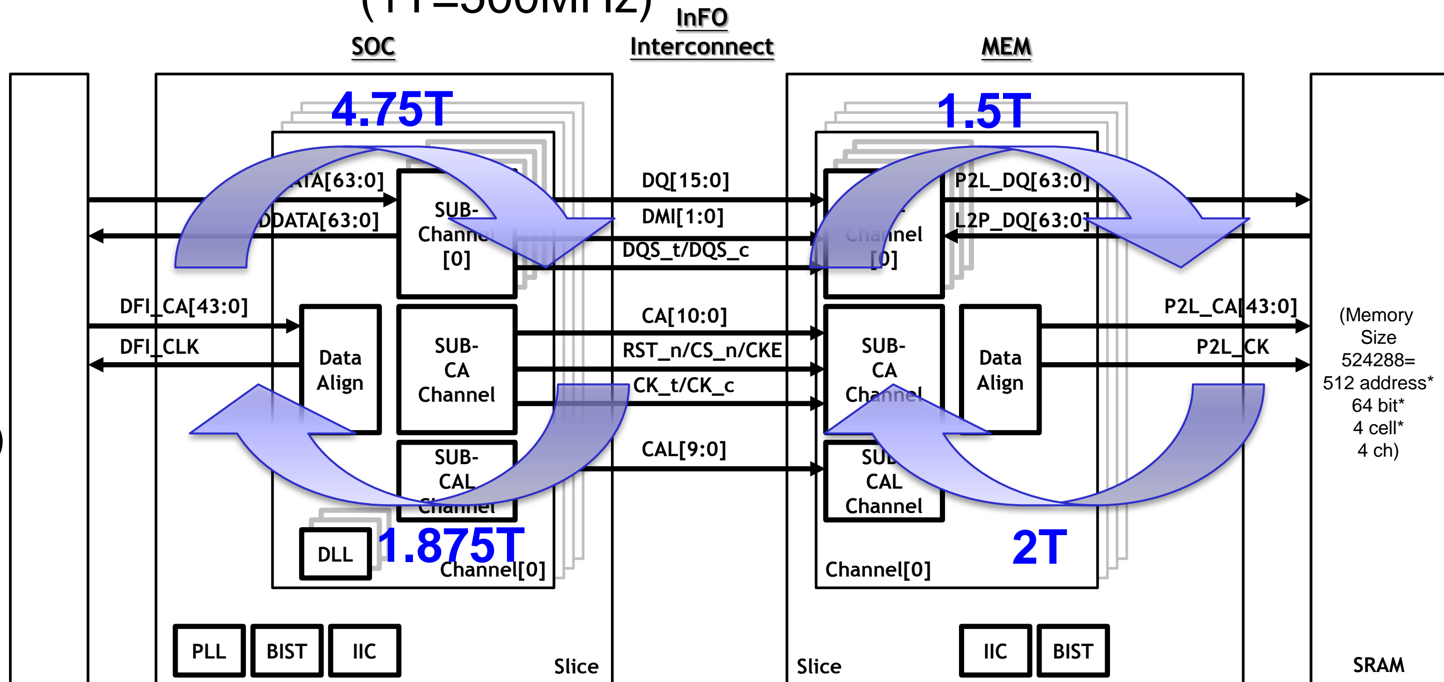
Latency-cost Degrades System Efficiency

TSMC Property

- De-/Serialization ratio: 4
- DBI enable
  (data-bus-inversion)



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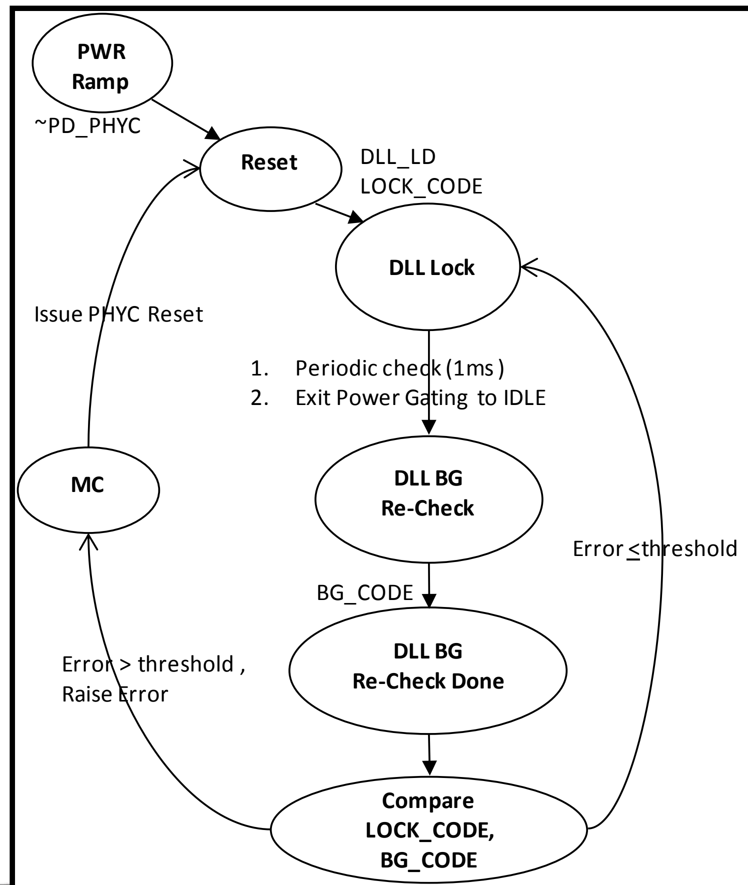
Temperature Drift Monitoring Scheme

TSMC Property

- Temperature drift ➔
  Timing variation ➔
  Performance degradation
- Leveraging DLL architecture
- Periodic check (1ms) **in background**
- Alert issue if drift exceed the tolerance



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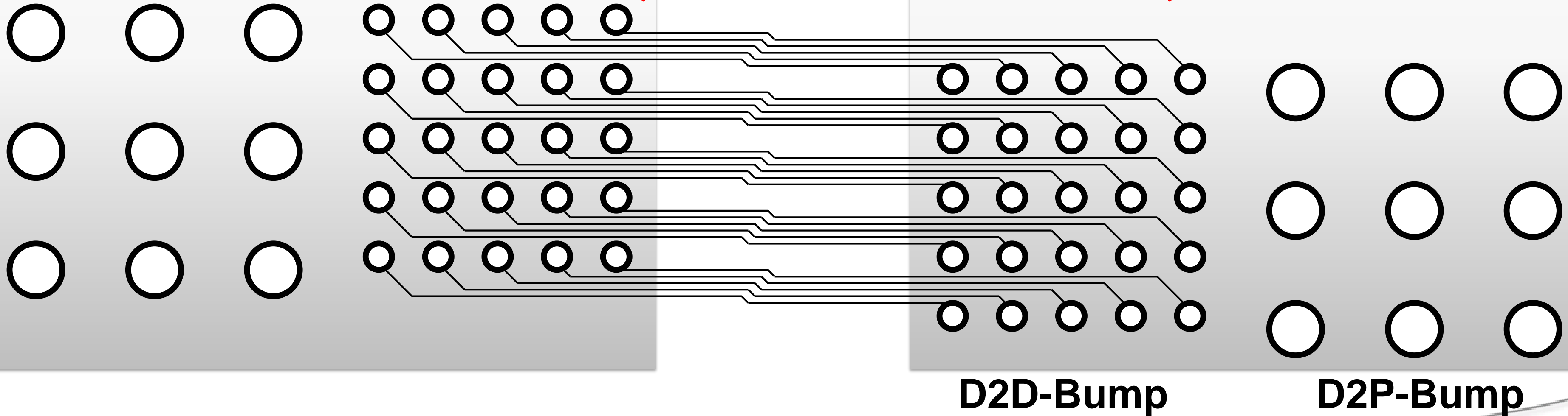
Pad Plan

- Compact pad plan with perfect-match trace length
- RDL routing density: 1*RDL/10um



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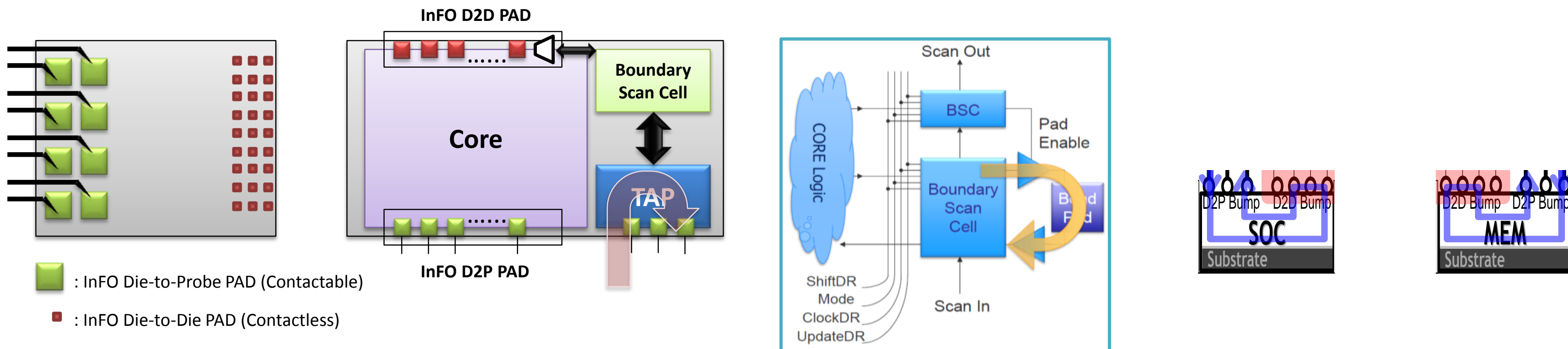
Boundary Scan Strategy

TSMC Property

- **KGD** (Known-Good-Die) – **Contactless IO**
  - Compatible with **IEEE1149.1**
  - Each die builds in self TAP controller
  - Support contactless LIPINCON-IO open/short test individually



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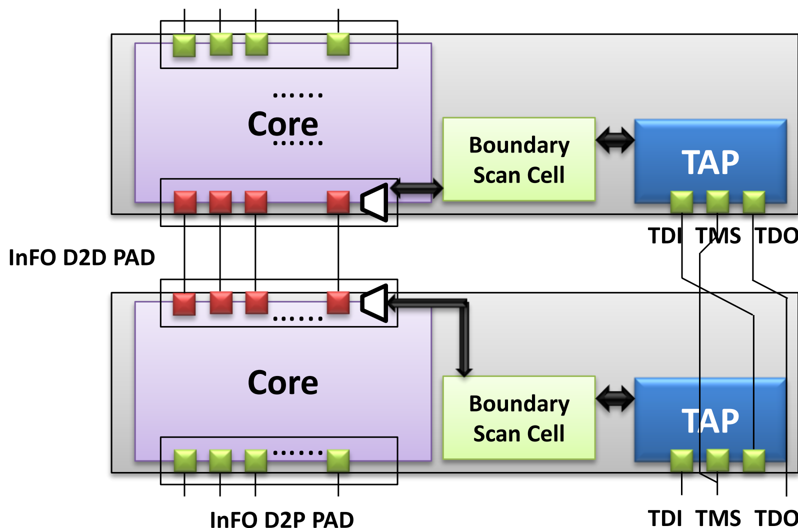
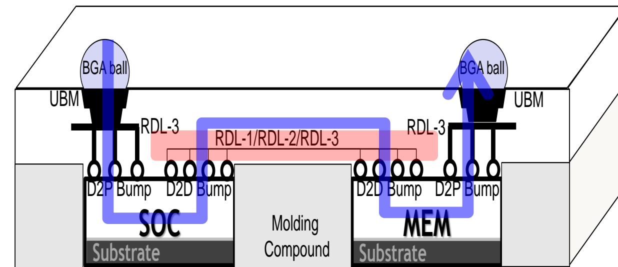
Boundary Scan Strategy

TSMC Property

- **KGS** (Known-Good-Stack) – **Interconnect**
  - Cascade TAP structure and control in sequence
  - Support inter-connectivity test through TAP/Bscan cells
  - Capable of per pin diagnosis





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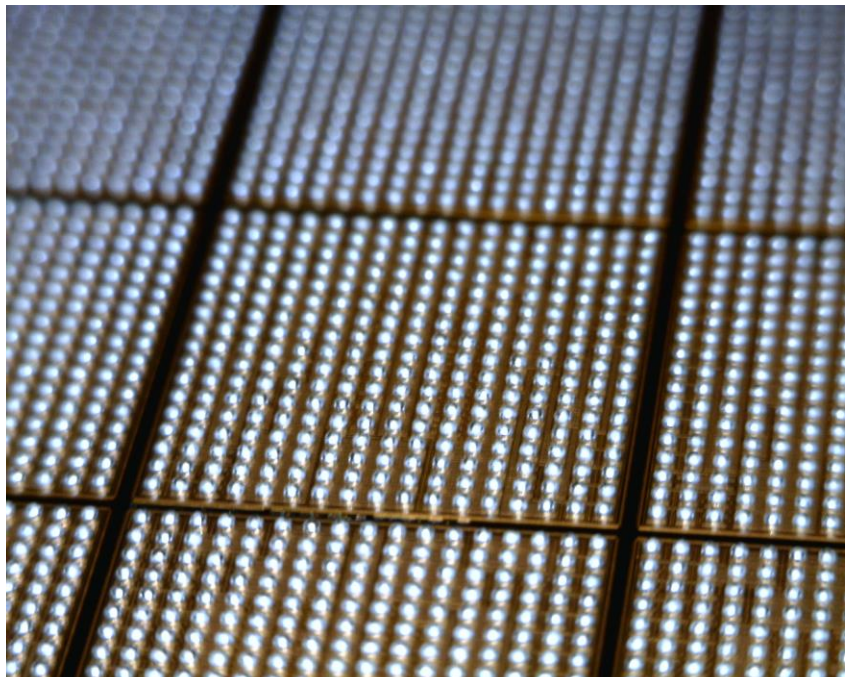
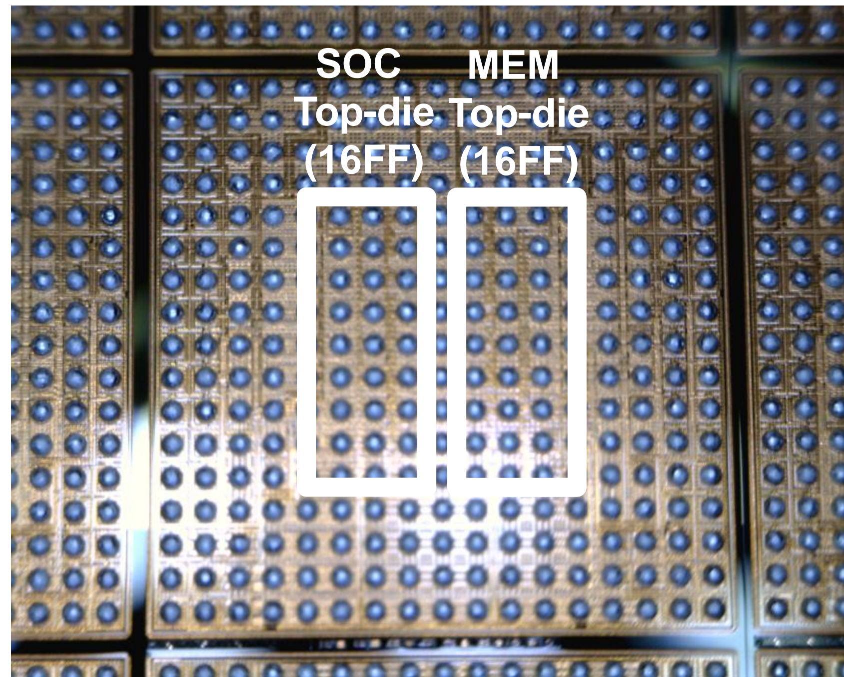
Packaged-Die Photo After InFO

- Fan-out to get the required direct-access BGA balls

[BGA ball side]



[7mm*7mm]



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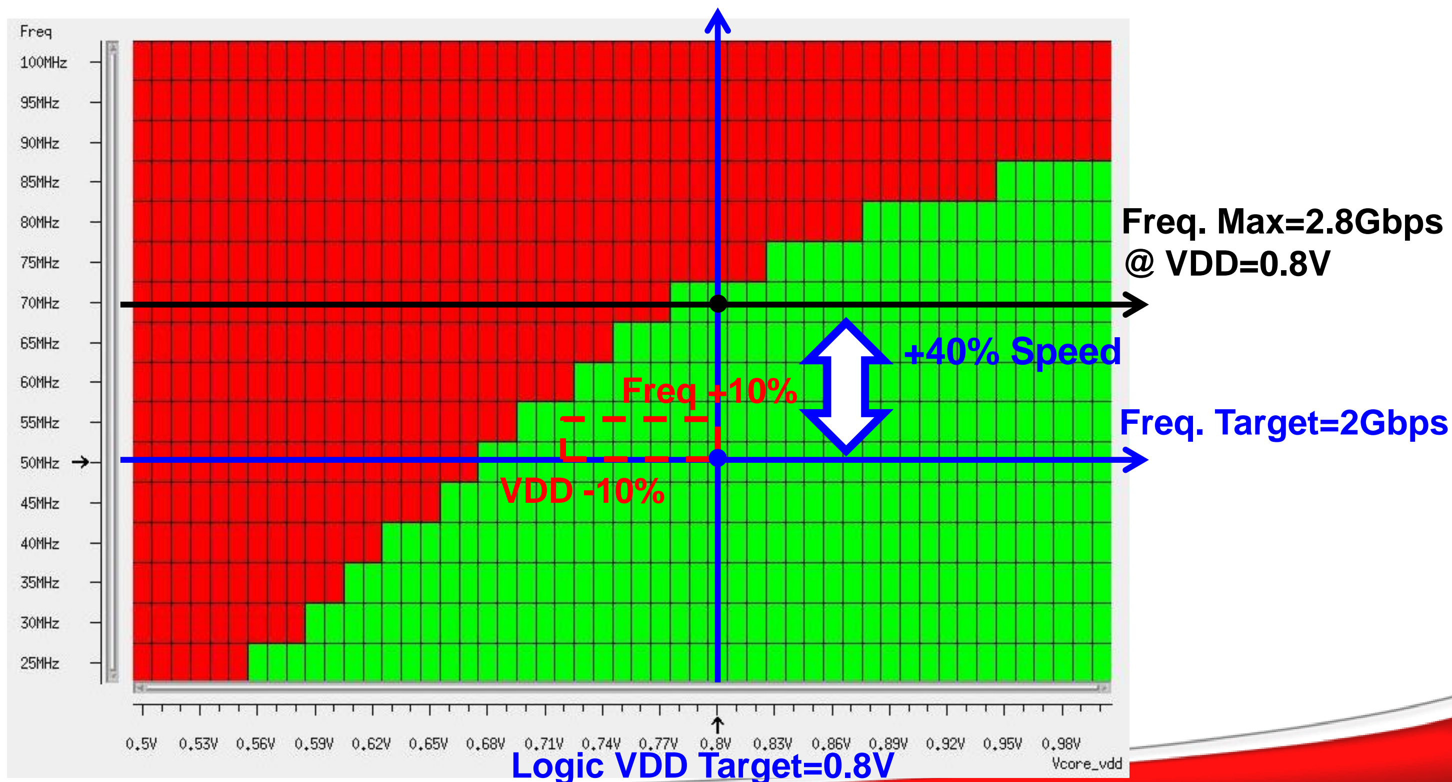
KGD Shmoo Plot

TSMC Property

- SOC/MEM-PHY loopback BIST (Logic VDD vs. Frequency)

- VDDQ=0.3V
- 256-DQ toggle
- DBI enable
- PRBS



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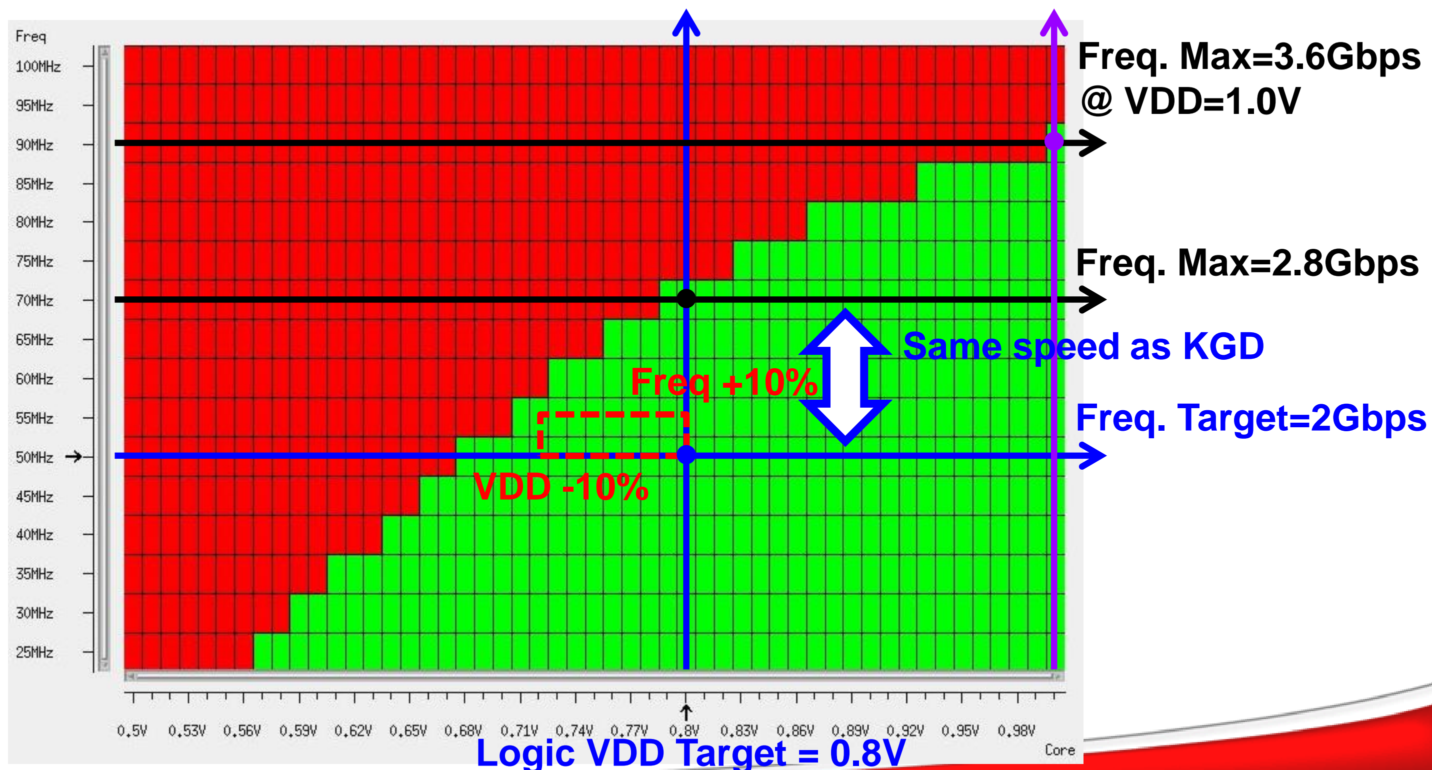
KGS Shmoo Plot

- SOC-to-MEM Write/Read BIST **(Logic VDD vs. Frequency)**

TSMC Property

- VDDQ=0.3V
- 256-DQ toggle
- DBI enable
- PRBS



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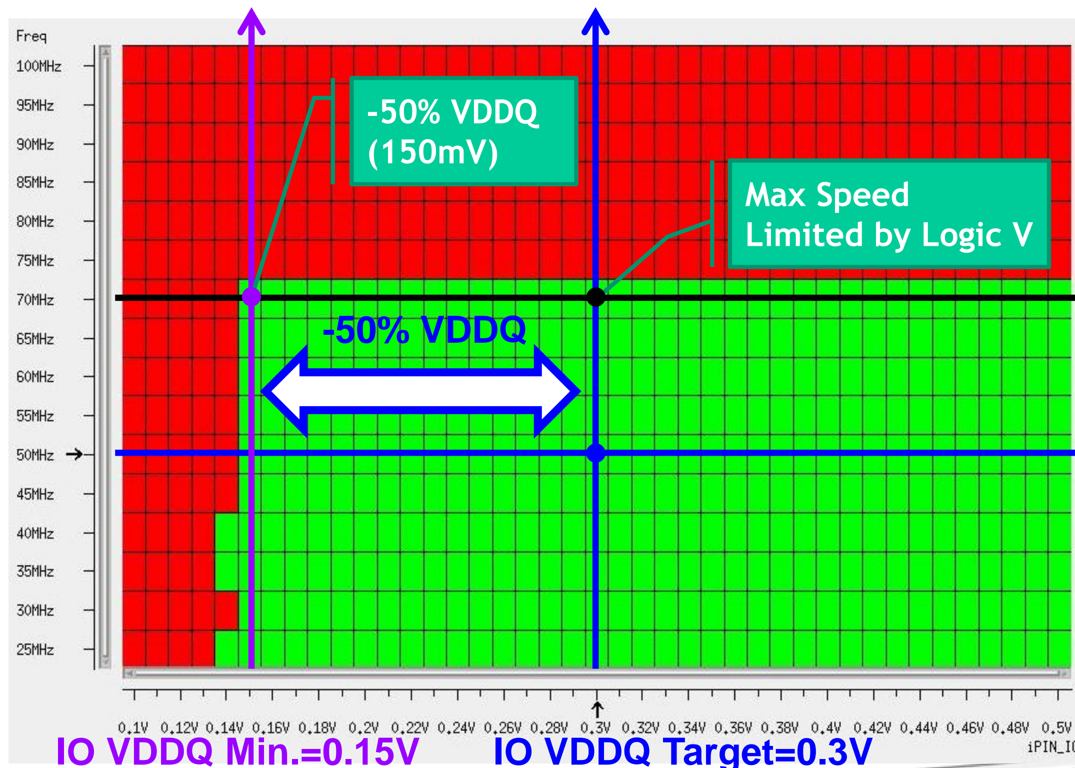
KGS Shmoo Plot

- SOC-to-MEM Write/Read BIST (IO-VDDQ vs. Frequency)

- VDD=0.8V
- 256-DQ toggle
- DBI enable
- PRBS



Freq. Max=2.8Gbps

Freq. Target=2Gbps

IO VDDQ Min.=0.15V

IO VDDQ Target=0.3V

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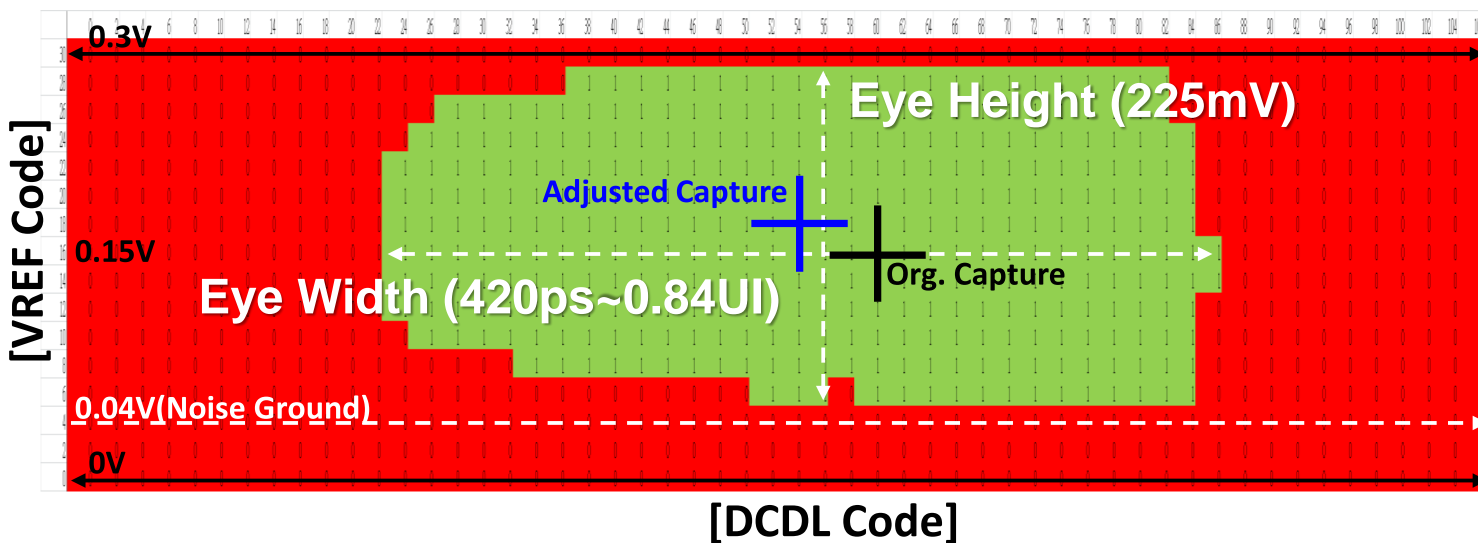
Capable of Eye-ploting

TSMC Property

- 0.3V Swing is critical to SSO under wide bus application
  - How to ensure signal integrity on the un-probed interconnect IO?

- X-axis: **DCDL code (7ps)**
- Y-axis: **VREF code (9.5mV)**
- VDD=0.8V
- 256-DQ toggle
- DBI enable
- PRBS



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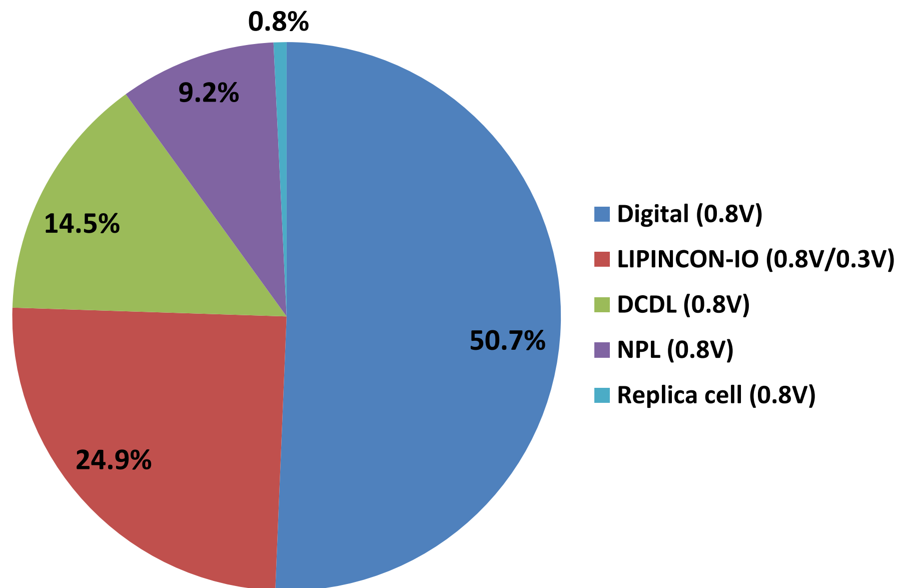
Power Breakdown

TSMC Property

- Base on simulation results with 100% toggling conditions

- LIPINCON-IO power efficiency: **0.062pJ/bit** (consider one single-end IO)
- LIPINCON-PHY power efficiency: **0.424pJ/bit**

Blocks	Power Consumption	Power Efficiency	Percentage
Digital (0.8V)	110.00	0.215	50.7%
LIPINCON-IO (0.8V/0.3V)	53.97	0.105	24.9%
DCDL (0.8V)	31.52	0.062	14.5%
NPL (0.8V)	20.00	0.039	9.2%
Replica cell (0.8V)	1.65	0.003	0.8%
SUM	217.141	0.424	100.0%
	(mW)	(mW/Gb/s)	



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Conclusion

TSMC Property

- An in-package interconnect for in-package memory application in InFO package has been demonstrated
  - Technology: **TSMC 16FF + InFO**
- **89.6GByte/s** total bandwidth is achieved with **256-DQ** operating in **2.8Gbit/s** and **0.3V**-swing
  - Low power: **IO (0.062pJ/bit)**; **PHY (0.424pJ/bit)**
  - Low latency: **Write** (4.75T+1.5T=**6.25T**); **Read** (2+1.875=**3.875T**)
- 0.3V signal integrity on the un-probed IO has been clarified
  - 420ps (**0.84UI**) Eye width; 225mV (**75%**) Eye height
- Prompt and automatic timing-calibration scheme

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Acknowledgement

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The authors would also like to specially thank **“Mentor Graphics”** for boundary scan design collaboration.

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- [7] JESD8-28 "300mV interface"

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