Design and development of a an Ultra-Low Power Intel Architecture MCU Class SoCs

HotChips 2016

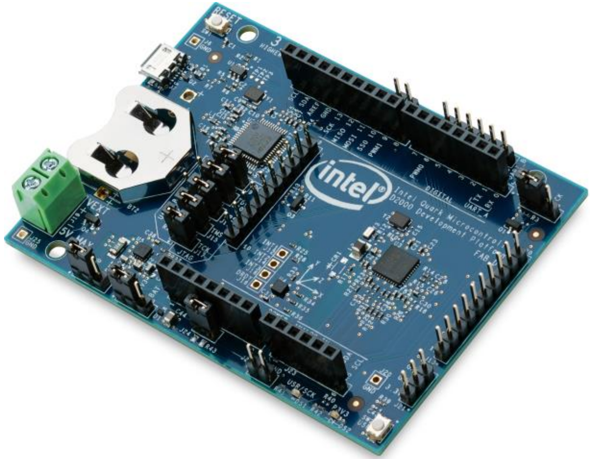
Peter Barry, contributions from Venkat Madduri & Raj Kothandaraman.

Overview

- Back to the future…
- Microcontroller Characteristics
- Intel® Quark™ Microcontroller D2000
- X86 tradeoffs for microcontrollers
- SoC level microcontroller tradeoffs.

1991… ..2016

Source: InfoWorld - 1991



- Yesteryears desk top is todays microcontroller.
- 33Mhz 486/Pentium Era – early ’90

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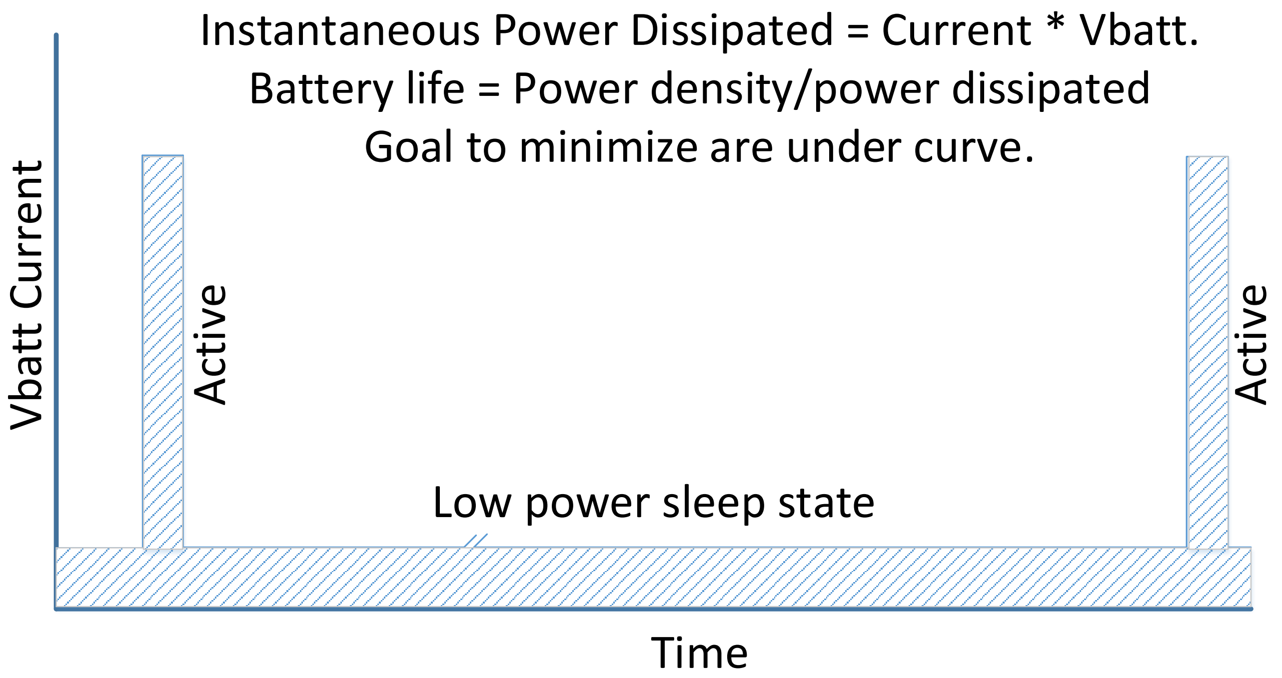
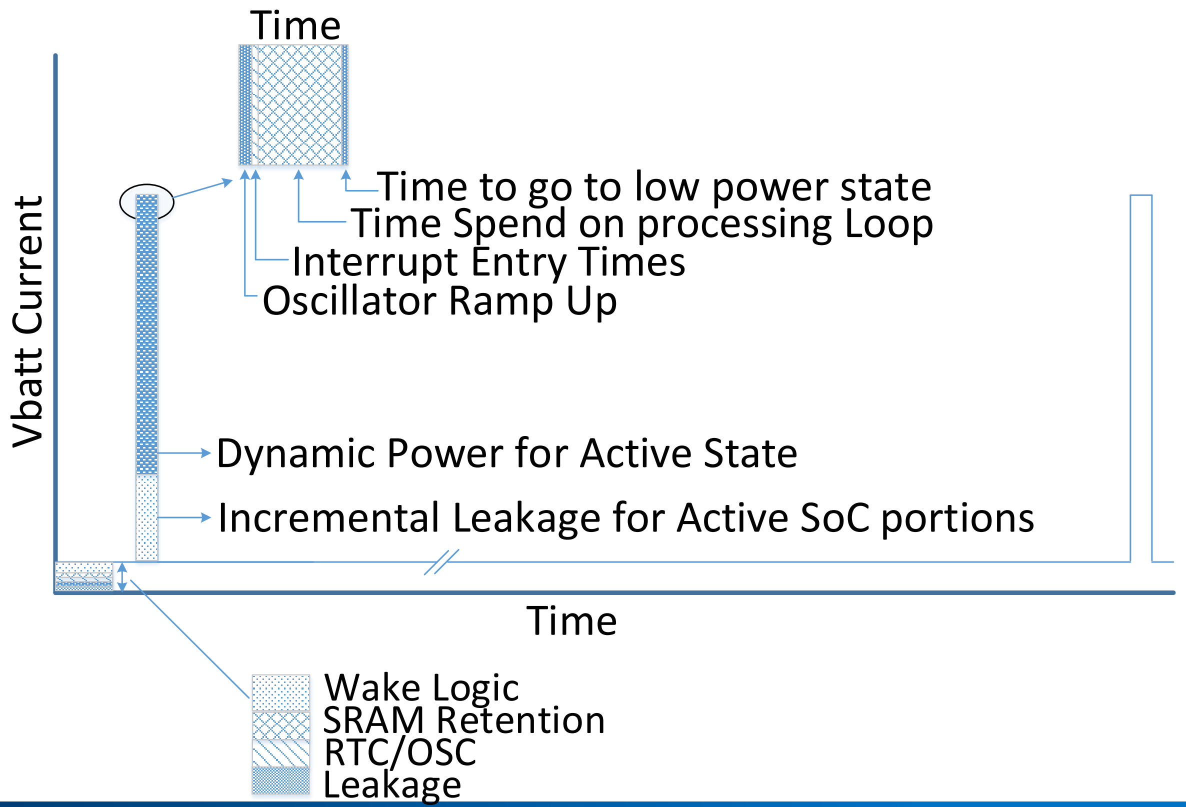
Microcontroller Characteristics

- Design targets for long life from battery
- Typically integrated Flash and SRAM.
- Mixed signal, DACs/ADCs/Comparators/Radios
- Duty Cycled use cases
  - ratio between low power and active states are critical.
- Application managed power state transitions.

Duty Cycling – active to sleep ratios



Expanded Power analysis



Product architecture driven by process

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Entry Edge Controller: D2000

Battery-operated

- <35mW active, <10uW idle*
- Months/years activity dependent on use case

Intel® Architecture Microcontroller

- Extensible End Point
- 40pin QFN

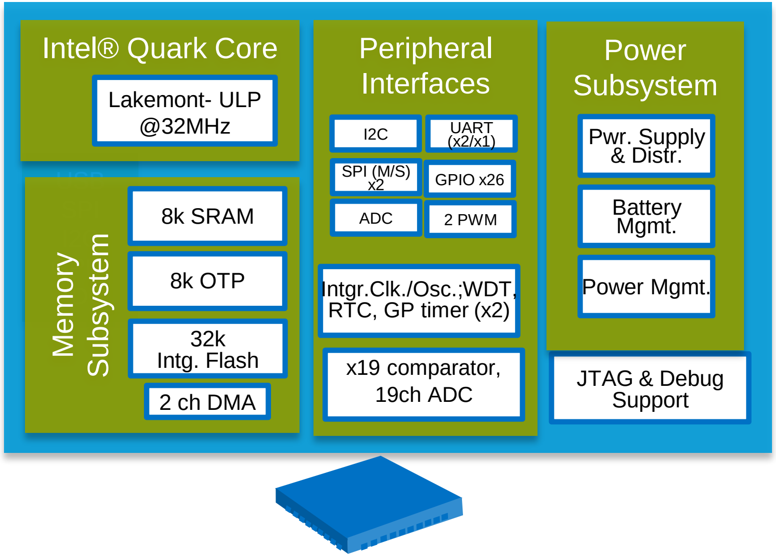
Scalable SW applications & Tools

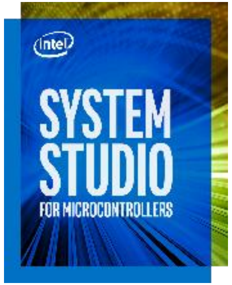
Intel® System Studio for Microcontrollers

- Free development tools, (GCC* Compiler, JTAG Debugger, flashing, optimized C and DSP libraries)
- Scalable Intel® Quark™ Microcontroller Interface API

Hardened

- -40 to 85°C ambient, 10 year reliability
- Long life availability





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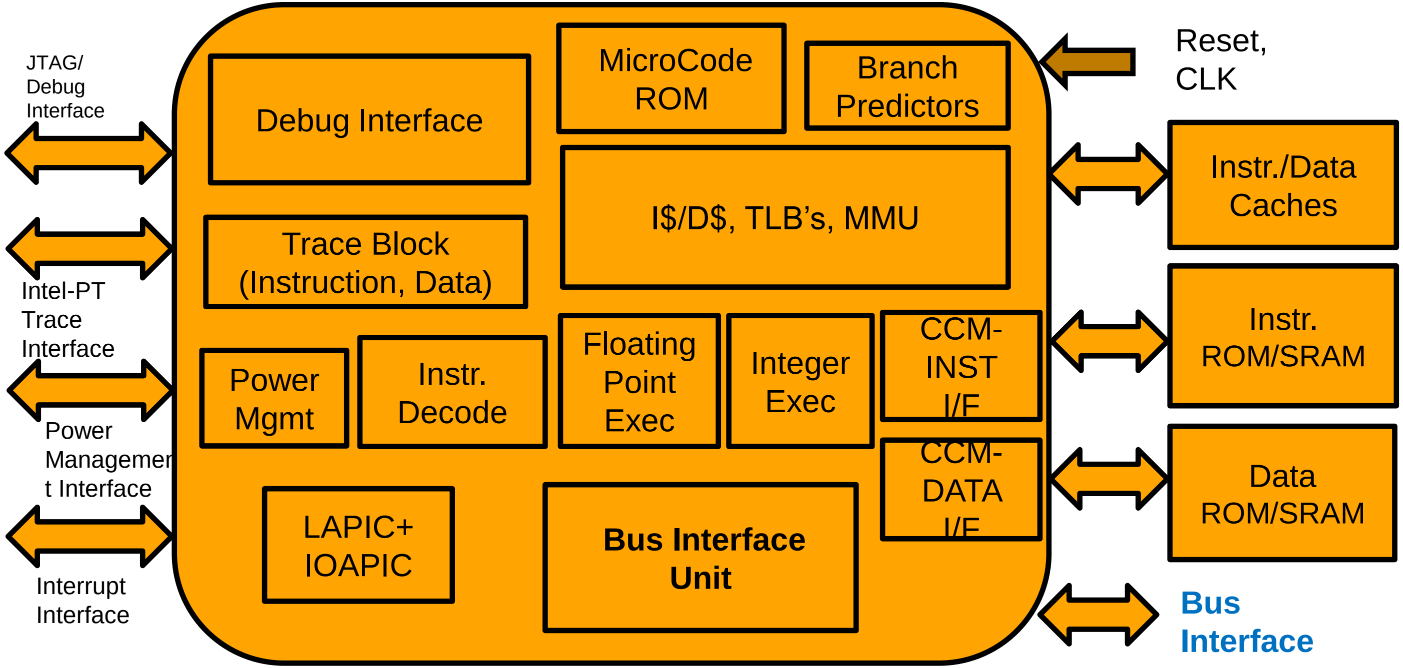
Tradeoffs

- Intel x86 ISA Compatibility
  - –Instruction set has evolved over 30years, what is the correct point.
- System level capability
  - –Tradeoff of existing software
- Performance, area and power

Configurable High Level Quark x86 CPU Block Diagram



- Quark is an in-order 5 stage IA32 CPU with Pentium ISA.
- Configurable SoftIP targeting area, power, performance and features for different applications.

Quark D2000 Core Configuration Options

Domain	Parameter Description
Arch	Pentium ISA baseline.
	PAEXD feature – disabled
	SMEP feature – disabled
	Local APIC – nested vectored controller
	IOAPIC – Vectored interrupt controller.
	No FPU
Bus Interface	AHB-Lite Fabric Interface
Target max	Frequency : 32Mhz

Domain	Parameter Description
Micro Architecture	Enable Tightly/Closely Coupled Memories(CCM)
	Instruction CCM Support
	Data CCM – 8K
	TLB Entries – 2/2
	Data Cache Disabled
Implementation	Single/Dual Ported Memories

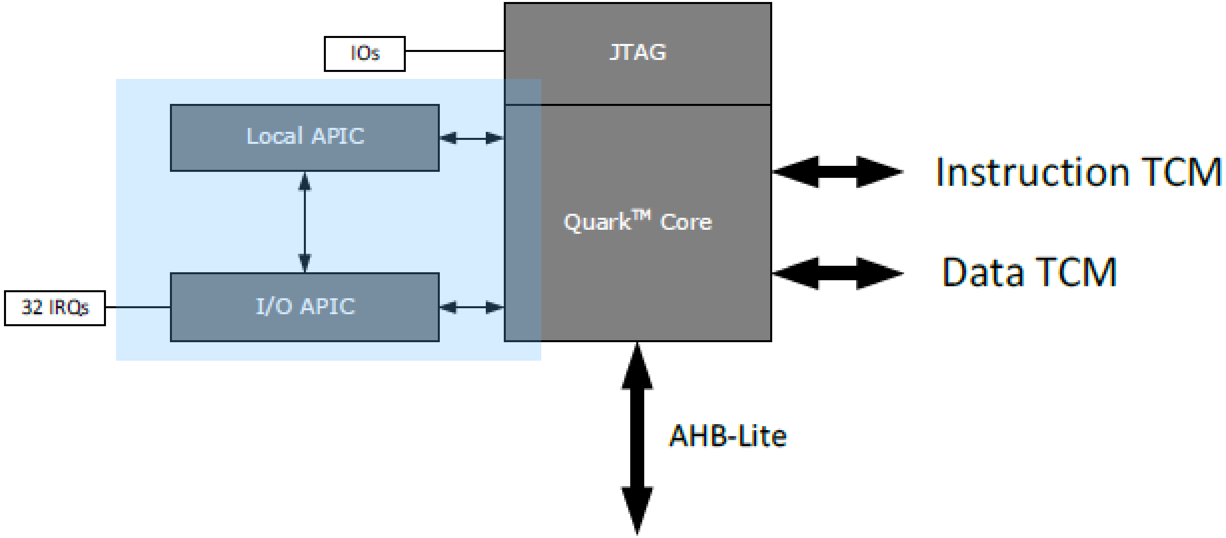
Application Instruction Set

- Retain instruction set compatibility for compiler/debugger/tool chain reuse.
- Binary compatibility lesser consideration.
- For the simplest MCU's – we chose Pentium ISA baseline.
- Drive implementation of Core to meet area/power/performance targets.

System Level ISA

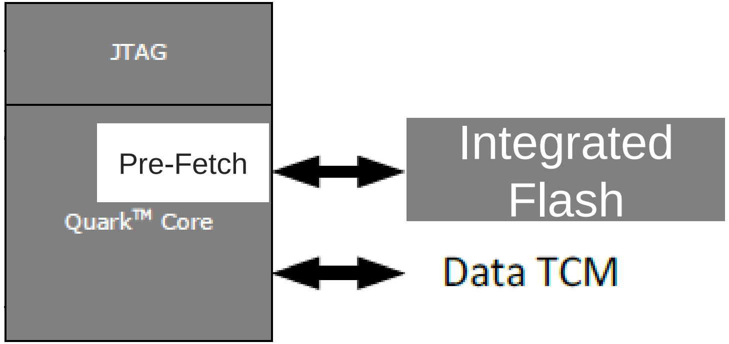
- Enumerate features using CPUID.
- Paging
  - –Retained in design for protection not translation
  - –Set TLBs to 2Instr/2Data.
- Segmentation
  - –Retained as provides memory protection.

Interrupt Routing - Latency reduction.



- Traditional – vector assignment and priority
- MCU – fixed vector assignment and priorities
- Integrated tightly into core, IDT cached

Instruction TCM Tradeoffs.



- Product Cost
- CoreMark Performance
- Core Prefetch Power performance tradeoff
- Flash Controller Sleep states
- Wait states vs core speed
- Race to halt power

Prefetcher (PRF) Sensitivity to CoreMark

+1024 iterations

Freq (MHz)	CoreMark Performance (CM/MHz)	Active Power (mW)	CM/MHz/mW	Perf Loss	Pwr Reduc	Energy (mJ)+
Prefetcher ON						
32	1.53	26.4	0.058	N/A	N/A	552.7
16	1.77	16.5	0.107	N/A	N/A	597.6
8	1.77	8.3	0.213	N/A	N/A	601.2
4	1.81	4.7	0.385	N/A	N/A	666.3
Prefetcher OFF (relative to Prefetch on)						
32	1.14	23.4	0.049	25%	11%	658.4
16	1.37	13.2	0.104	23%	20%	614.8
8	1.37	6.9	0.199	23%	17%	642.7
4	1.60	4.1	0.390	12%	13%	657.5

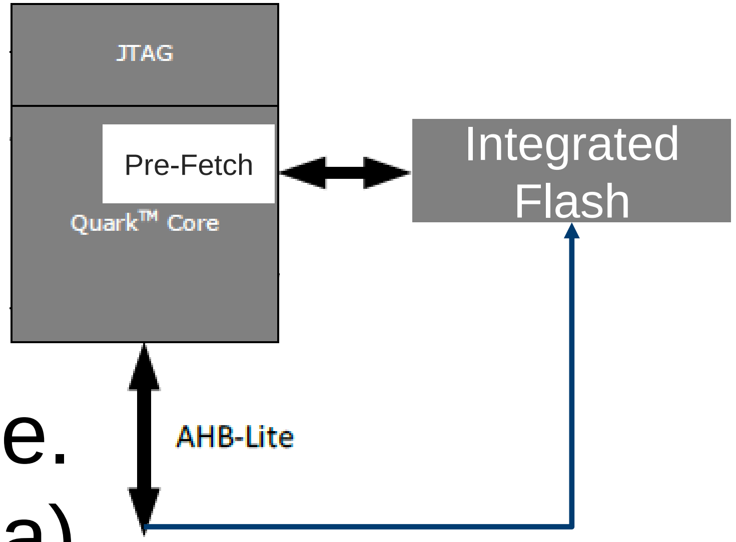
1-wait-state (16 and 8 MHz, Prefetcher ON)

1-wait-state (16 and 8 MHz, Prefetcher OFF)

Recommendation: Prefetcher ON Always – more energy efficient

Von Neumann/Harvard – Data Fetches

- Lower latency direct paths to memory
- Self modifying code
  - ITCM Flash only, no cache.
- Literal Pools (immediate data)
  - X86 Variable length instructions
  - Data fetch to ITCM routed via AHB
  - C env startup relocate data to SRAM



Core Sleep States

- Tradeoff between sleep power and exit latency.
- Clock Stopping
  - X86 Core/memory clock stop via Halt intr.
  - Wake on interrupt
- Power state – core – always on (no C6 supported)

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Power Management Efficiency.

- Power deliver efficient/mode depends on supply current.

Config	Mode	Max Current	Efficiency
1.8v Normal	Switching	50mA	90% 50mA-10mA : 70% 10mA
1.8v Low Current	Linear	300μA	99%
1.35v Retention	Linear	300μA	99%

- 30% Efficiency delta – equates to 30% battery life, when dominated by idle power.

D2000 Deep Sleep Power

SoC Power State	VR	HYB OSC	RTC OSC	CPU	CMP	ADC	Deep Sleep Current Actual (μA)
Deep Sleep RTC AONPT Wake	iLR-1.8V	OFF	ON	HALT	OFF	OFF	3.4
	iLR-1.35V	OFF	ON	HALT	OFF	OFF	2.5
Deep Sleep NoRTC Comparator Wake	iLR-1.8V	OFF	OFF	HALT	1 ON	OFF	2.2
	iLR-1.35V	OFF	OFF	HALT	1 ON	OFF	1.6
Deep Sleep NoRTC GPIO Wake	iLR-1.8V	OFF	OFF	HALT	OFF	OFF	1.9
	iLR-1.35V	OFF	OFF	HALT	OFF	OFF	1.3

Notes:

- Deep Sleep Current = PVDD Current + AVDD Current + IOVDD Current. Sum of all 3 inputs rails.

SoC Clocking

- Core Frequency Scaling (32/16/8/4Mhz)
  - Race to halt usually best, but running slower for longer better in some use cases.
  - 4Mhz Operation could fit in Low Power regulator modes max current.
  - Tradeoff of Power Islanding & Leakage.

Summary

- First iteration right ballpark in terms of performance/area/power/cost
- We Continue to
  - Continue to iterate on the micro architecture
  - Process related micro-architecture evolution
  - Analog IP evolution

Q&A

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LMT – ITCM/DTCM Pipeline Diagram

Micro-Operation	Prefetch	D1	D2	Execute	Write Back
Prefetch from ITCM	Prefetch Code from ITCM	Opcode Decode	X	RF Read ALU Operation	Register Update
Load	Prefetch Code from ITCM	Opcode Decode	Linear Address Generation	TLB Lookup DTCM Read	Register Update
Store	Prefetch Code from ITCM	Opcode Decode	Linear Address Generation	TLB Lookup DTCM write	DTCM Write
Jump	Prefetch Code from ITCM	Opcode Decode	X	Taken/Not Taken	
				Prefetch (PF) from Target Address for Tkn	D1