Samsung Exynos M1 Processor

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M1 Processor

- ISA - ARM v8.0, 64-bit/32-bit compliant.
  - AArch64 (A64), AArch32 (A32 + T32, formerly ARM+Thumb) instruction sets
- Samsung's first in house, from scratch design.
- 3-year design cycle - Reqs to Tapeout.
- Best in class, quadcore design.
- 2.6Ghz , sub 3-watt/core
- 14nm FinFet

Microarchitecture Overview

- Advanced Branch Prediction
- Quad instruction decode
  - Most instructions map directly to a single uop
- Quad uOP dispatch and retire
- Full Out-of-Order instruction execution
  - Full OoO loads and stores
- Multistride / multistream prefetcher
- Low latency / low power caches

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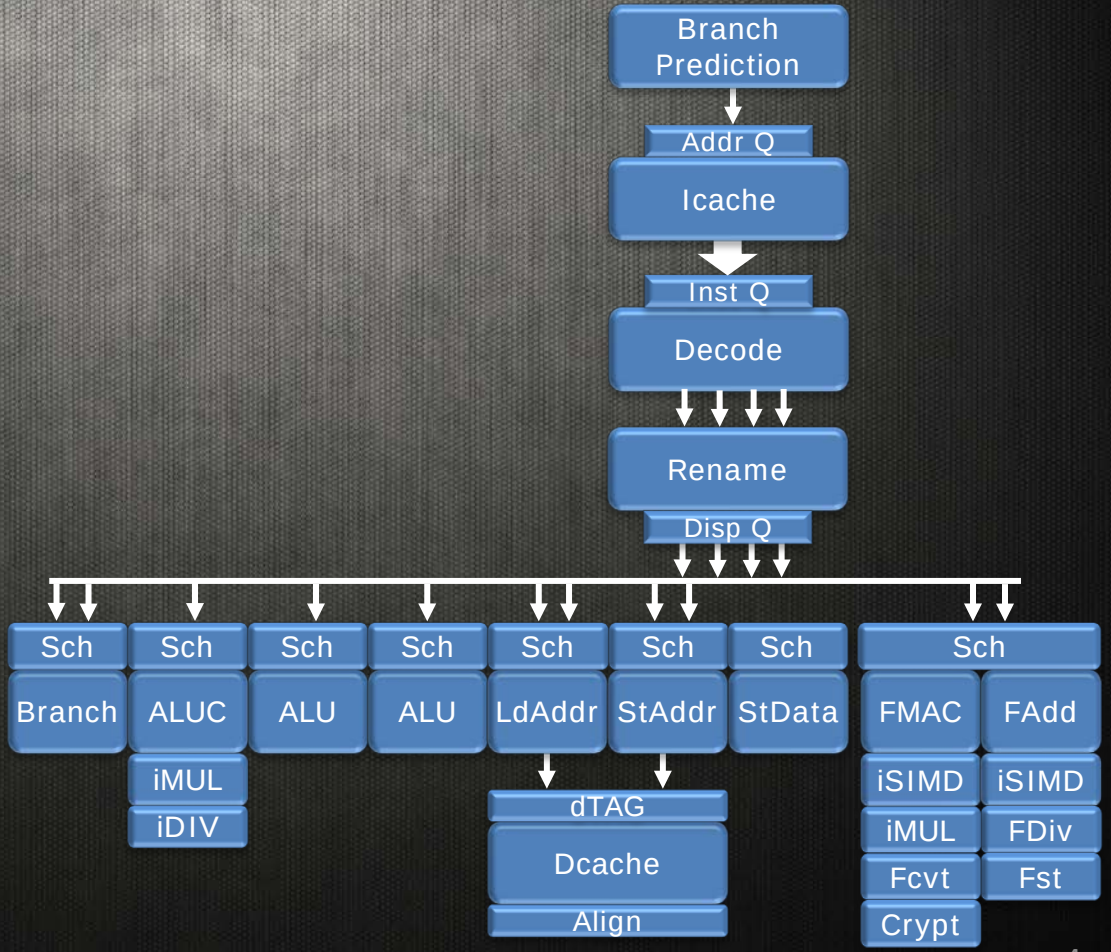
Micro-Architecture



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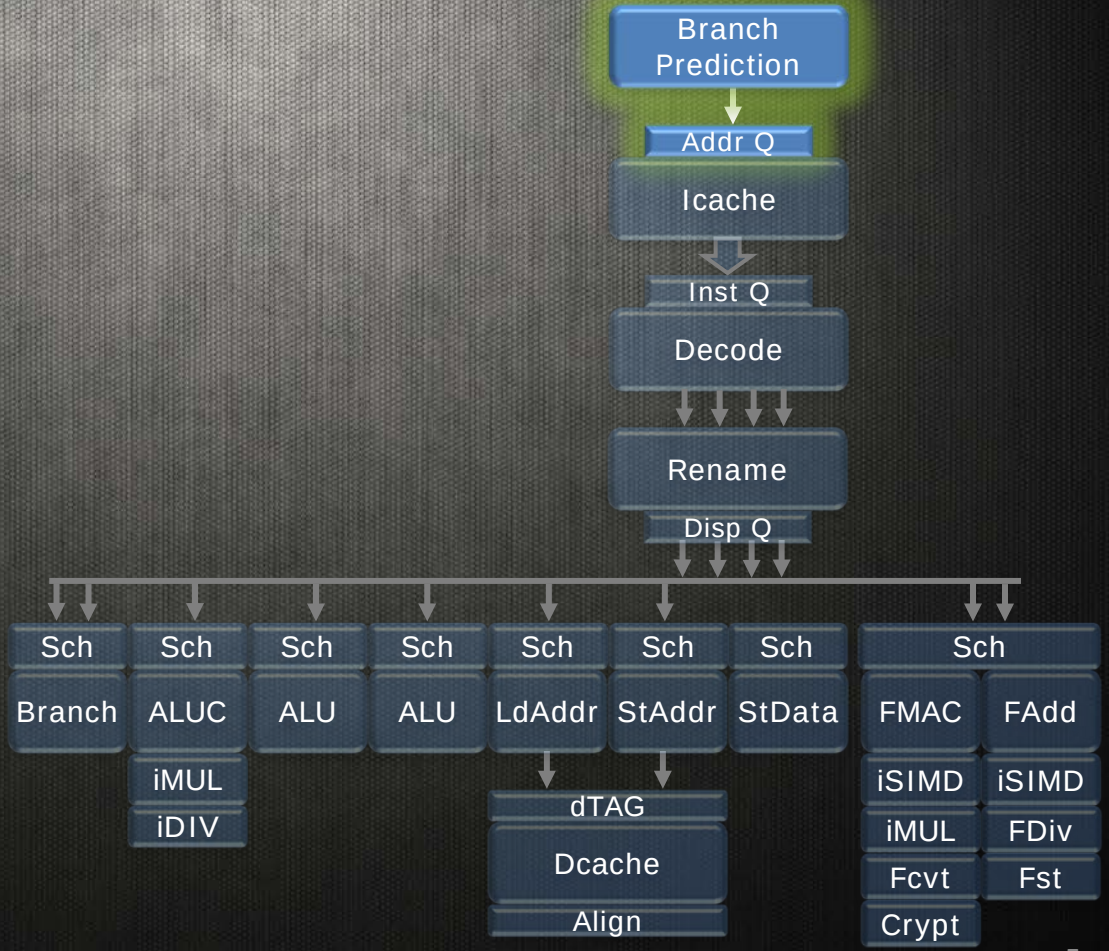
Micro-Architecture

Branch Prediction:

- Neural Net based predictor
- Two branches/cycle
- Fetch up to 24-bytes/cycle
- 64-entry microBTB
- 4k-entry mainBTB
- 64-entry Call/Return Stack
- Indirect Predictor
- Loop Predictor
- Decoupled AddrQ



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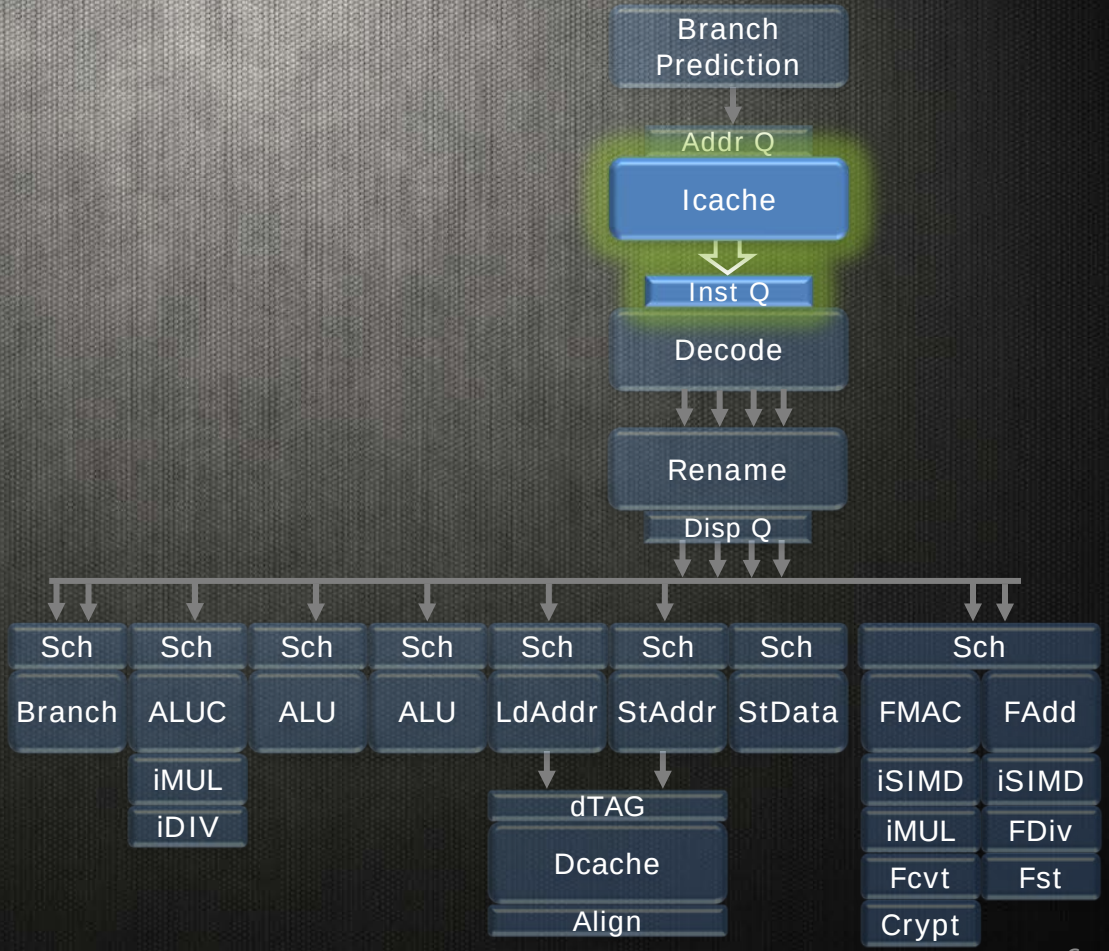
Micro-Architecture

Instruction Cache:

- 64kB/4-way
- 128-byte line size
- Read 24-bytes/cycle
- Parity Protected
- Decoupled InstQ
- 256 entry iTLB



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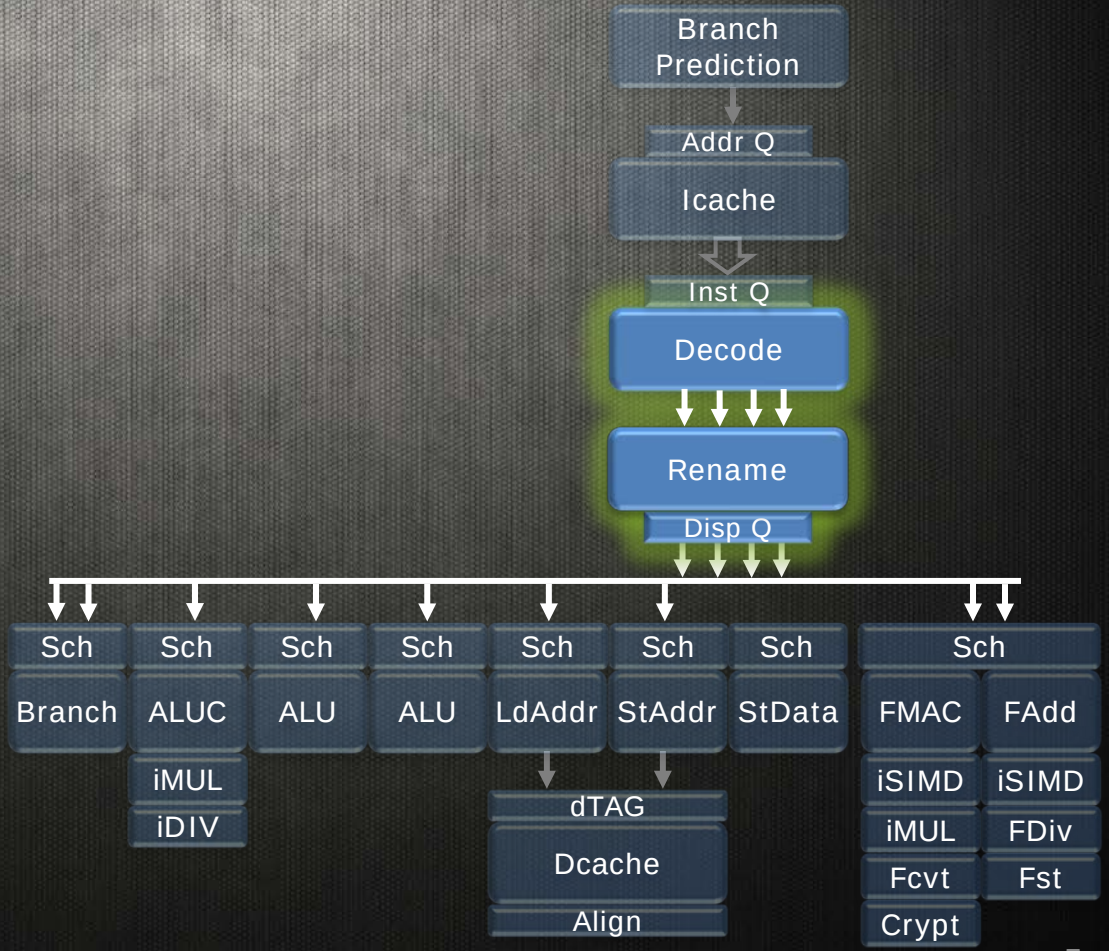
Micro-Architecture

Decode / Rename / Retire:

- Decode 4 inst/cycle
- AArch64, AArch32
- Sequencer for multi-uop
- Rename 4-uops/cycle
- Special renaming for FP
- Fast map recovery
- Retire 4-uops/cycle
- 96-entry ROB
- Dispatch 4-uops/cycle



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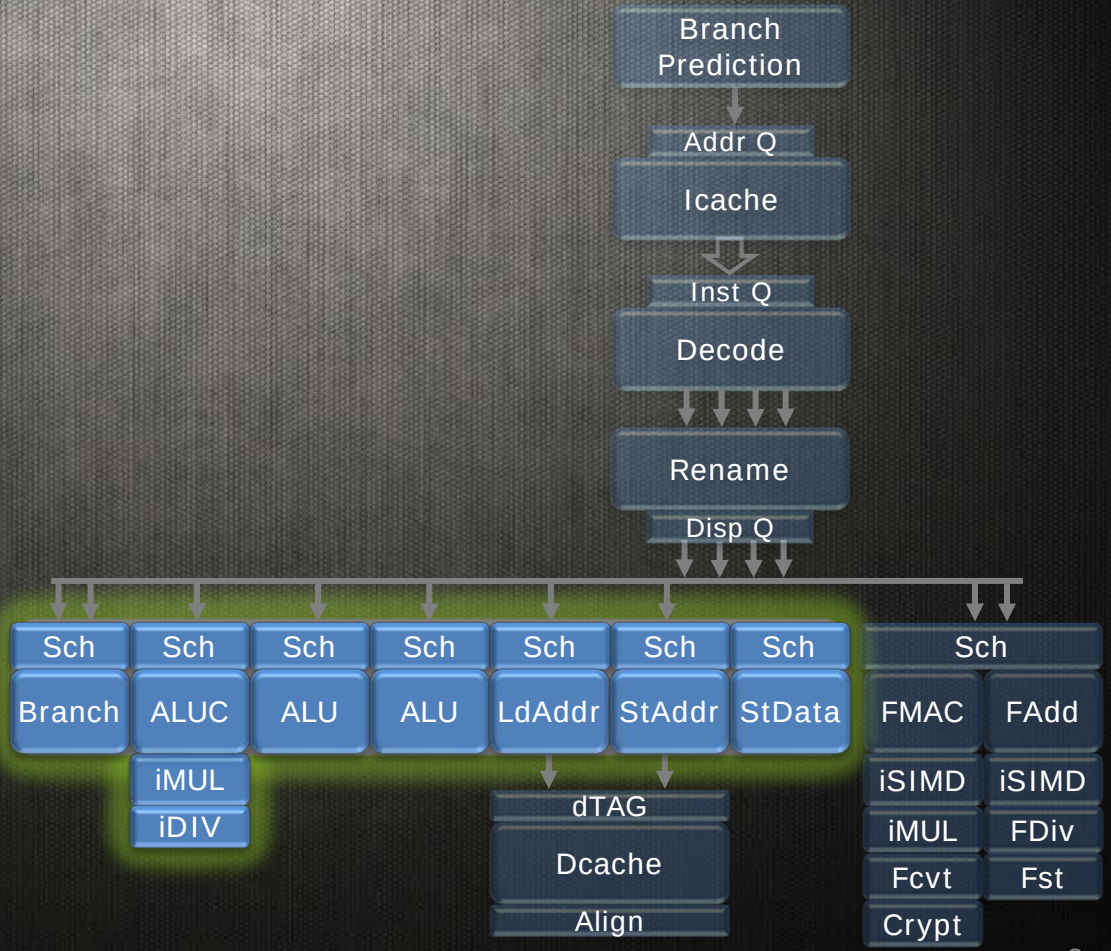
Micro-Architecture

Integer Execution:
- Issue up to 7 uops/cycle
- 96-entry integer PRF
- 58-entry distributed sched.
- Branch resolution
- ALUC – three source uops
- ALU – two source uops
- Load Address Adder
- Store Address Adder
- Store Data



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Micro-Architecture

Floating Point Execution:

- 32-entry scheduler
- 96-entry FP PRF
- FMAC : 5-cycle MAC
  4-cycle Mul
- FADD: 3-cycle

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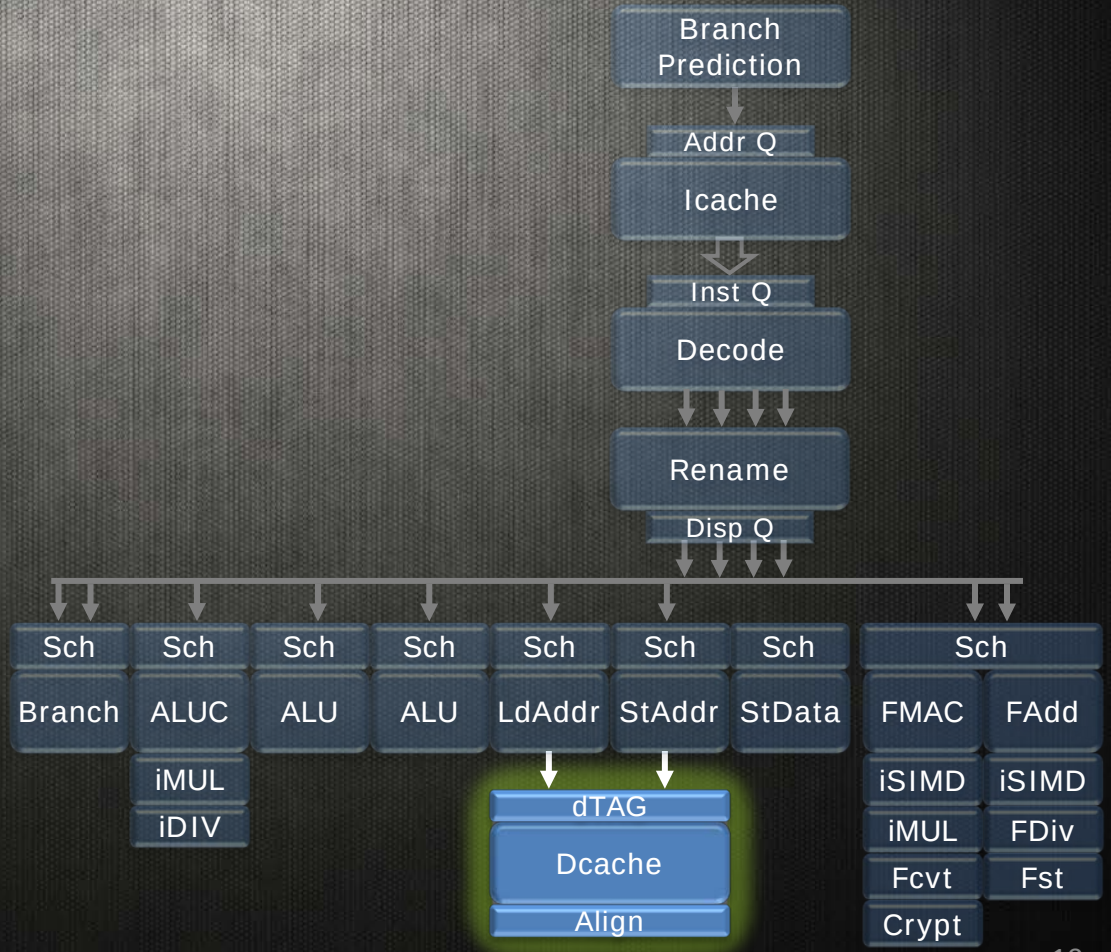
Micro-Architecture

Load/Store:
- 32kB/8-way Data Cache
- 64-byte line size
- ECC protected
- Out-of-Order loads and stores
- 1-Load/cycle, 4-cycle latency
- 1-Store/cycle
- 8-outstanding misses
- 32-entry dTLB
- 1024-entry L2TLB
- Multi-stride Prefetcher
- Stream/Copy Optimizations



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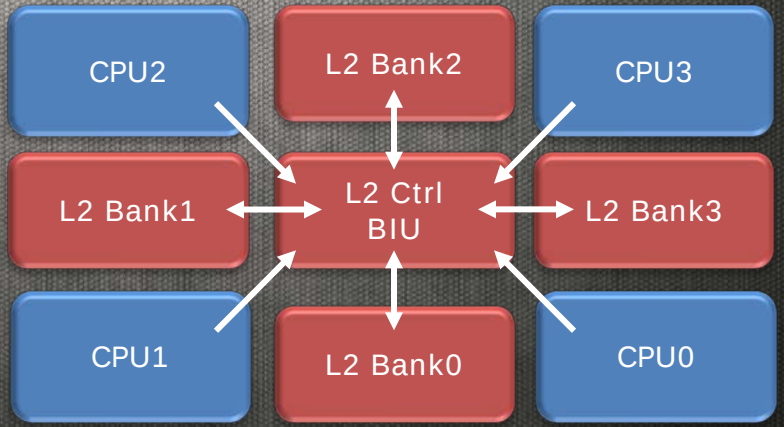
Micro-Architecture

L2/Biu:

- 2MB, 16-way
- Four banks
- Inclusive w/ filtering
- 22 Cycle latency
- 16-bytes/cycle/CPU



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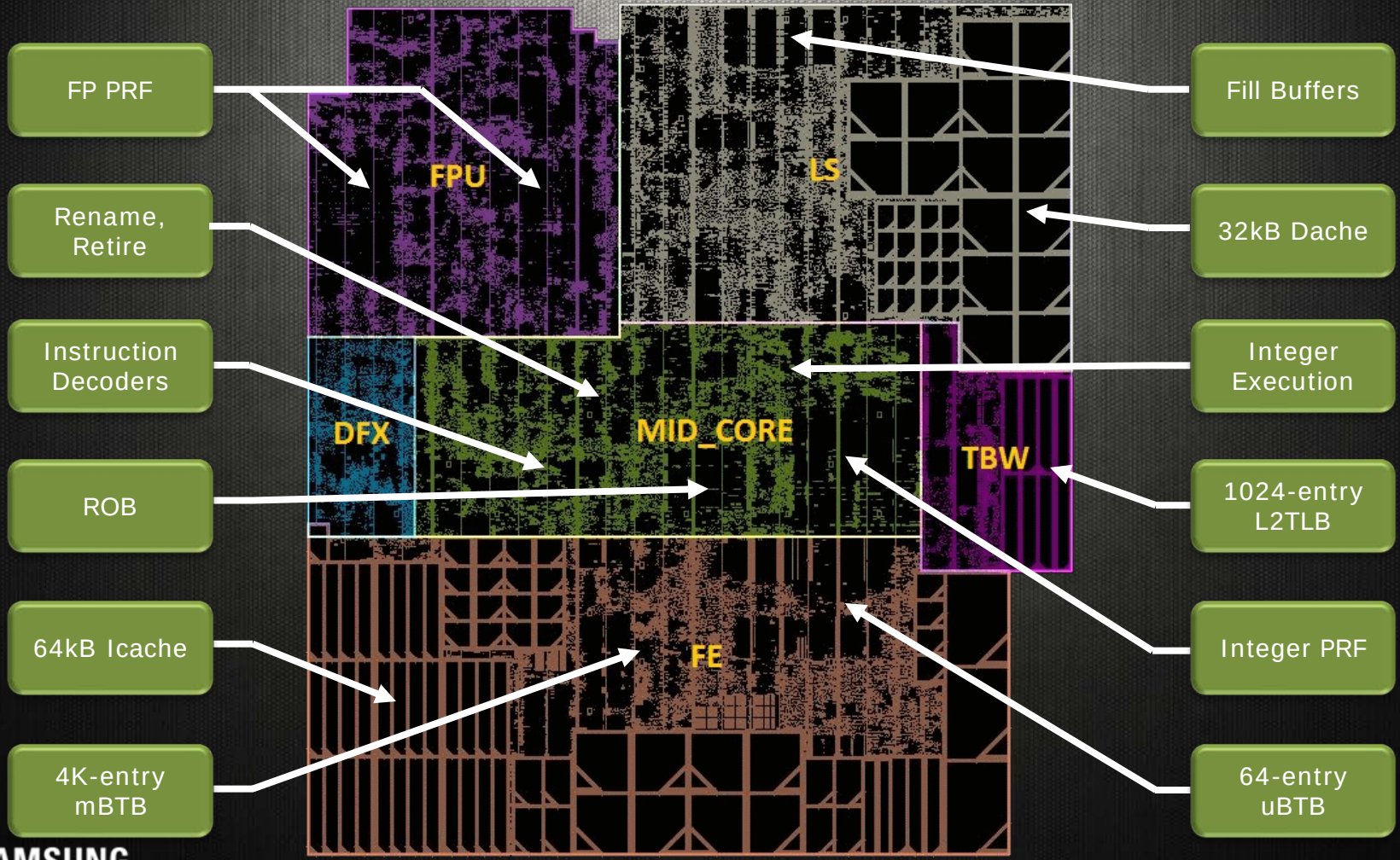
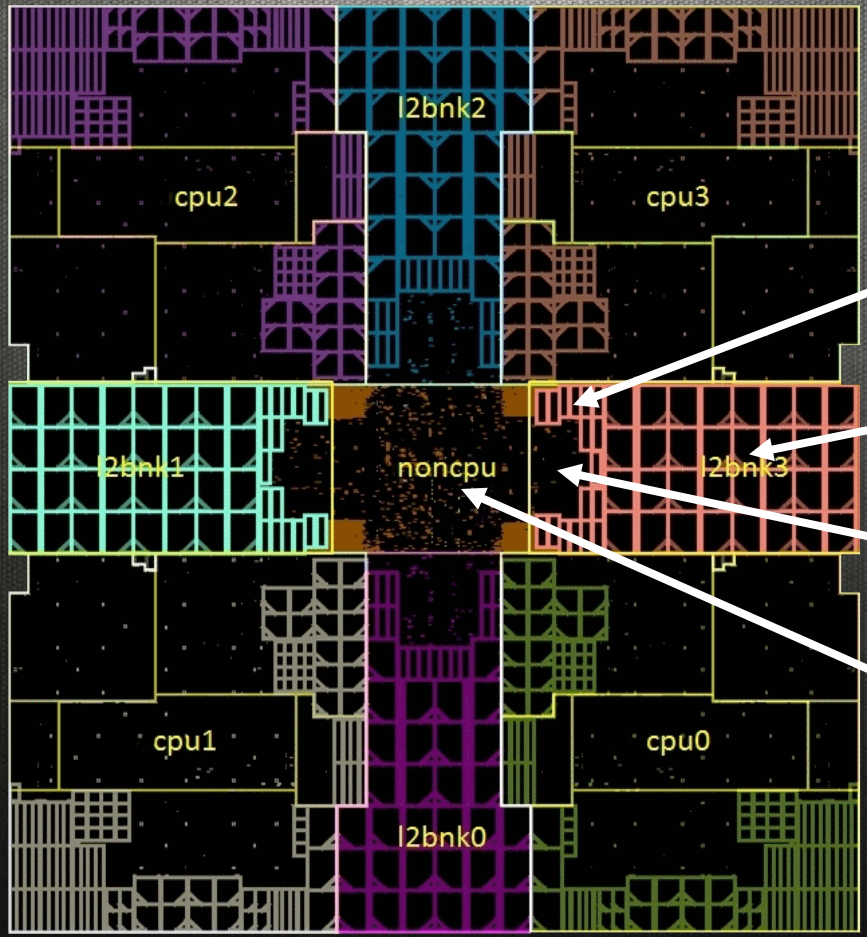
Basic Pipeline


FP PRF
Rename, Retire
Instruction Decoders
ROB
64kB Icache
4K-entry mBTB
FPU
LS
DFX
MID_CORE
TBW
FE
Fill Buffers
32kB Dache
Integer Execution
1024-entry L2TLB
Integer PRF
64-entry uBTB


l2bnk2
cpu2
cpu3
l2bnk1
noncpu
l2bnk3
cpu1
cpu0
l2bnk0
L2 Tags
L2 Data
Bank Logic
Centralized Arb/Muxing

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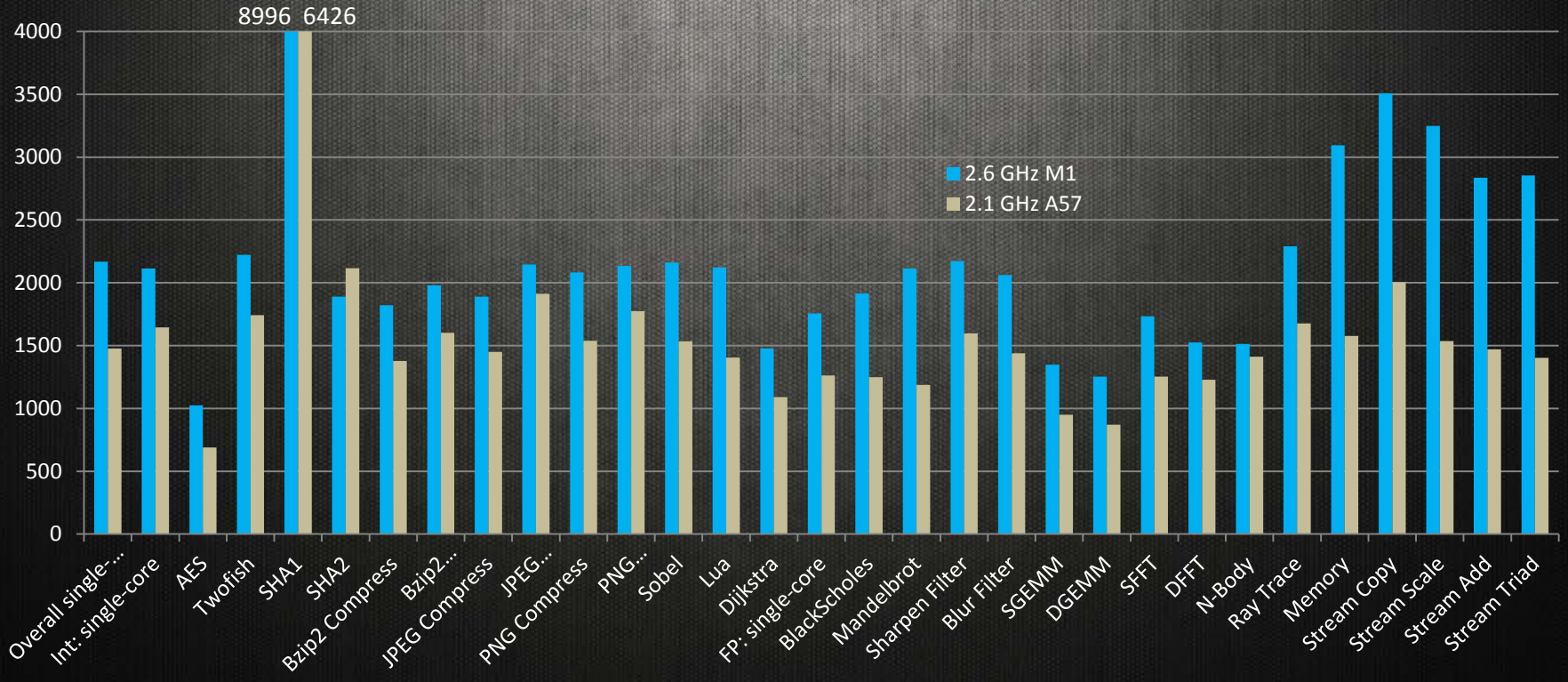
Single-core Performance



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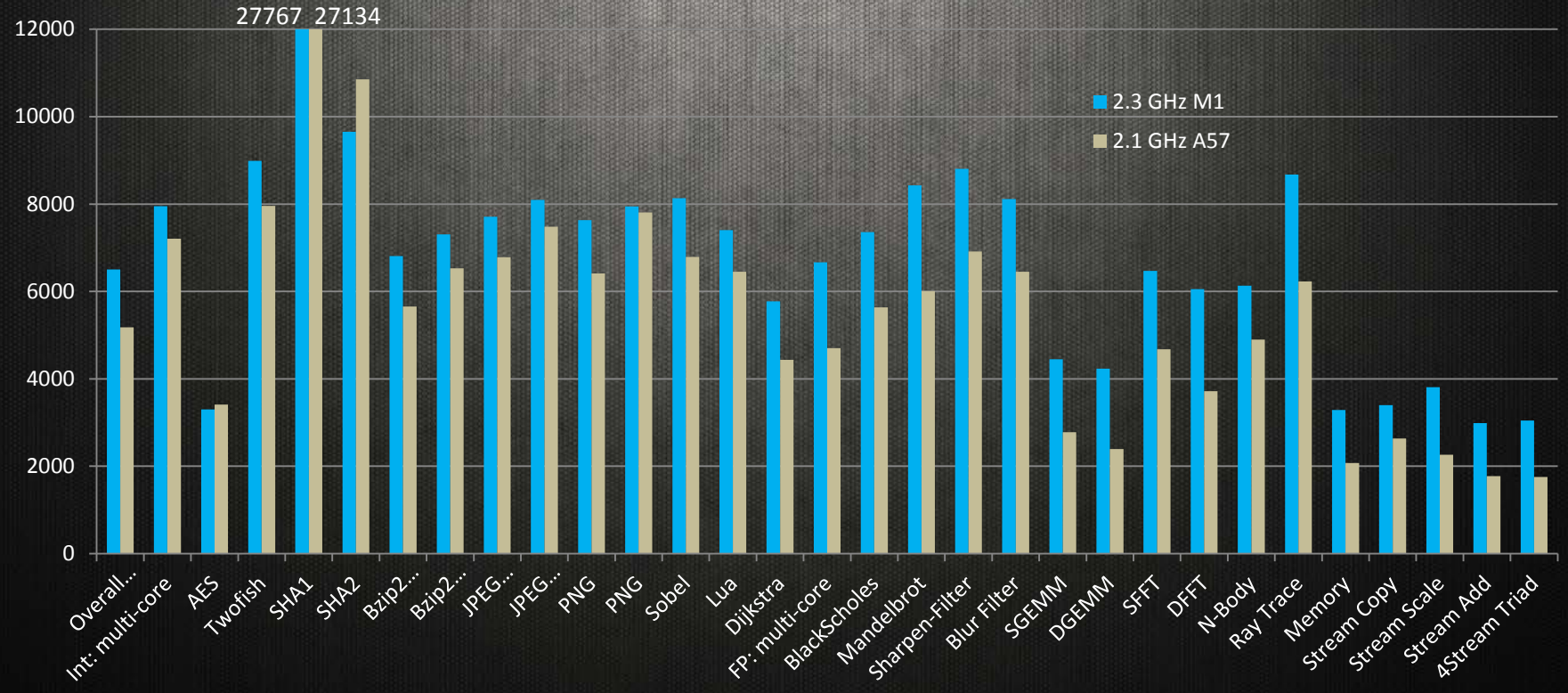
Multi-core Performance



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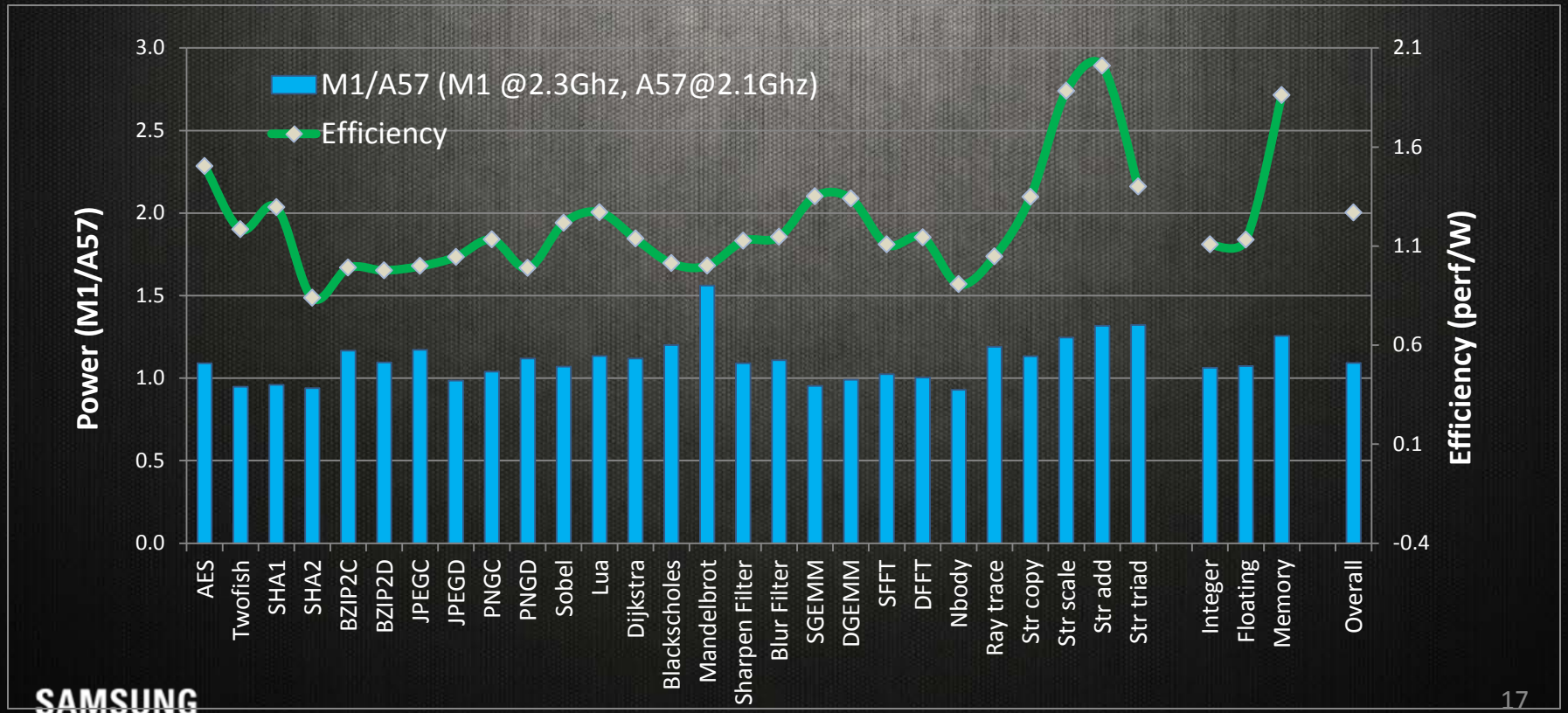
Single-core Power and Efficiency



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Conclusion

- Samsung's first from scratch CPU design
- Very aggressive, 3-year design schedule
- Cleanly into Production on time
- Performance and efficiency gains over prior generation
- Best in class quad core mobile design
- More to come…