A Perpetuum Mobile 32bit CPU on 65nm SOTB CMOS Technology with Reverse-Body-Bias Assisted Sleep Mode

Shiro Kamohara[1], Nobuyuki Sugii[1], Koichiro Ishibashi[2],
Kimiyoshi Usami[3], Hideharu Amano[4], Kazutoshi Kobayashi[5], and Cong-Kha Pham[2]

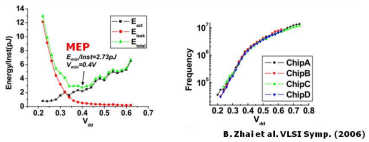
[1]Low-power Electronics Association & Project (LEAP), Tsukuba, Japan, [2]The University of Electro-Communications, Tokyo, Japan,
[3]Shibaura Institute of Technology, Tokyo, Japan, [4]Keio University, Yokohama, Japan, [5]Kyoto Institute of Technology, Kyoto, Japan

What is MEP (Minimum Energy Point) operation?

Any transistor should work under the condition; "lowest energy per operation"

Power: $P = CV_{dd}^2 f + I_{leak} V_{dd}$ (active / leakage)

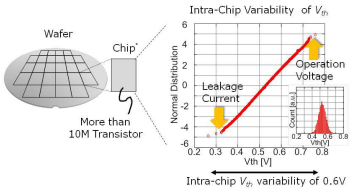
Energy per operation: $E = CV_{dd}^2 + I_{leak} V_{dd} / af$ (a: activity)



B. Zhai et al. VLSI Symp. (2006)

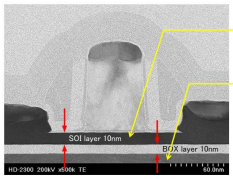
Big wall for MEP operation: Variability

Large Vth variability caused by RDF deteriorate the trade-off between V_{min} and standby leakage.



SOTB (Silicon On Thin Buried Oxide)

SOTB drastically relax the trade-off between V_{min} and the standby leakage by two mechanism.

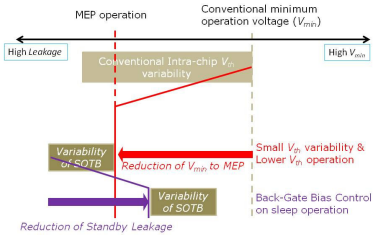


(1) Dopant-less Channel
Minimize V_{th} variability by suppressing RDF.

(2) Bake baias control
Minimize standby leakage by heightening V_{th} when sleep mode operation.

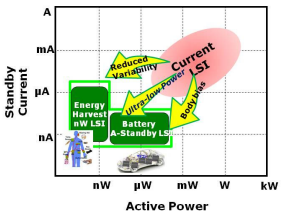
RDF: Random dopant fluctuation

Mechanism of MEP operation via SOTB

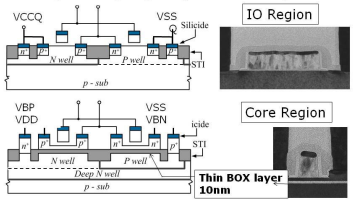


Target of SOTB to realize IoT world

Our goal is the 1/10 X reduction of an active power and the standby current to realize IoT world.



65nm process platform for ultra-low power

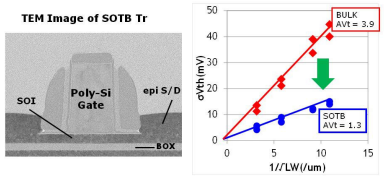


IO Region (Bulk)	3.3V device, Lg=400nm, T_{SON}=7.5nm, Twin Well
Core Region (SOTB)	1.2V device Lg=60nm, T_{SON}=2.0nm, T_{BOX}=10nm, Triple Well VTP/VTN (VBB=0) = 0.20V/0.19V(Logic), 0.24V/0.22V(Memory)
Metal layers	7 metal (5 fine, 2 Semi global), 1 AL

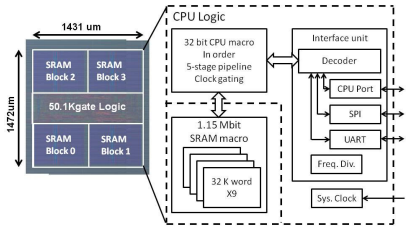
Extreme low V_{th} variability by SOTB

Our 65nm SOTB core transistor shows the ectreme variability reduction of 1/3 in comparison with conventional one.

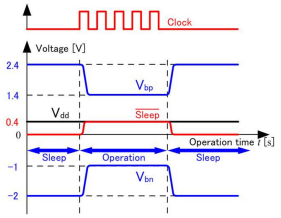
TEM Image of SOTB Tr



CPU Chip Photomicrograph and Structure

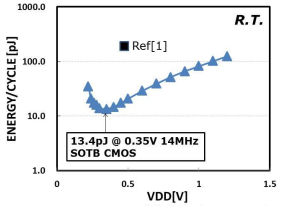


Control method of CPU test chip



Energy per Cycle Value of CPU

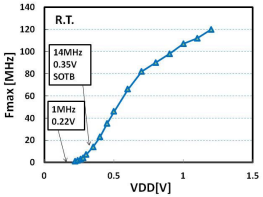
SOTB enable our test chip of a MEP operation of 0.35V and 13.4pJ .



[1] Shailendra Jain et. al., ISSCC 2012.

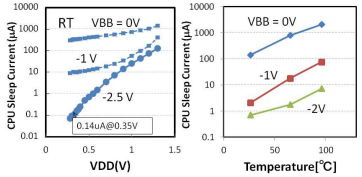
Maximum Operating Frequency of CPU

Even for a MEP operation, our test chip show F_{max} of 14MHz and V_{min} is 0.22V.



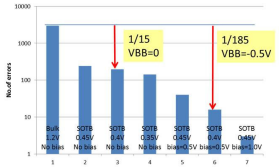
CPU Sleep Current

Back bias control the standby leakage of more than 3 order and it makes the system a free for thermal running.



Reliability benefit for SOTB

Soft error immunity of FF for SOTB are less than 1FIT, while those for Bulk are more than 100FIT.



CONCLUSIONS

- **Perpetuum computing 32bit CPU is demonstrated with 65nm SOTB and back bias technology.**
- **13.4 pJ/cycle operating minimum energy, 0.14μA sleep current is attained.**
- **The CPU operates eternally with ambient light indoor.**

Acknowledgments

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