Low Power Fixed-Latency DSP Accelerator with Autonomous Minimum Energy Tracking (AMET)

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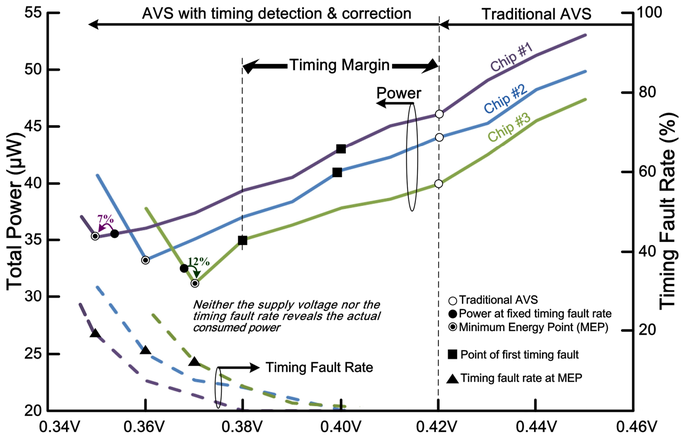
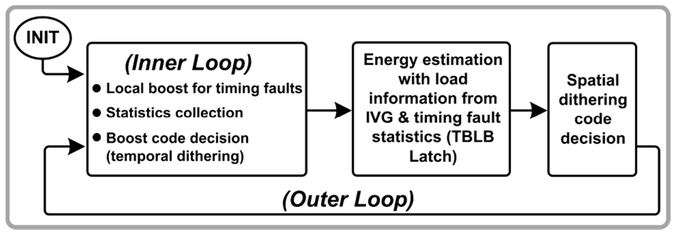
Autonomous Minimum Energy Tracking (AMET)





Traditional Adaptive Voltage Scaling (AVS)

- No timing fault allowed
- Voltage guardband required to guarantee correctness
- Limited power reduction

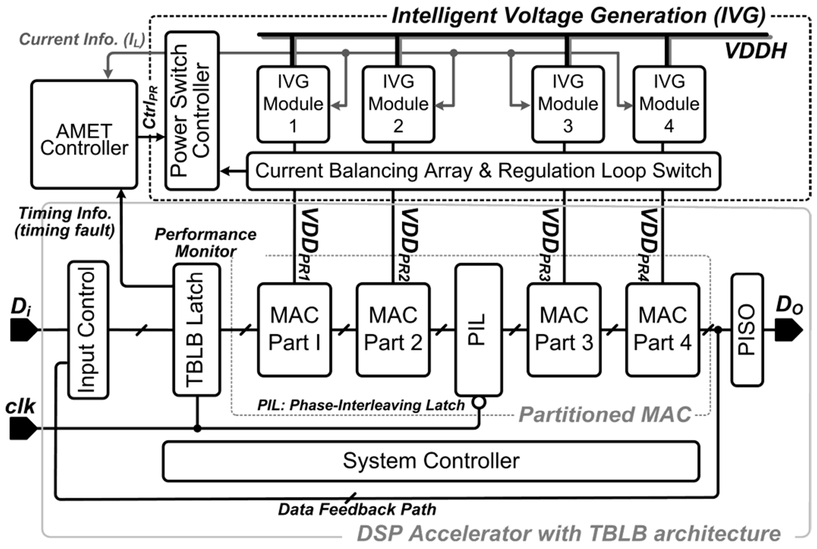
Razor-based AVS [1-4]

- Voltage over-scaling (VOS) w/ timing fault detection & correction)
- Performance penalty w/ stall cycles or architectural replay
- Non-trivial to find minimum energy point (MEP)

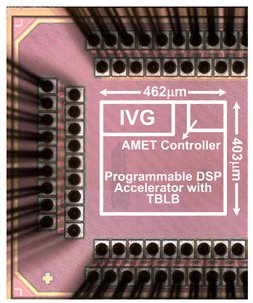
Proposed AMET loop

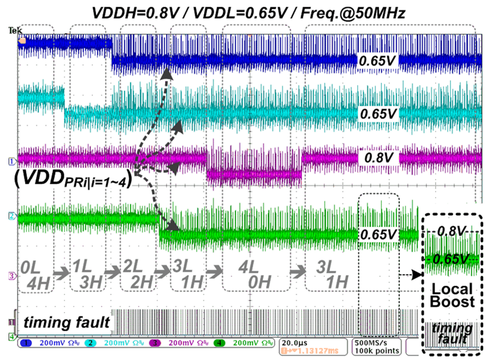
- Intelligent VOS w/ spatial & temporal voltage dithering
- Spatial voltage dithering: Explores optimal voltage combination
- Temporal voltage dithering: Timing rescue with local boost
- Fixed latency w/ time borrowing and local boost (TBLB) [5]
- Short path problem associated with the original TBLB is solved by the phase-interleaving latch (PIL)
- Autonomous MEP tracking w/ intelligent voltage generation (IVG)

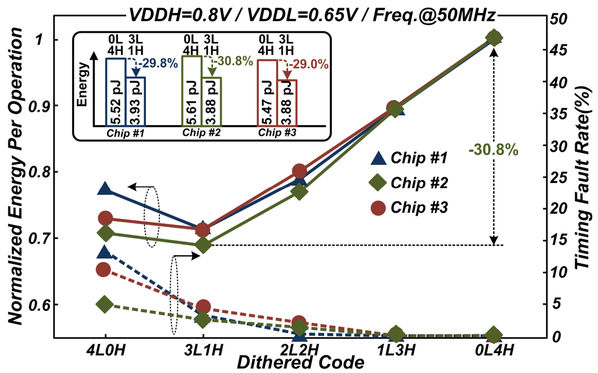
Fixed-latency DSP Accelerator with AMET



Chip Implementation







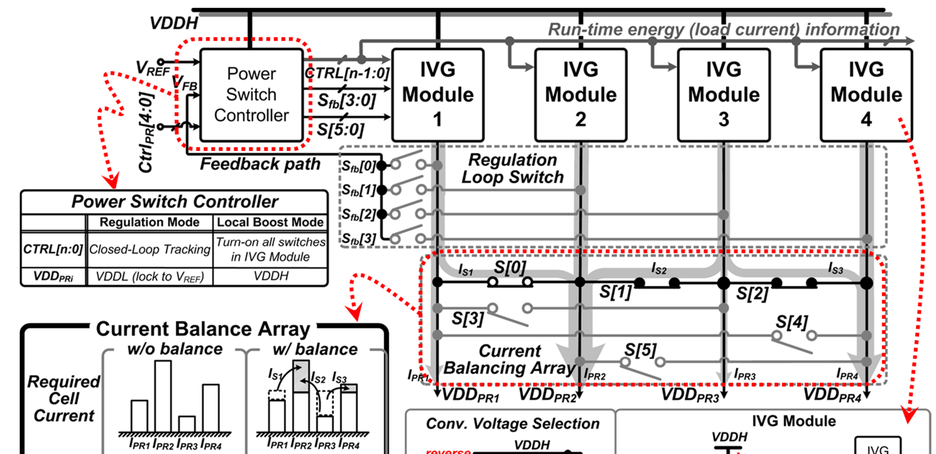
- TSMC 65nm LP
- Core size: 0.186mm^2
- Frequency: 50MHz
- VDDH = 0.8V,
  Regulated VDDL = 0.65V

Average energy

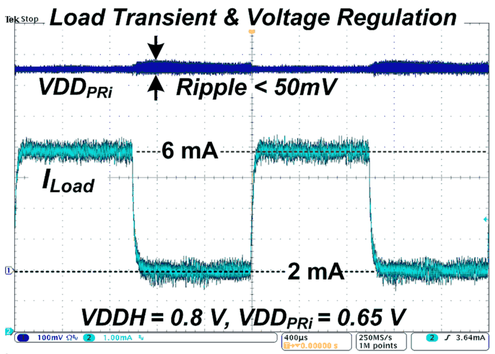
- 0L4H mode: 5.53pJ
- 3L1H mode: 3.89pJ

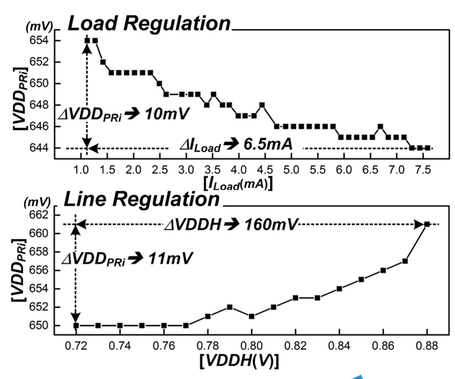
29.8%, 30.8%, and 29.0% energy savings were achieved for 3 measured chips

Intelligent Voltage Generation (IVG)



- Single-controller multiple-output
- Reverse-current-free
- IVG module: As a digitally controlled resistor to provide external VDDH or regulated VDDL
- Current balancing array: Redistribute load current to more demanding DSP accelerator partitions





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