



Myriad 2: "Eye of the Computational Vision Storm"

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Movidius Update Since Hot Chips 2011

 Mobile Vision Processor company opening the era of computational cameras:







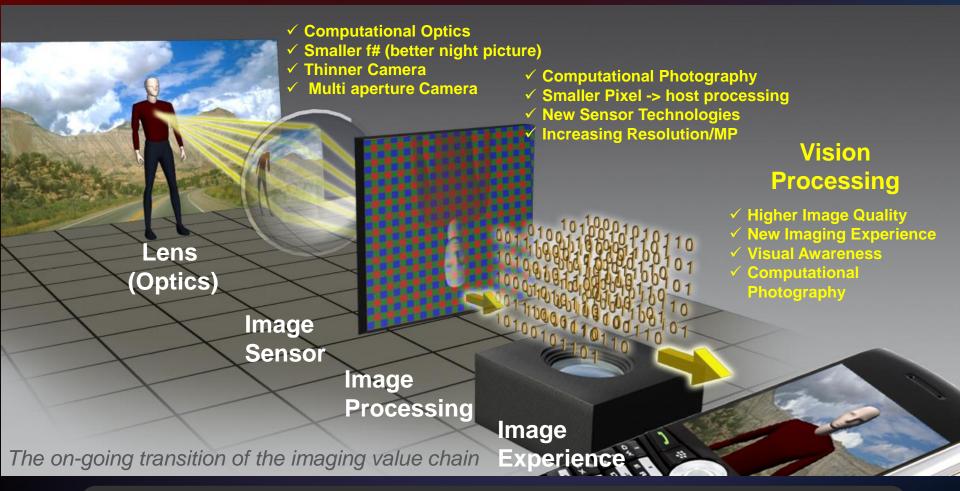
SLR performance Brand new UXP in mobile devices for mobile devices

Brand new product categories

- 8+ years of heritage. Close to \$60M invested into technology development
- Proven architecture. 100% internally developed. Strong IP position
- February 2014 announcement: Google partnership with Myriad 1
- July 30, 2014 announcement: Myriad 2 Vision Processor SOC
- Headquartered in San Mateo, CA with design centers in Dublin, Ireland and Timisoara, Romania. Currently employing 70 staff including 65 engineers (10% hardware, 90% software/system)



Disruptive Imaging Evolution From <u>Digital</u> Imaging to <u>Computational</u> Imaging



Why Digital \rightarrow Computational Imaging ?

the only way to overcome physical, mechanical and computational limitations of today's mobile cameras

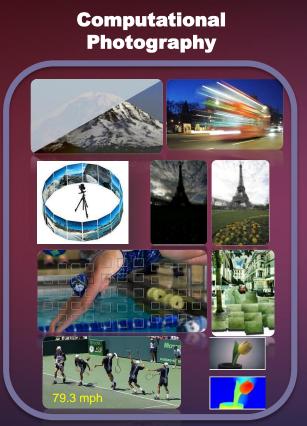


Why are Computational Cameras a Game Changer ? Highway to the next generation user experiences Visual

Visual Awareness



The old paradigm



"Optical" zoom, Depth, HDR, Ultra-fast AutoFocus, Panorama, 360º capture, Extreme low light

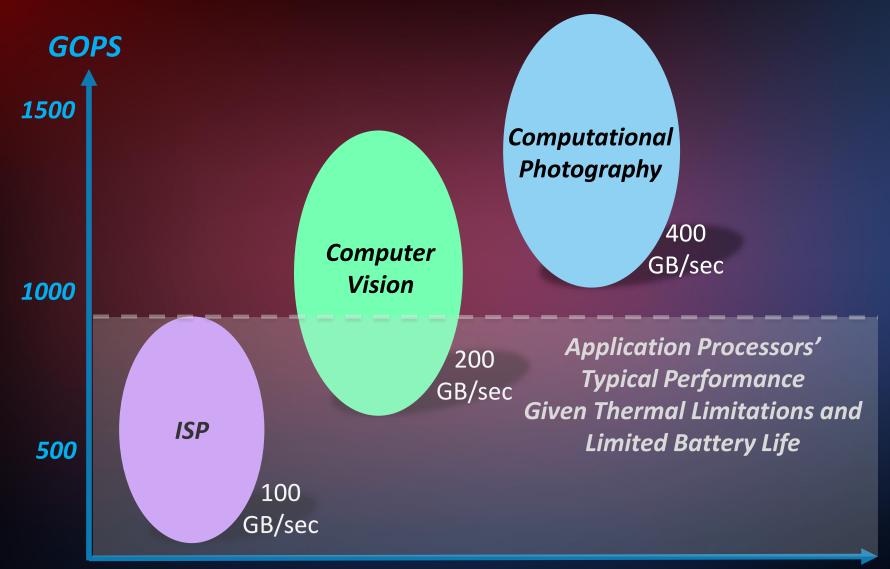


3D Modeling, 3D Scanning, Visual Search, Indoor navigation, Augmented reality, Object detection, Object recognition...

Vision Processing: the new imaging paradigm



Need for Special Purpose Vision Processor



Computational Complexity

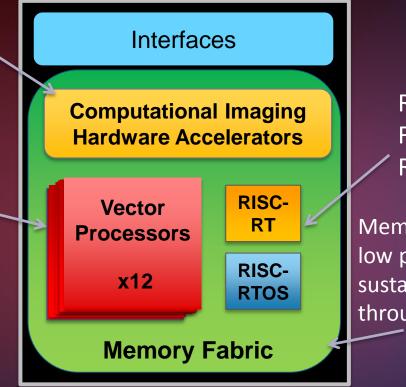


Source: Movidius

Introducing the Myriad 2 Vision Processor SOC

Optimized **configurable** imaging and vision hardware engines (framework)

Vector VLIW processors designed to crunch complex vision and imaging algorithms at high performance and low power



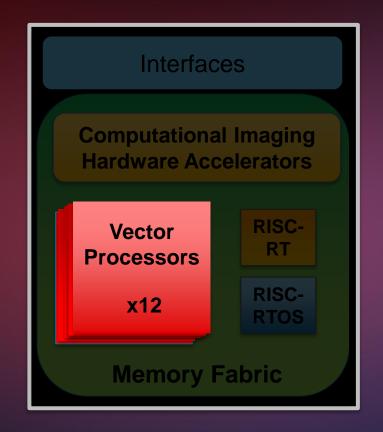
RISCs run RTOS, Firmware, RunTime Scheduler...

Memory designed for low power, zero latency, sustained high performance through **data locality**

Nominal 600 Mpixels/sec throughput enables connection to multiple cameras, world-class computational imaging pipelines, and complex vision applications

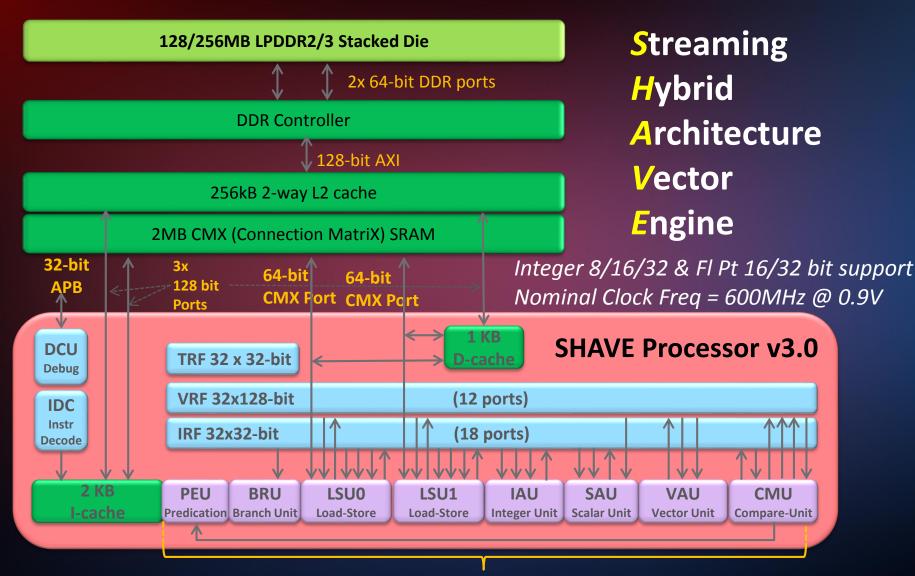


(1) Specialized Vector VLIW Processors for Vision





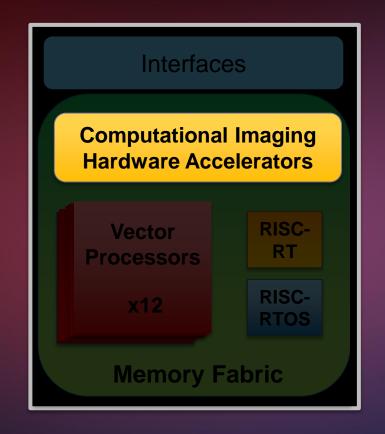
SHAVE 128 bit SIMD-VLIW Vector Processors



8 parallel SHAVE VLIW Functional Units Supplied with VRF & IRF Data 128-bit Instruction-Fetch (Variable-Length Instructions max 192 bits)



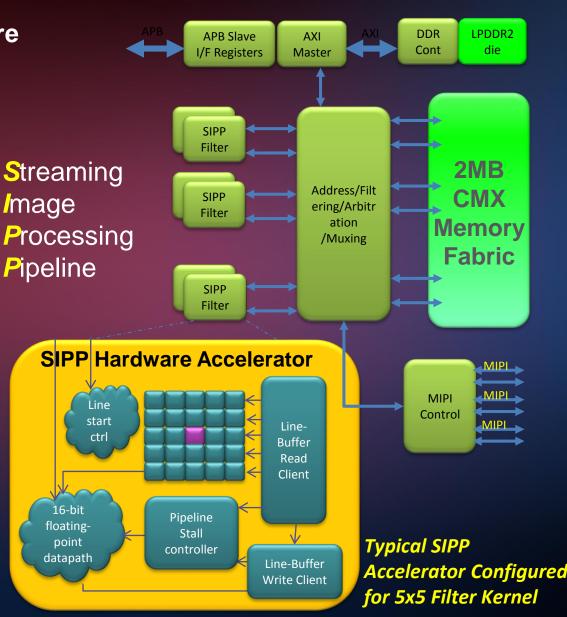
(2) Imaging Hardware Accelerators





SIPP Computational Imaging Hardware Accelerators

- 20+ programmable hardware accelerators including:
 - Poly-phase resizer
 - Lens shading correction
 - Harris Corner detector
 - HoG/Edge operator
 - Convolution filter
 - Sharpening filter
 - $-\gamma$ correction
 - tone-mapping
 - Luma/Chroma Denoise
 - ..and others
- Each accelerator has
 - Memory ports
 - Local decoupling buffers
 - Ability to fully compute 1 operation per pixel per cycle



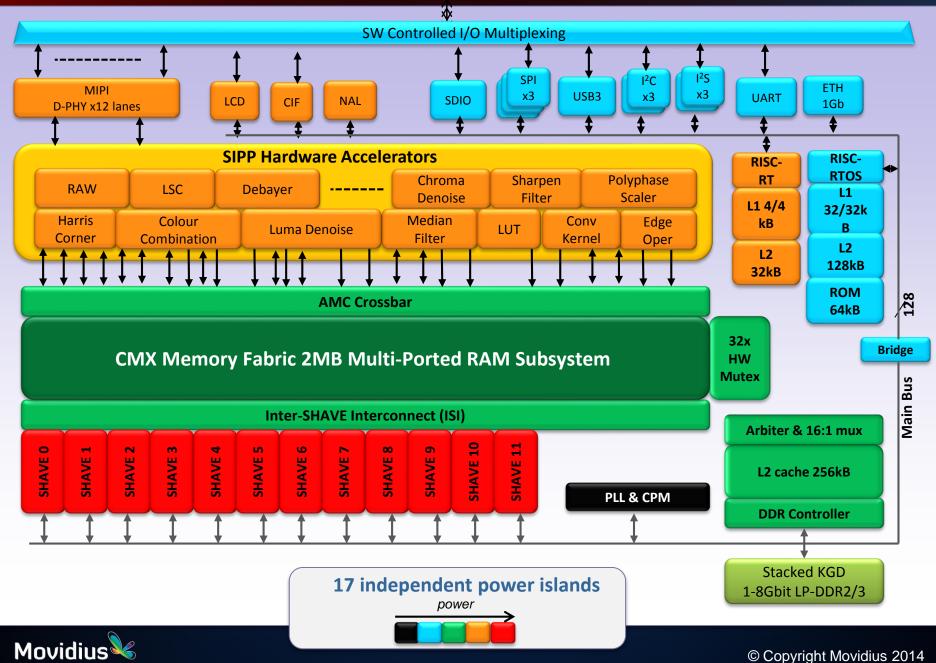


SIPP Hardware Accelerators Details

- Myriad 2 achieves 20-30x performance of Myriad 1
 - SHAVE performance compared to Myriad 1 roughly: (600 MHz / 180 MHz) * (12/8) = 5x
 - SIPP Hardware Accelerators in Myriad 2 can output one fully computed output pixel per cycle
 - Comparison with SHAVE-only software filters on Myriad 1 which range from 1.5 up to dozens of cycles per pixel
 - 15-25x additional performance compared to Myriad1
- Hardware accelerator rationale fits with Moore's law trend below 28nm
 - Memory access is expensive in terms of power
 - Memory scaling 20-30% vs 50% for logic
 - This means we can trade arithmetic OPS for less memory occupancy and lower power



Myriad 2 Detailed System Diagram



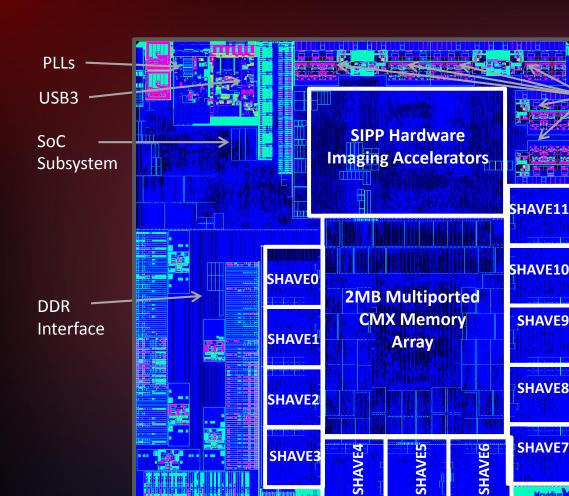
Myriad 2 Die



0.35mm pitch **WLCSP**

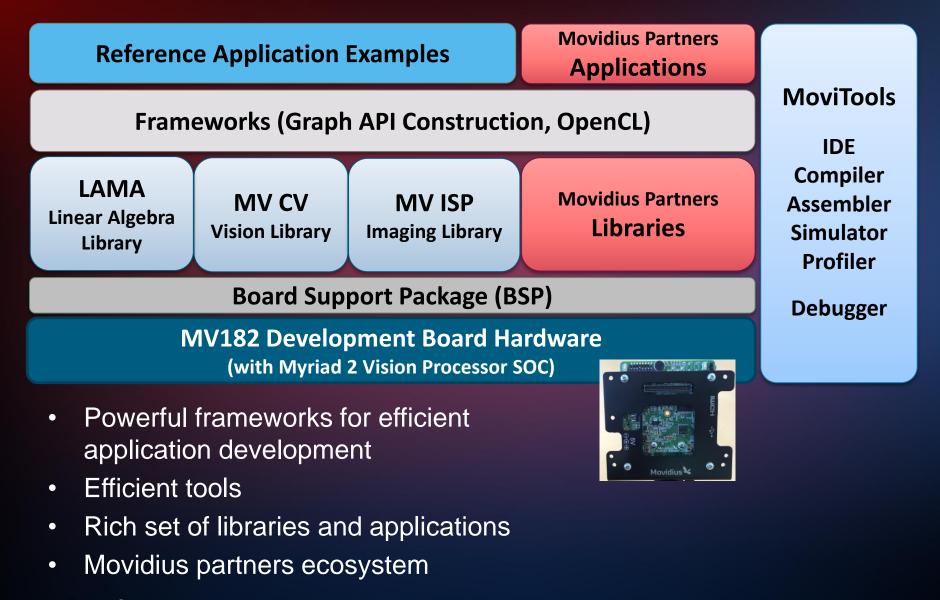


Movidi





Myriad 2 Software Development Kit (MDK)





Myriad 2 Power Efficiency: Depth Extraction

- Depth extraction using structured light
 - Projector emits structured light pattern
 - Aligned camera captures reflected structured light pattern
 - Significant computation required to extract depth
- Achieves 30 fps < 250 mW full package power
- Resources used on Myriad 2:
 - 6 x SHAVE vector VLIW processors
 - 2 x SIPP hardware accelerators
 - Mix of 16b floating-point intermediates and 32b floating-point final output



Hard Real-time Support for Low Latency Computer Vision

- Essential for line sync based super low latency processing
- Deterministic data access due to 2MB on-chip SRAM
 And dedicated stacked DDR (no contention with GPU etc.)
- Low latency (<2µsec worst case) interrupt handling
 - No contention with peripherals such as USB, SPI etc.
- 64 bit timestamp support

| Algorithm Example | Details |
|--------------------------------|---|
| Haar Cascade classification | OpenCV compatible multi-scale Haar Cascade with 20 stages, computed using 12 x SHAVEs and 1 x SIPP accelerator. |
| | Latency: For each 1080p resolution frame, calculates 50,000 multi-scale classifications in <7 msec |



Conclusions

- We're entering a new era of computational imaging
- Myriad 2: An advanced 28nm self-contained Vision Processor SOC
 - Aggregate nominal 600 Mpixel/sec throughput for complete pipeline(s)
 - Sustained performance from a highly innovative multicore memory subsystem (400GB/sec BW)
 - Low-latency for demanding vision applications by allowing flexible memory allocation lines, tiles etc. not just frames
 - 20-30x more performance per Watt compared to Myriad 1

• Myriad 2 Software Development

- Powerful frameworks for efficient application development
- Efficient tools
- Rich set of libraries and applications
- Movidius partners ecosystem







Thank you!

Q&A

