THE AMD OPTERON™ A1100 PROCESSOR CODENAMED "SEATTLE"

SEAN WHITE

11 AUGUST 2014

“SEATTLE” – WHAT IS IT AND WHY?

AMD

- What is it?
  - “Seattle” is AMD’s first 64-bit ARM-based processor
    - 8 ARM Cortex™-A57 cores
    - 2 DDR3/4 DRAM channels
    - 10G Ethernet, PCI-Express, SATA
    - GlobalFoundries 28nm process

- Why did AMD build it?
  - “Seattle” is a dense server processor for datacenter applications
    - Performance/dollar/watt drives today’s datacenter designs
    - A significant number of datacenter workloads have inherently low Instructions Per Clock (IPC) and high cache miss rates
    - For such workloads, processors like “Seattle,” with smaller cores and caches, can deliver the equivalent performance as traditional server processors with large cores and caches, but using much less power and area
  - The 32-bit to 64-bit transition for the ARM architecture is a major shift in the industry, like the 32-bit to 64-bit transition in x86 was
    - AMD is taking a leadership role in the 64-bit ARM space, as it did in the 64-bit x86 space

“SEATTLE” SOC OVERVIEW

Power Efficient Cores
- Up to Eight ARM Cortex-A57 cores
- Up to 4MB shared L2 cache total

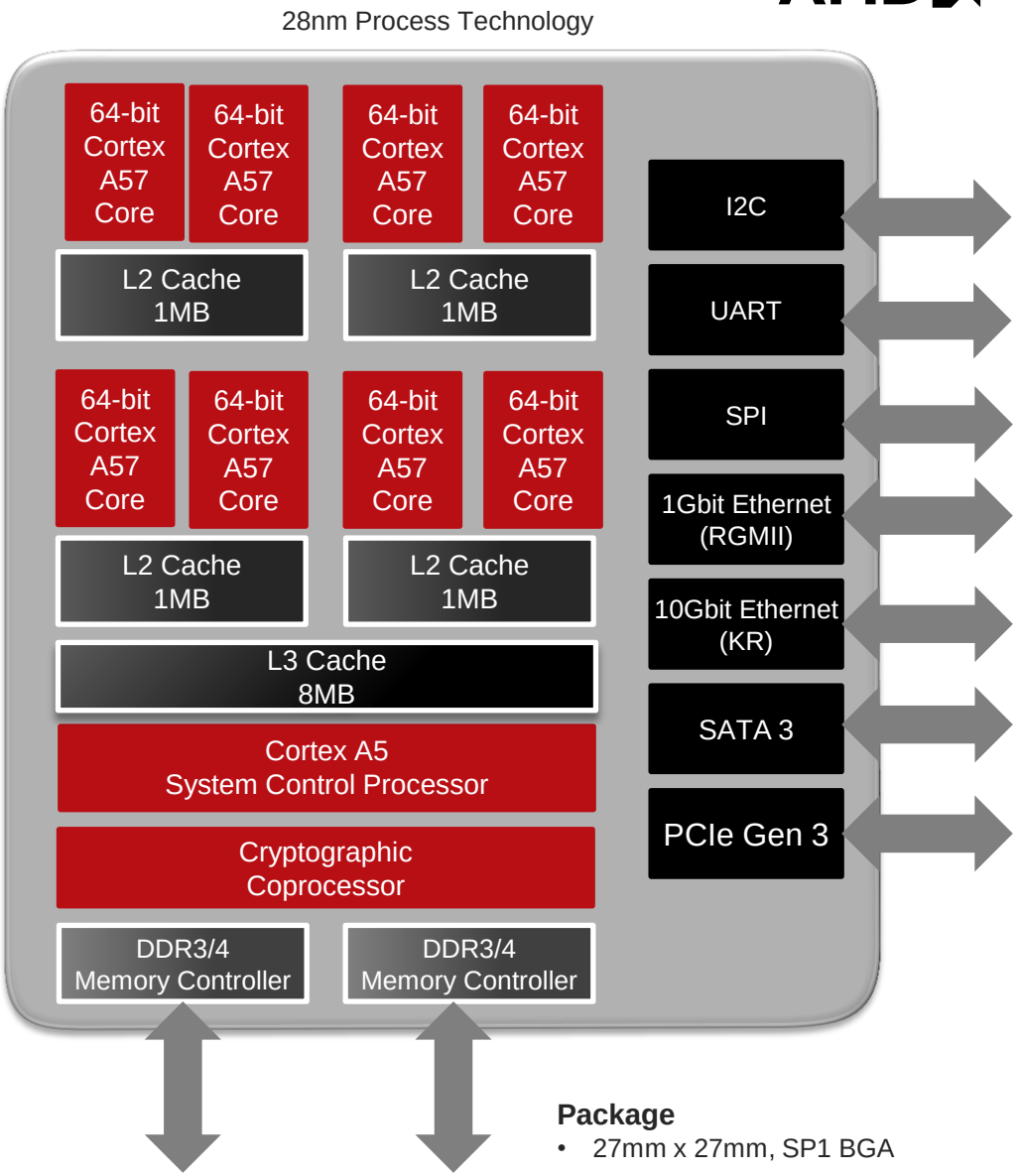
Cache Coherent Network
- Full cache coherency
- 8MB L3 cache
- SMMU: I/O address mapping and protection

High Performance, Flexible Memory
- Two 64-bit DDR3/4 channels with ECC
- Two DIMMs/channel up to 1866Mhz
- SODIMM, UDIMM, RDIMM support
- Up to 128GB per CPU

Highly Integrated I/O
- 8x SATA 3 (6Gb/s) ports
- Two 10GBASE-KR Ethernet ports
- 8 lanes PCI-Express® Gen 3, supports x8, x4, x2

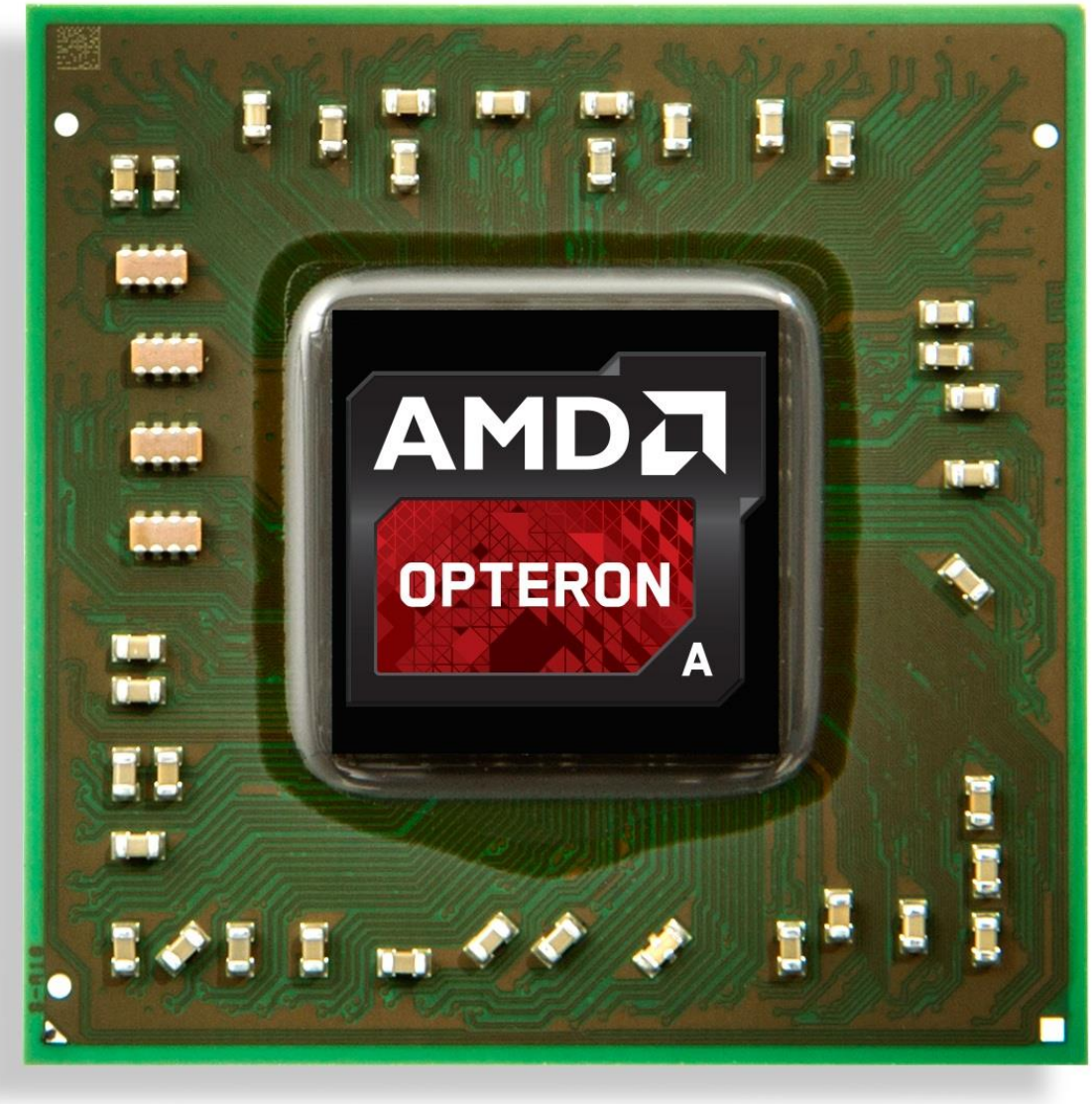
System Control Processor
- TrustZone® technology for enhanced security
- Dedicated 1GbE system management port (RGMII)
- SPI, UART, I2C interfaces

Cryptographic Coprocessor
- Separate Cryptographic algorithm engine for offloading encryption, decryption, compression, decompression computations

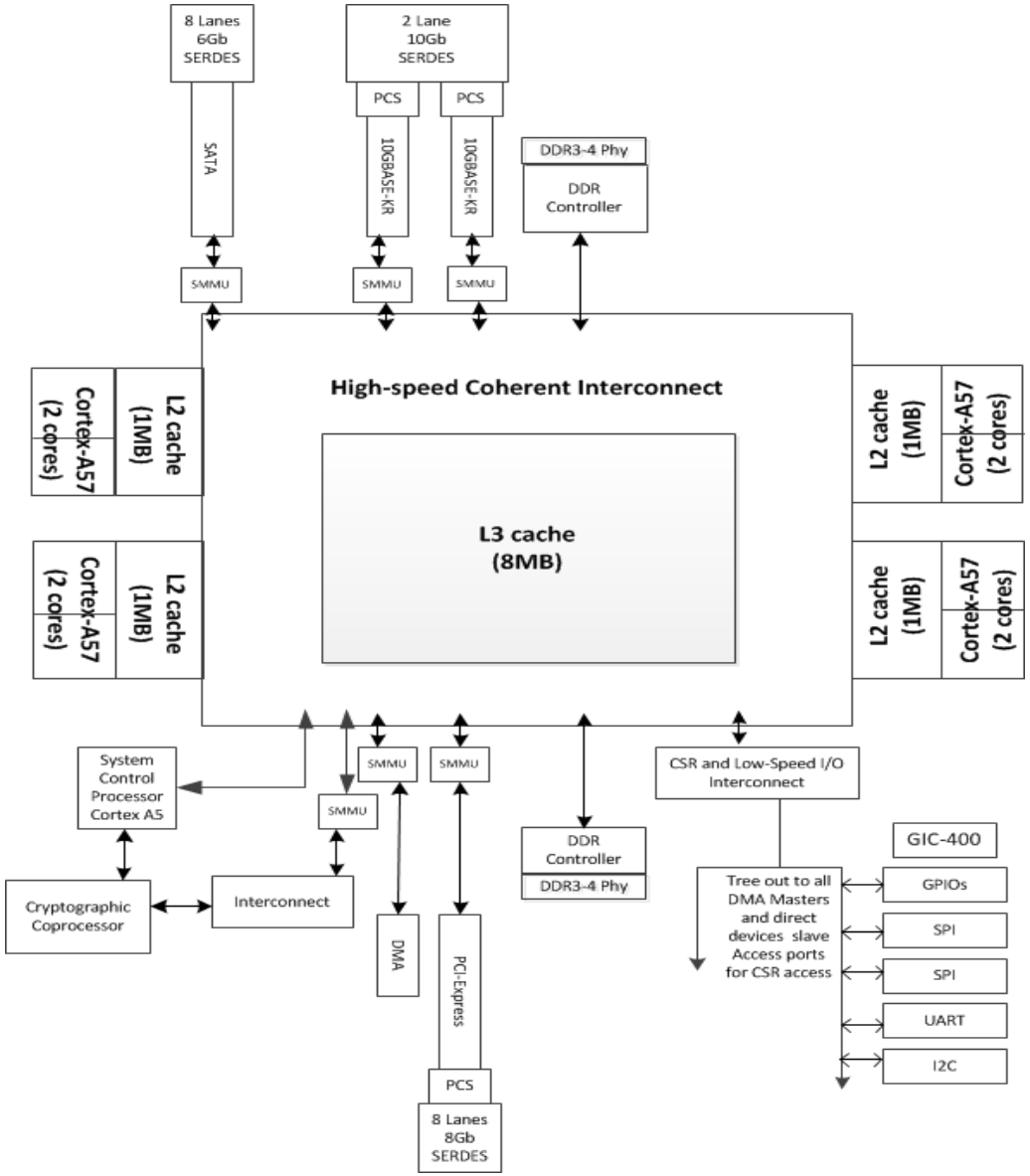


Package
- 27mm x 27mm, SP1 BGA

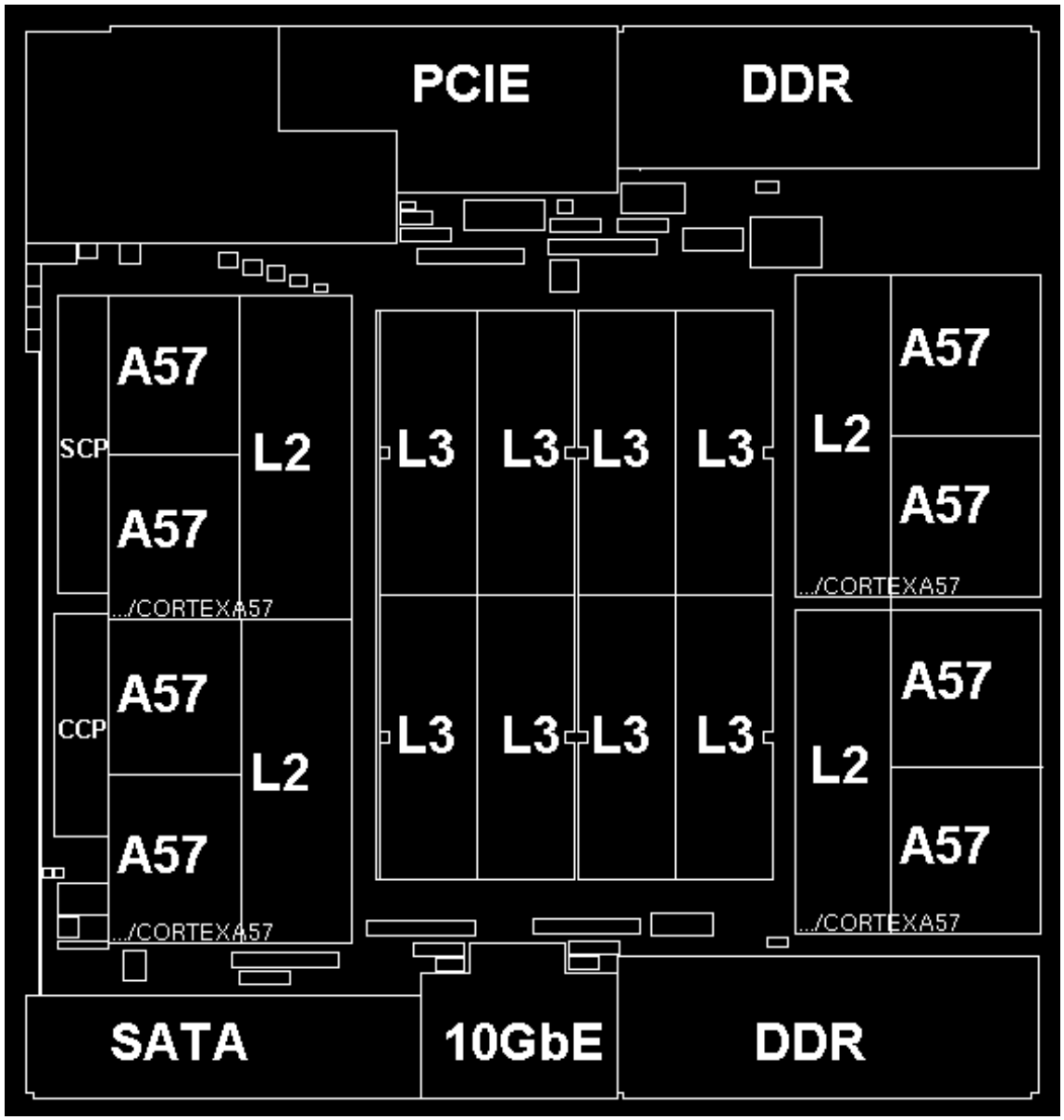
“SEATTLE” BALL GRID ARRAY PACKAGE



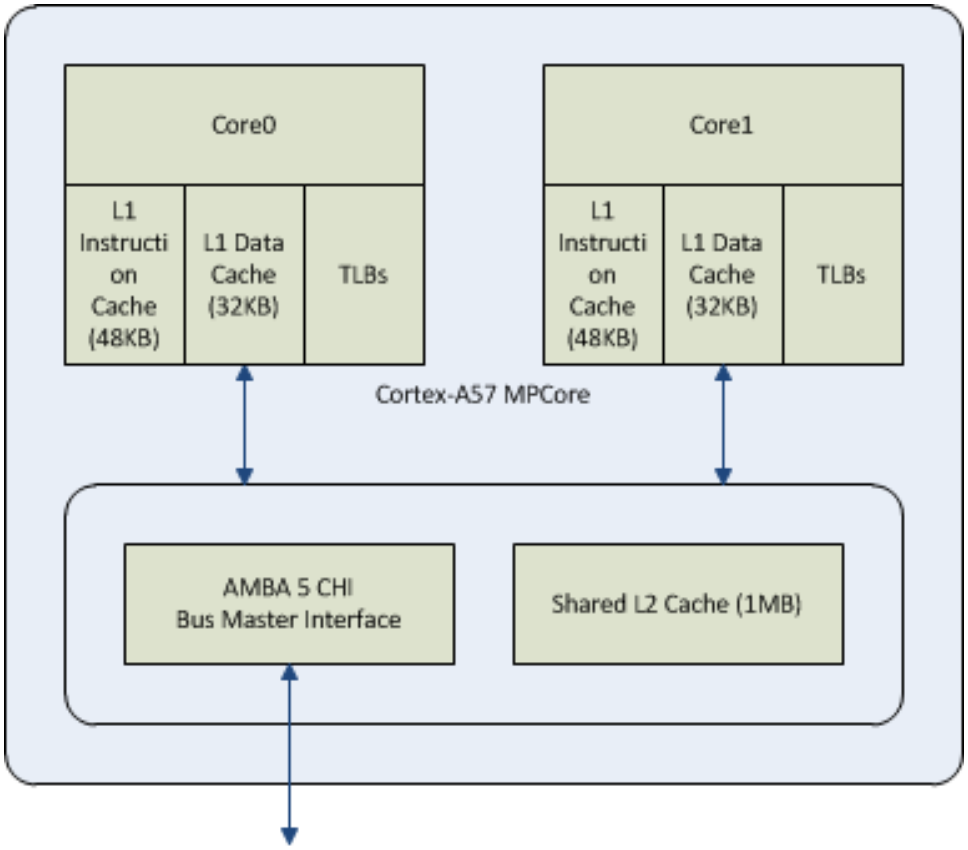
“SEATTLE” SIMPLIFIED BLOCK DIAGRAM



“SEATTLE” FLOORPLAN



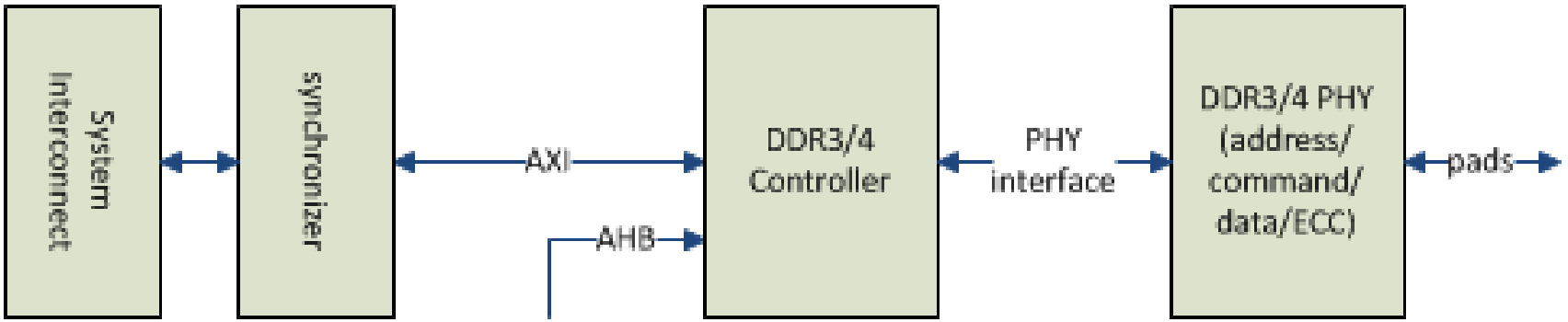
“SEATTLE” CORTEX-A57 MPCORE, L1/L2/L3 CACHES



- 2 X A57 cores plus shared 1MB L2 cache
- ARMv8-A architecture
- Caches (64 byte cache line size)
  - 48KB Level 1 Instruction Caches, 3-way set associative, parity protected
  - 32KB Level 1 Data Caches, 2-way, ECC protected
  - 1MB shared Level 2 Cache, 16-way, ECC protected
  - 8MB shared Level 3 Cache, 16-way, ECC protected (Snoop filter integrated with L3 cache)
- Cryptographic instructions included
- AMBA 5 CHI interface to rest of system
- CoreSight debug, Cross-Trigger Interface (CTI) and Embedded Trace Macrocell (ETM) also in MPCore
- Interface to Generic Interrupt Controller (GIC) also in MPCore

“SEATTLE” MEMORY SYSTEM

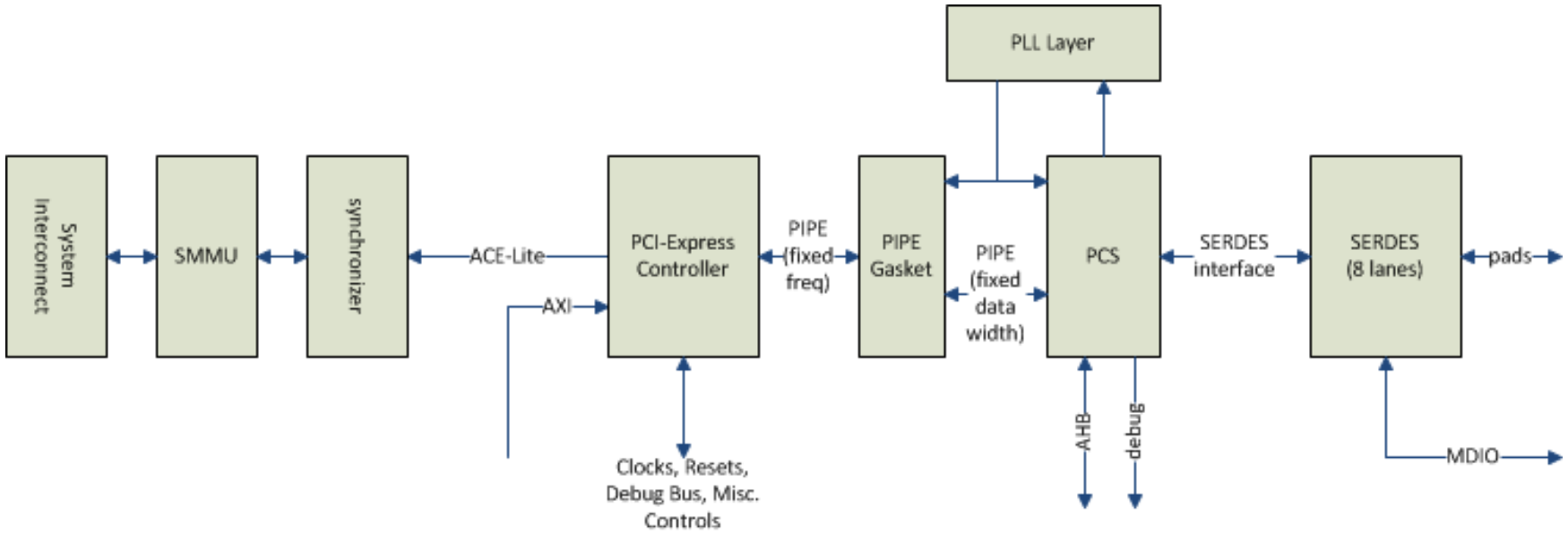
DRAM CONTROLLERS



- 2 interleaved DDR3/4 DRAM channels
  - 72-bit datapath (data + ECC) per channel
  - 1 or 2 DIMMs per channel supported
  - RDIMMs, SODIMMs, UDIMMs supported (dependent on system design)
  - Up to 128GB with 4 RDIMMs
- DRAM controller clk runs at ¼ of the DDR3/4 data rate
  - Ex: DDR3-1600 requires 400MHz DRAM controller clk
- Single-bit Error Correct/Double-bit Error Detect (SECDED) ECC
  - Single-bit errors corrected inline before data delivered to requester

PCI-EXPRESS COMPLEX

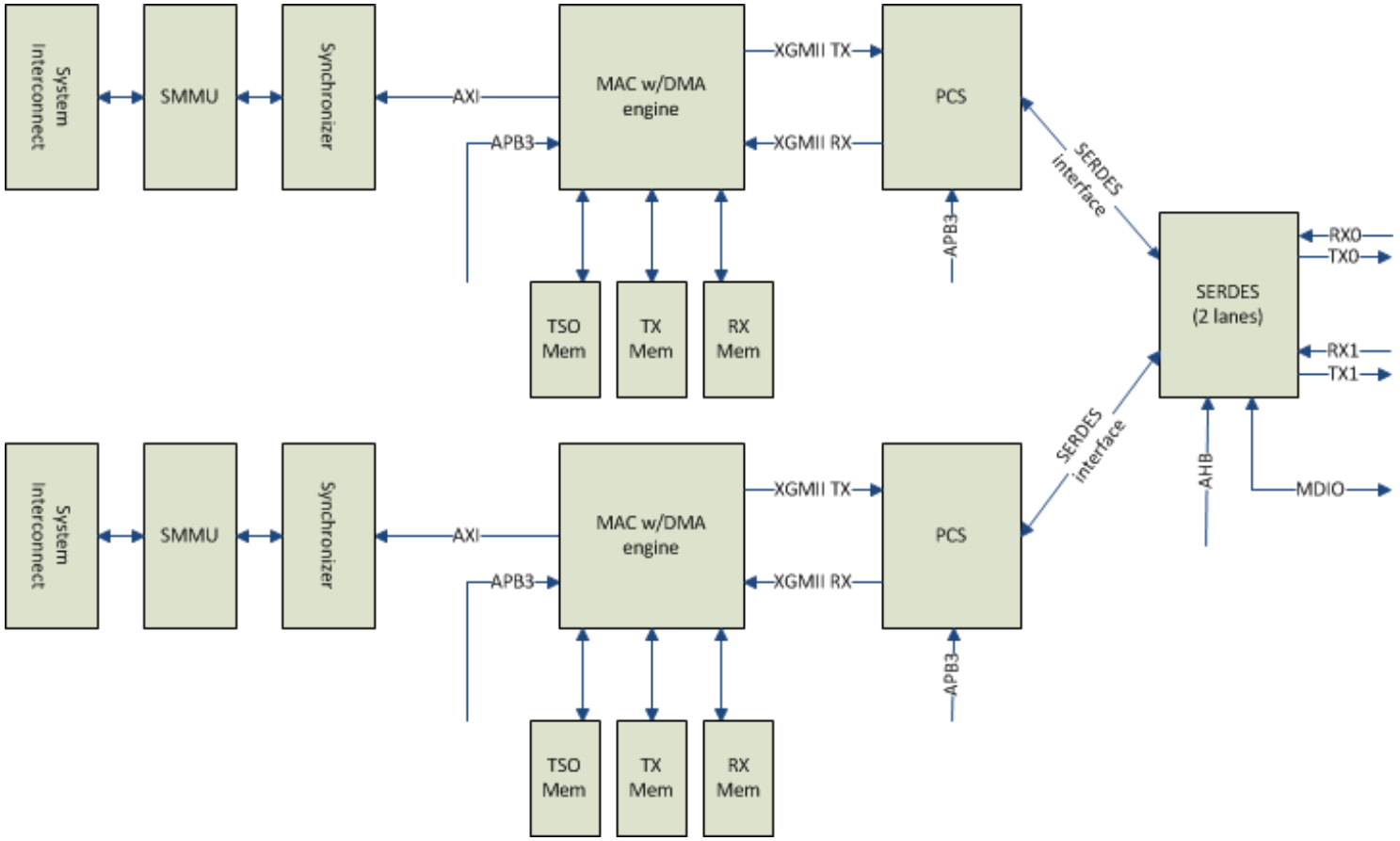
8 LANES OF PCI-EXPRESS



- Supported configs: x8 (1 controller), x4/x4 (two controllers), x4/x2/x2 (three controllers)
- Each controller supports Gen1/Gen2/Gen3 operation independently of the others
- Message Signalled Interrupts (MSIs) supported
  - 256 Shared Peripheral Interrupts (SPIs) on the GIC-400 for MSIs, non-secure only

10GBASE-KR ETHERNET COMPLEX

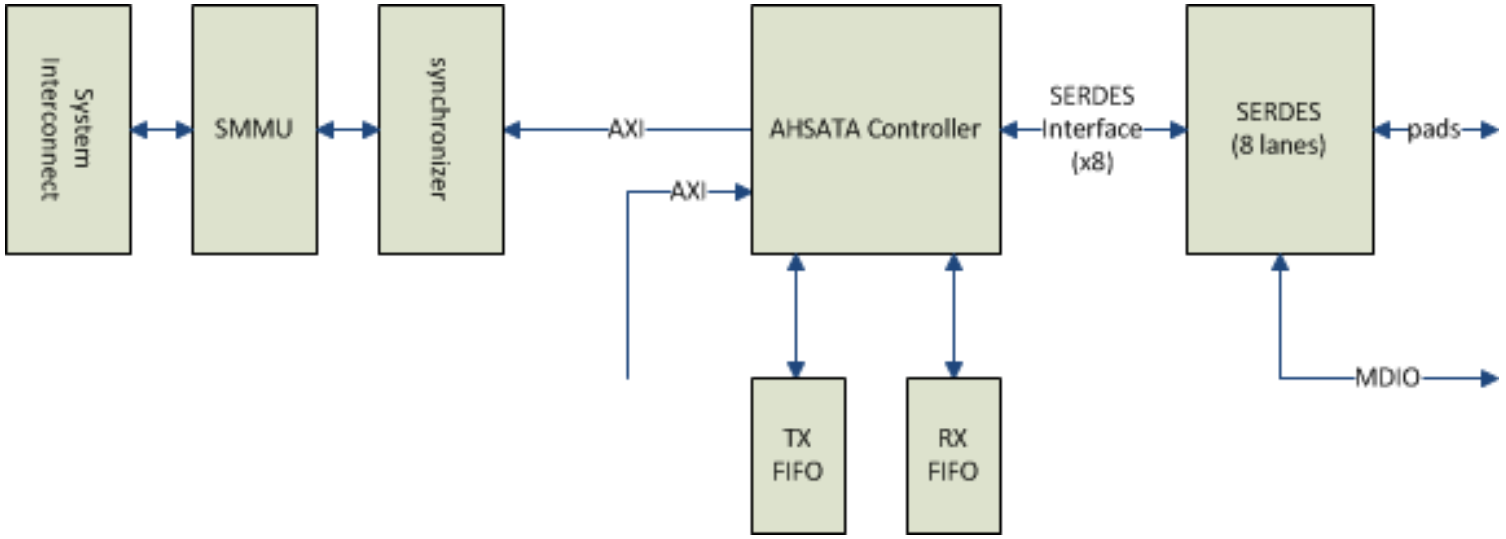
2 CHANNELS OF 10GBASE-KR ETHERNET (SHARED 2-LANE SERDES)



- 1 meter copper printed circuit board channels for backplane Ethernet in dense servers
- 1000BASE-KX (1-gigabit) also supported
- TCP Segmentation Offload (TSO) supported

SATA COMPLEX

8 LANES OF SATA

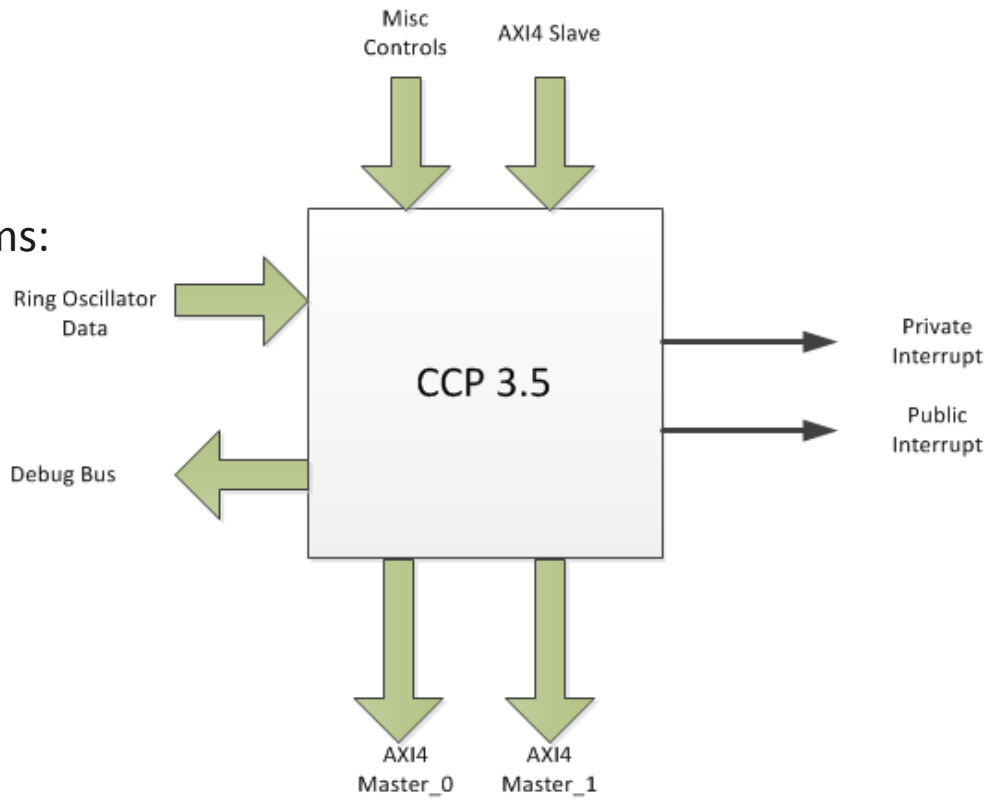


- SATA rev 3.0 compliant
- Advanced Host Controller Interface (AHCI) rev 1.3 compliant
- Supports Gen1/Gen2/Gen3 operation independently per lane

CRYPTOGRAPHIC COPROCESSOR (CCP)

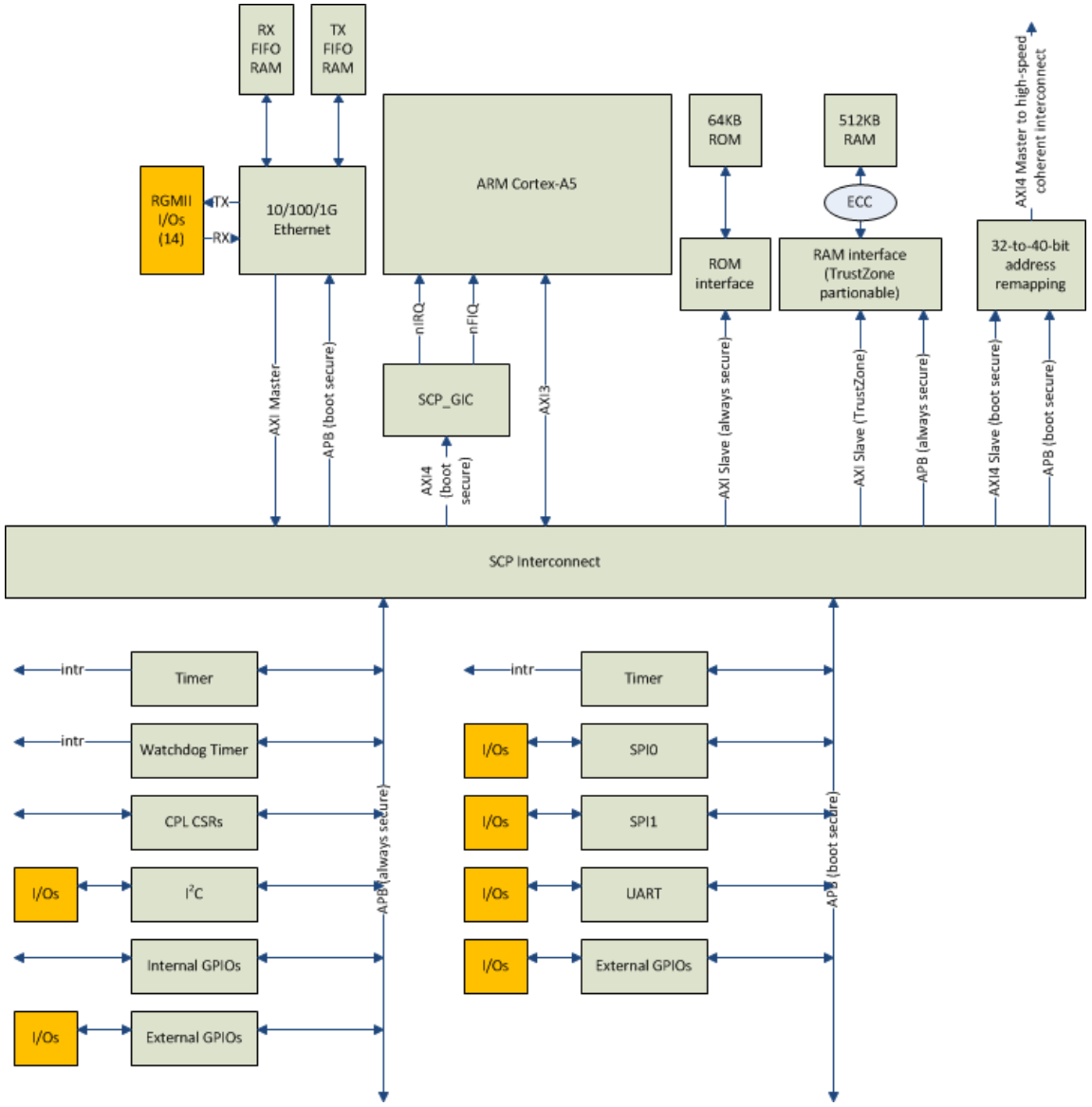
COMPUTE OFFLOAD HARDWARE

- The Cryptographic Coprocessor is a dedicated accelerator for the following encryption/decryption and compression/decompression algorithms:
  - Advanced Encryption Standard (AES)
  - Elliptic Curve Cryptography (ECC)
  - RSA
  - Secure Hash Algorithm (SHA)
  - Zlib compression
  - Zlib decompression
  - True Hardware Random Number Generator
- Available to the System Control Processor (SCP) for secure and non-secure processing
- Available to the Cortex-A57 cores for non-secure processing



SYSTEM CONTROL PROCESSOR

- System Control Processor (SCP) is an ARM Cortex-A5 processor with attached ROM, RAM and I/O devices
- SCP is used to control power, configure the system, initiate booting, and act as a service processor for system management functions
- SCP is effectively a small system-on-a-chip (SOC) within the larger “Seattle” SOC
- SCP looks like an I/O device to the rest of the system

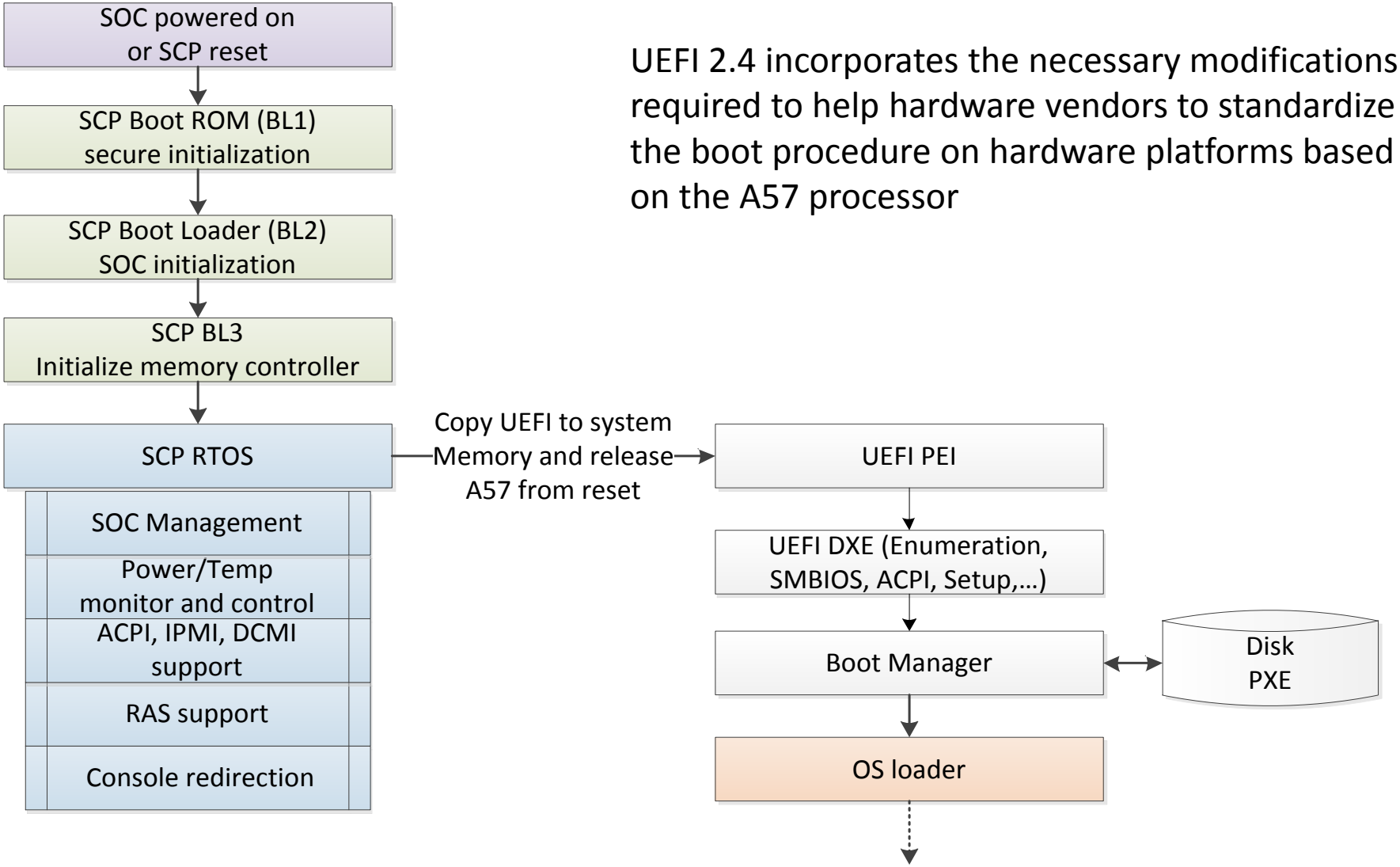


SYSTEM CONTROL PROCESSOR – COMPONENTS

AMD

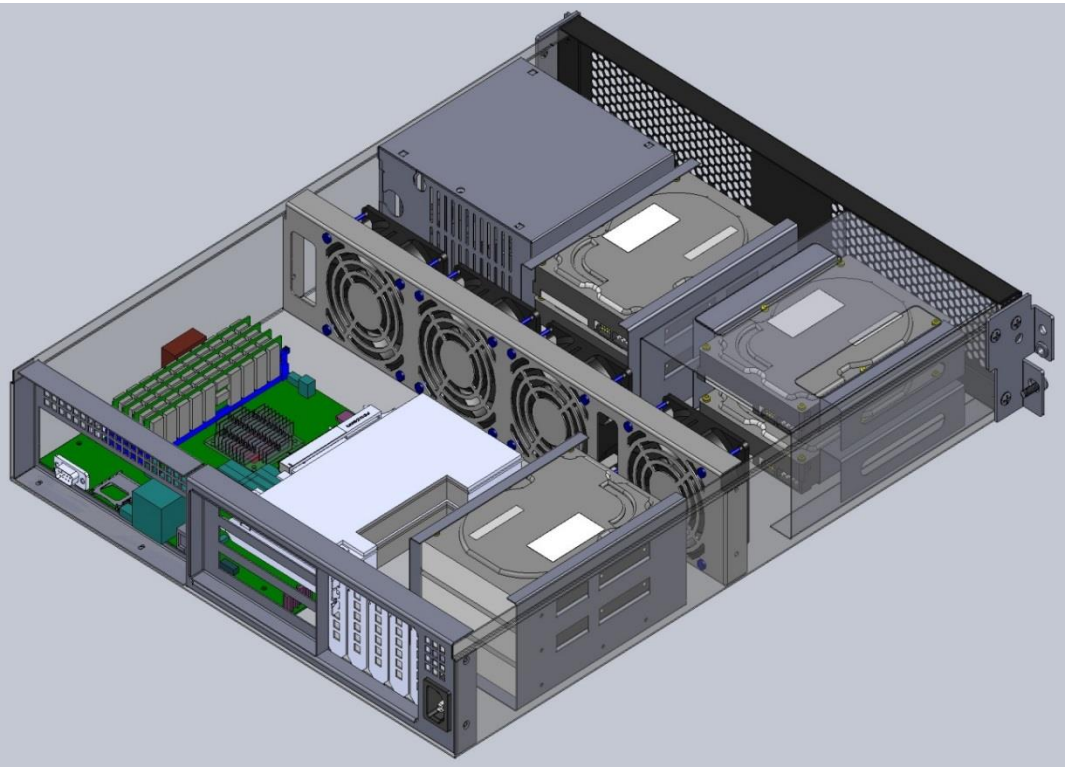
- SCP contains the following components:
  - ARM Cortex-A5 processor with Embedded Trace Macrocell (ETM) and Cross-Trigger Interface (CTI)
  - 64KB ROM
  - 512KB SRAM with TrustZone components to control secure vs. non-secure address regions, ECC protected
  - 10/100/1000 Ethernet for System Management (RGMII)
  - Control and Status Register (CSR) interface for Chip Pervasive Logic (CPL) like clocking, reset, power management, and thermal logic
  - CoreSight debug and performance monitoring logic
  - General Purpose I/O (GPIO) controllers for internal and external signals
  - Generic Interrupt Controller (GIC)
  - I^2C controller
  - Two Serial Peripheral Interface (SPI) ports
  - Timers
  - Universal Asynchronous Receiver/Transmitter (UART)
  - A bridge from the SCP private address space to the high-speed coherent address space

“SEATTLE” SCP/CORTEX-A57 BOOT FLOW



UEFI 2.4 incorporates the necessary modifications required to help hardware vendors to standardize the boot procedure on hardware platforms based on the A57 processor

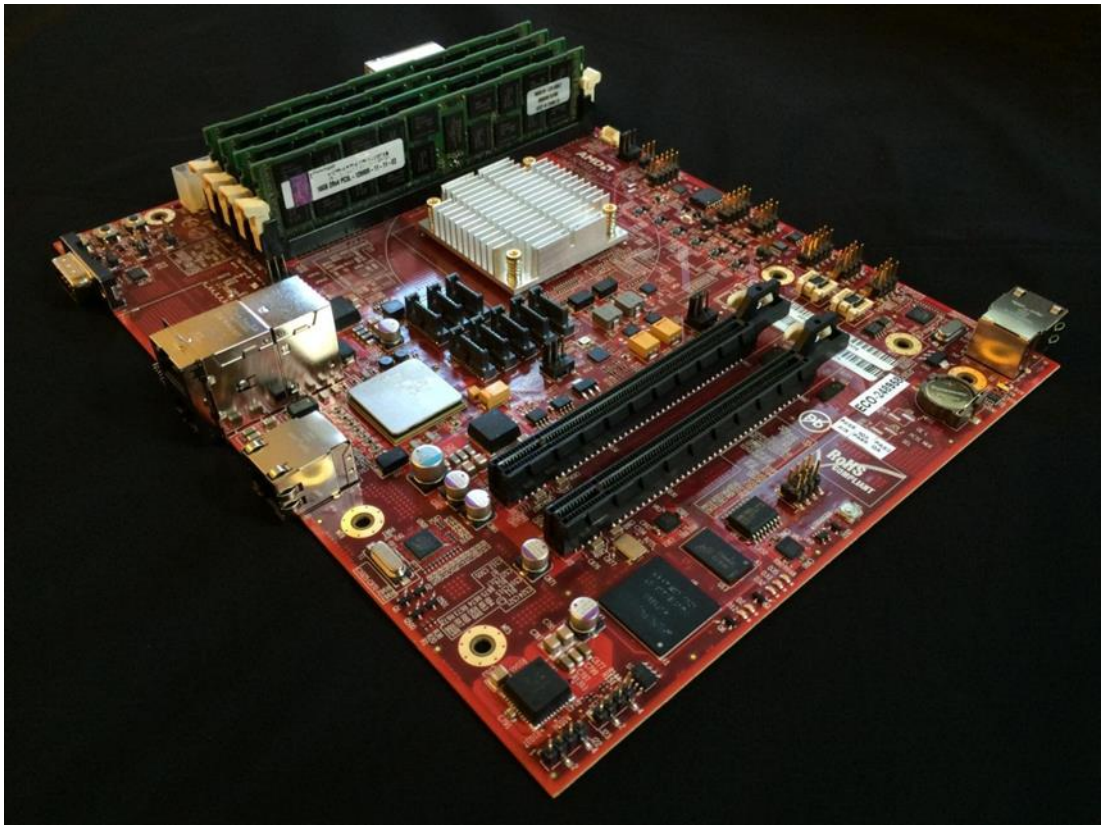
“SEATTLE” REFERENCE SYSTEM



Standalone uATX board

- 1P standalone platform intended to meet the needs of partners (ISV, OSV, IHV)
  - Off-the-shelf 2U rack mount chassis
- DDR3 DIMMS only
- x8 PCIe Gen3 lanes supporting (1) x8 slot or alternatively (2) x4 slots
  - NIC supported through add-in card option
- Supports up to 8 hard drives
- Provisions for remote access to start, stop, and remote console will be provided

“SEATTLE” REFERENCE SYSTEM BOARD



- uATX form factor
- 1 “Seattle” SP1 BGA processor
- DDR3 2-DIMM per memory channel config (up to 4 DIMMs per CPU)
- 1 x8 PCIe slot
  - 2 x4 PCIe slots an alternative via mux
- 8 SATA3 ports
- 2 10GBase-T connectors
- 4 I^2C ports
- 2 UARTs
- Supports required debug features

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