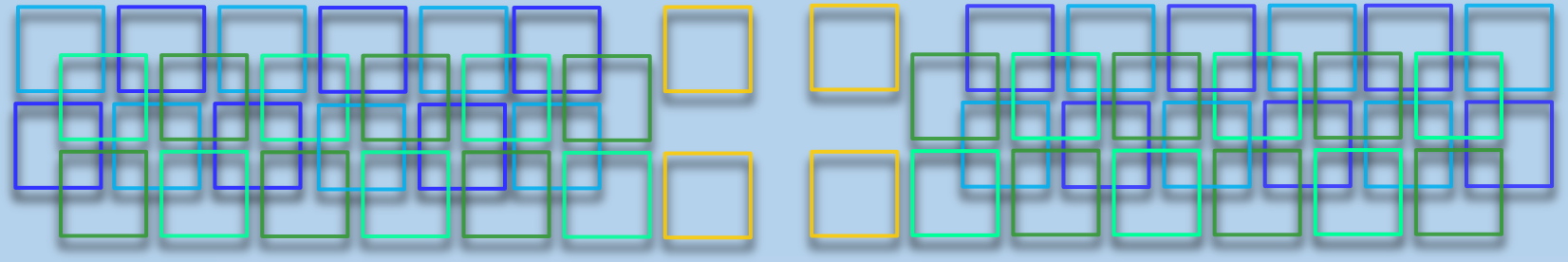

Low-Cost 3D Chip Stacking with ThruChip Wireless Connections

Dave.Ditzel@ThruChip.com
Tadahiro.Kuroda@ThruChip.com
Stephen.Lee@ThruChip.com

ThruChip Communications
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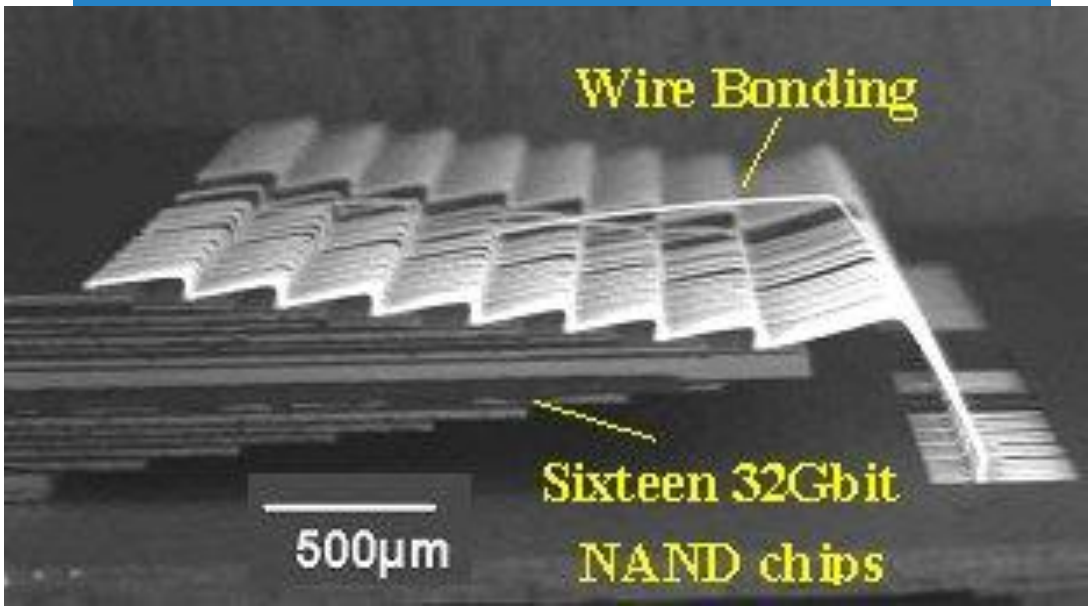
Hot Chips 26

Wireless 3D stacking

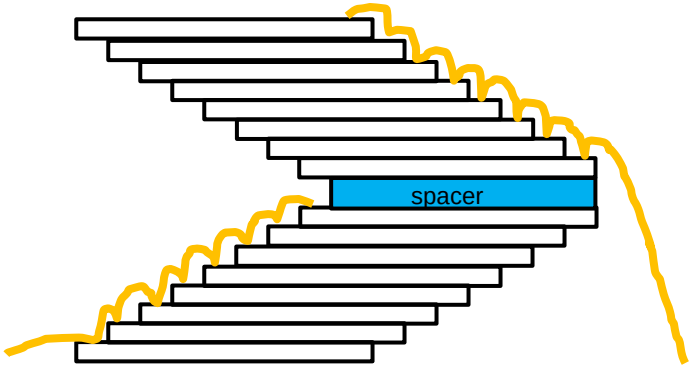
- Current 3D stacking methods have challenges
  - Main challenge is the high cost of Thru Silicon Vias
- Wireless is a better approach for stacking
  - Lower cost, lower power, higher bandwidth
  - Less costly if we can avoid having to add vertical wires
- Cost reduction possible, instead of increase, with:
  - Advances in wafer thinning
  - Wireless data communication between stacked die
  - Lower-cost power distribution from front to back of die

Challenges with current 3D stacking

3D Stacking with Wire Bonds



Staircase stacking constrains wire bond access to one side of each die.



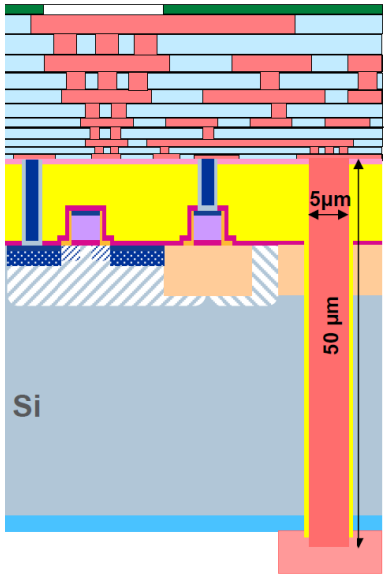
Pros:

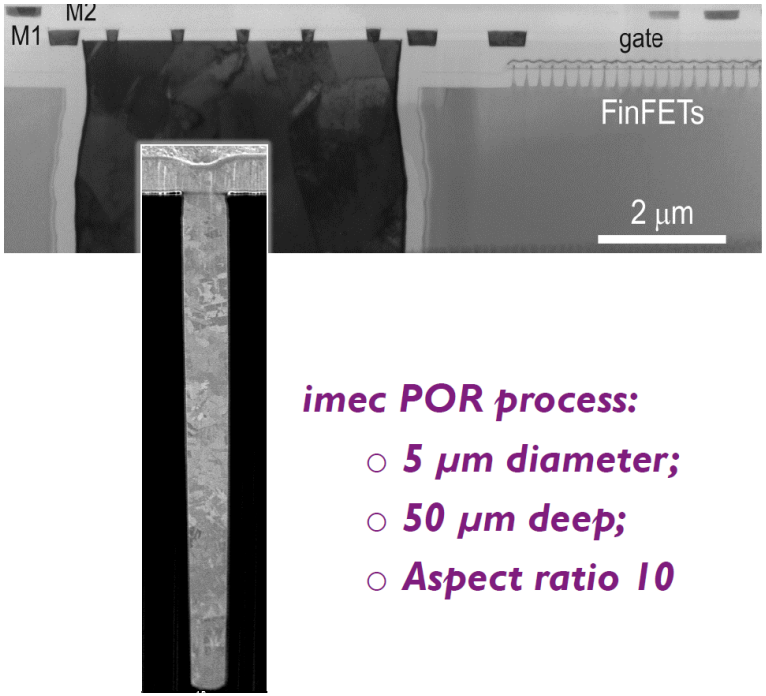
- Low Cost
- Good yield
- Allows ~50µ thin die
- Existing infrastructure

Cons:

- High wire bond inductance
- Higher power IO
- Bandwidth limited to a few GHz
- Staircase stacking constraints
  - Limited number of bond wires
  - Underside clearance limits die thinness

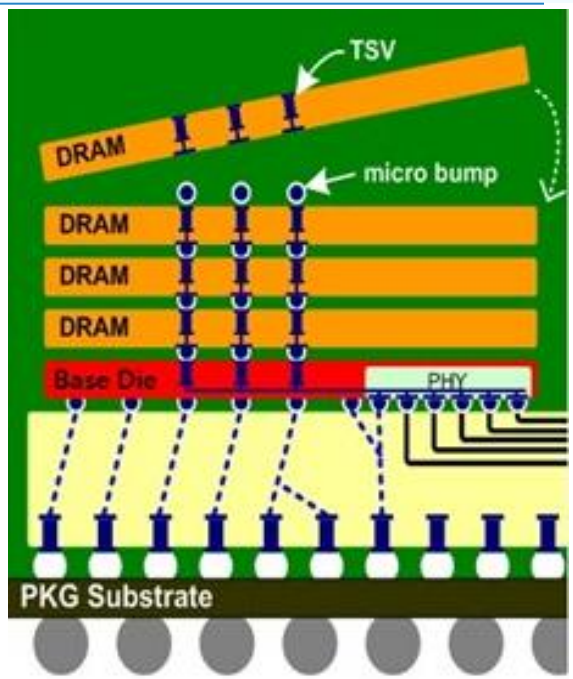
3D Stacking with Thru Silicon Vias (TSV)





imec POR process:

- *5 µm diameter;*
- *50 µm deep;*
- *Aspect ratio 10*



Pros:

- ~10x lower power IO
- Thousands of IO possible

Cons:

- High Cost (1.4x - 2x) over bare die
- Requires new CMOS process
- Yield reductions from bumps
- Area impact from TSV & KOZ
- Effects on nearby transistors

Proposal for lower cost 3D stacking

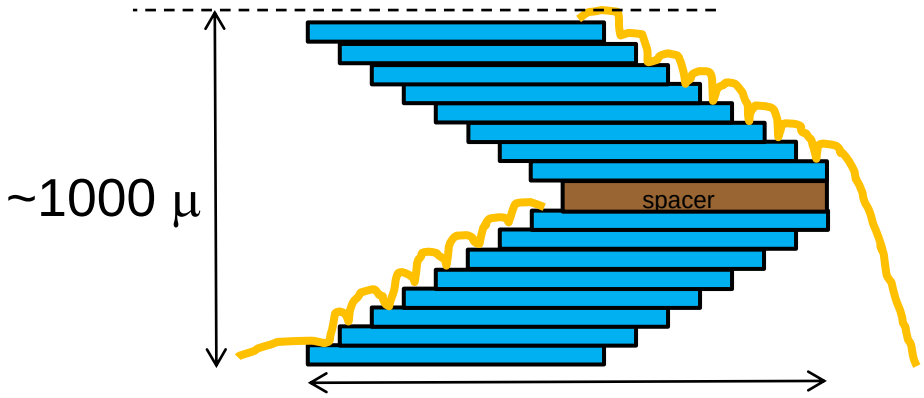
- Separate *Data Communication* from *Power Distribution*

- Data Communication: Use wireless near-field inductive coupling
  - Uses simple CMOS digital circuits: No new semiconductor process expense
  - Provides best in class inter-die power and bandwidth
  - May reduce chip cost if IO area can be reduced
  - Well understood technology validated with dozens of test chips
  - Becomes more compelling as die get thinner

- Power Distribution: Many options available when wireless used for data
  - Wire bond – Low cost, in high volume production
  - TAB – Low cost, in high volume production
  - RDL/FOWLP – Medium cost, production ready
  - TSV – High cost, early production
  - Recommend *Highly Doped Silicon Vias* – New lowest cost proposal, discussed later

NAND goal is to go

From this

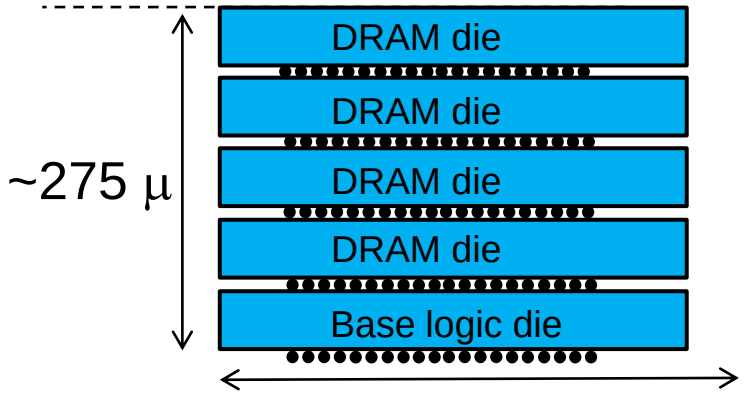


To this

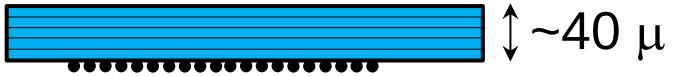
Example	NAND FLASH	NAND FLASH
# stacked die	16	16
Die pitch	50 µ	5 µ
Total height	~1000 µ	~80 µ
Die area	1x	~0.9x
Data communication	wire bond	wireless
Power delivery	wire bond	wireless (no metal)
IO energy/bit	1x	< 1/400x

DRAM goal is to go

From this



To this

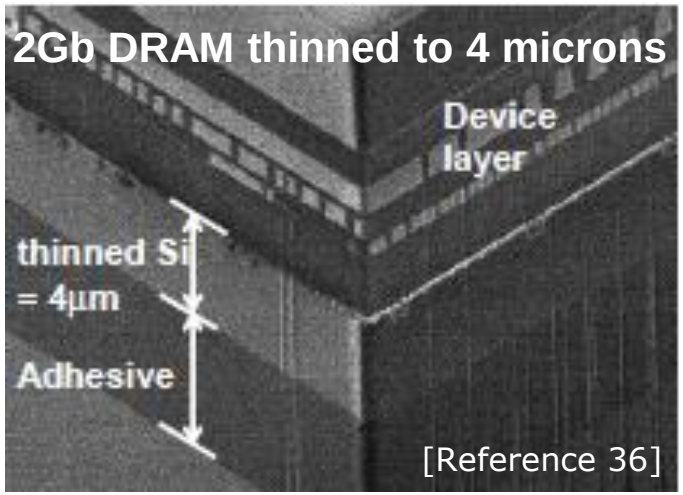


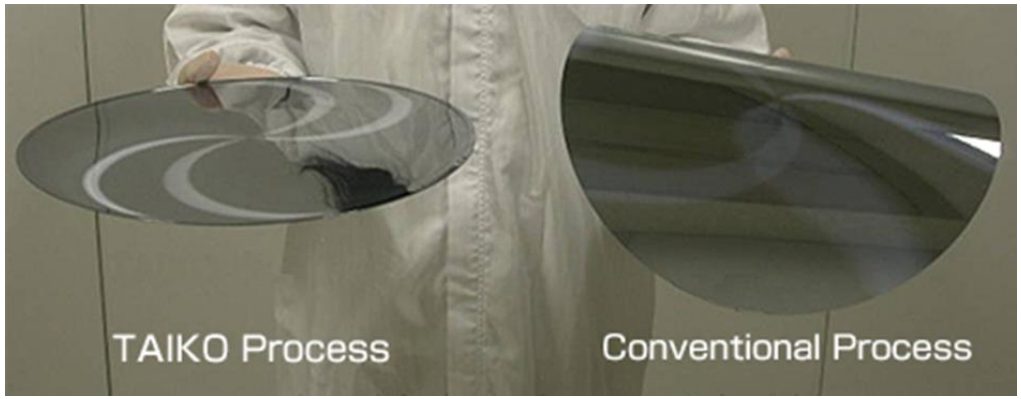
Example	DRAM with TSV	DRAM
# stacked die	5	5
Die pitch	55μ	8μ
Total height	~275μ	~40μ
Die area	1x	0.87x
Data communication	TSV	wireless
Power delivery	TSV	wireless (no metal vias)
IO energy/bit	1x	< 1/10x

Relevant advances in wafer thinning

Ultra-Thin 4μ wafer breakthrough

- Wafer thinning has been stuck at ~40μ due to "Gettering problem"
  - Barrier was due in part to loss of the "gettering effect" at smaller dimensions when performing back grinding, causing impurities affecting device performance (particularly leakage) and yield.
- DISCO Corporation solution can now thin to a few microns
  - DISCO introduced a "Gettering Dry Polish" wheel which forms gettering sites while grinding, allowing thinning of wafer silicon to a few microns without device damage. [35]
- Example: DRAM silicon thinned to 4 microns
  - See "Ultra Thinning down to 4μm using 300-mm Wafer proven by 40-nm Node 2 Gb DRAM for 3D Multi-stack WOW Applications."[36] They concluded "No degradation in terms of retention characteristics and distribution employing 2 Gb DRAM wafer was found after ultra-thinning."





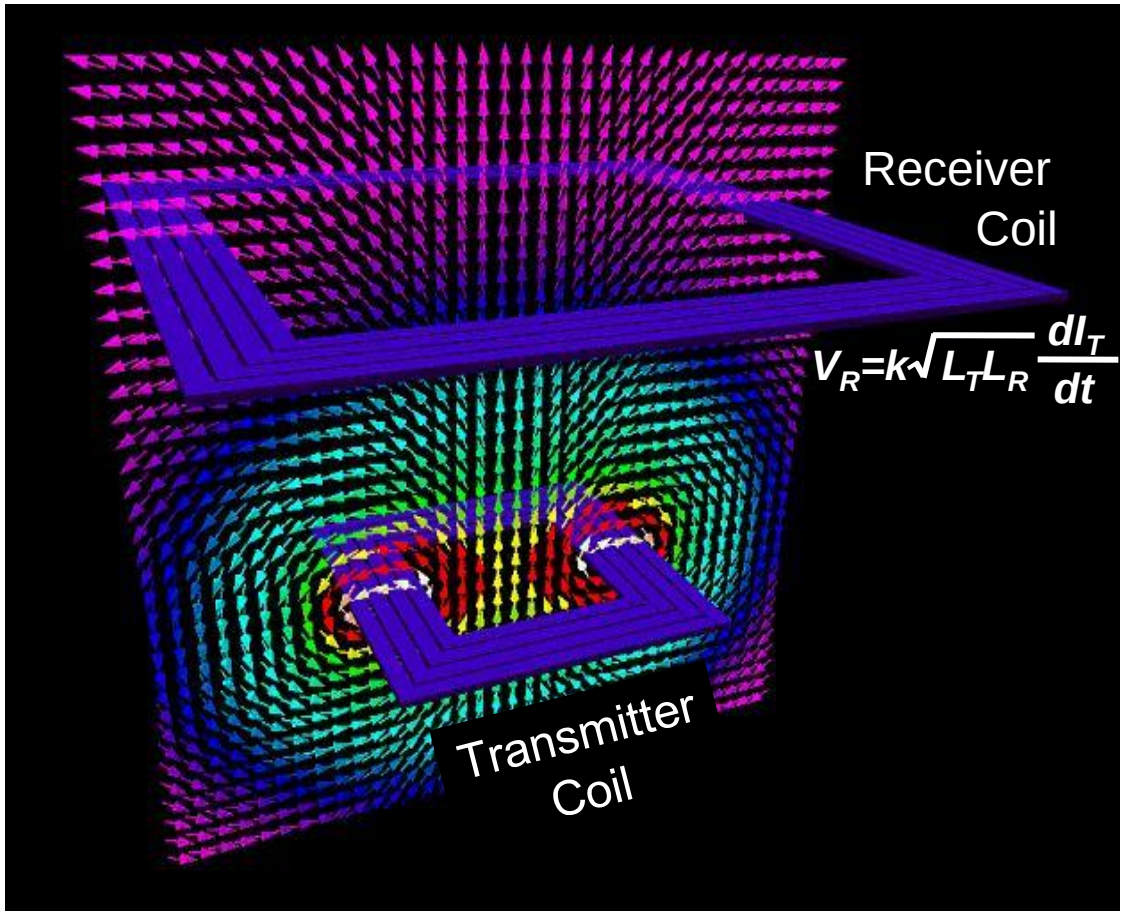
Ultra-thin wafers can be handled (from DISCO website)

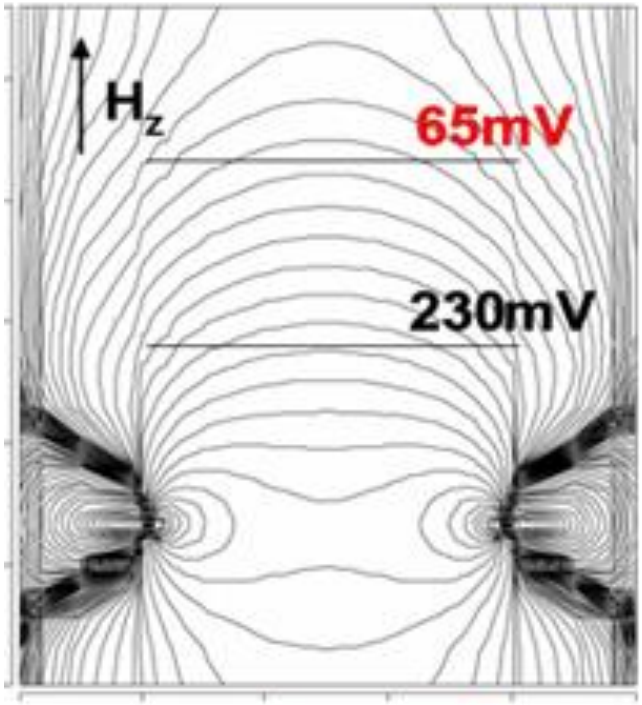
Wireless 3D data

Wireless Near-Field Inductive Coupling

- Chip designers often spend a lot of time making sure they do not have too much coupling between adjacent wires.
- Idea: Turn that coupling into an advantage.
- Use Inductive Coupling for 3D wireless data communication
  - Inductive coils made with a few turns in standard metal layers
  - Coil diameter is about 3x the communication distance
  - Coils communicate vertically to adjacent chips by magnetic field
  - Receive and transmit coils can be placed concentrically on each die to form a transceiver
  - Multiple coils used to increased bandwidth
  - Bandwidth improves with Moore's law improvement in devices

Communication is via magnetic field





$\mu_{si} = \mu_{siO_2} = 1$

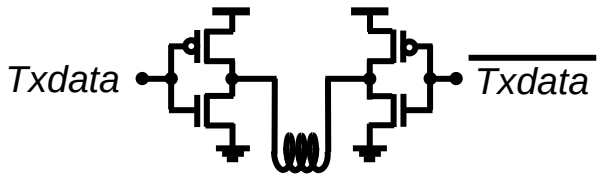
Can easily induce a 200 mV signal in receiver coil.

Magnetic field can pass through silicon, including over active circuitry.

ThruChip Interface (TCI)

- Simple transmitter and receiver circuits (basic form shown)
- Standard digital CMOS: Scales with Moore's Law
- Bandwidth: >40 Gigabits/second/coil with modern digital CMOS
- Delay: About 7 equivalent logic gates (NAND2 FO4)
- Energy: About 80 equivalent gates

TCI Transmitter



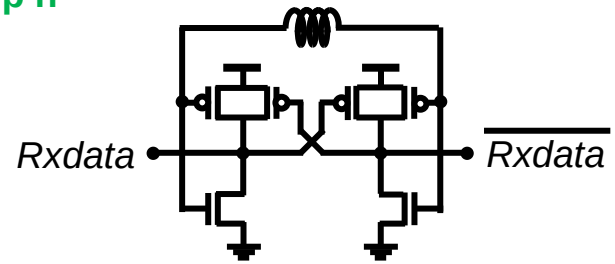
Chip 1

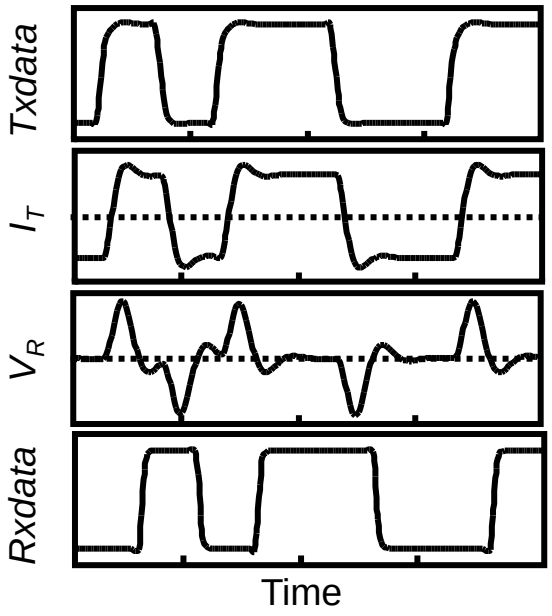
Transmitter Coil

Chip n

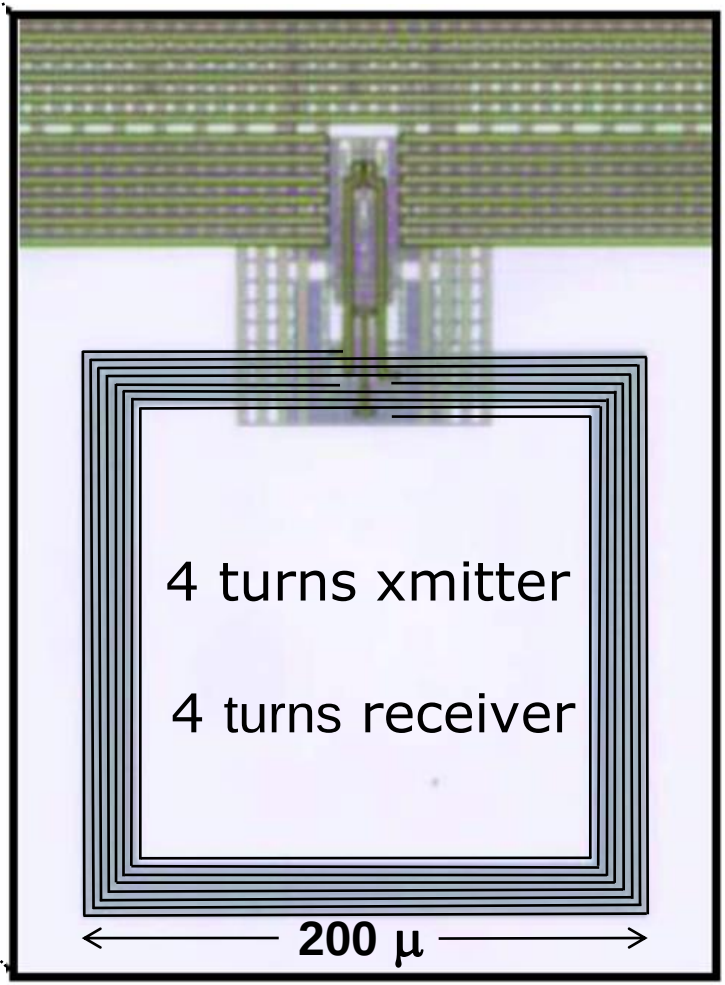
Receiver Coil

TCI Receiver





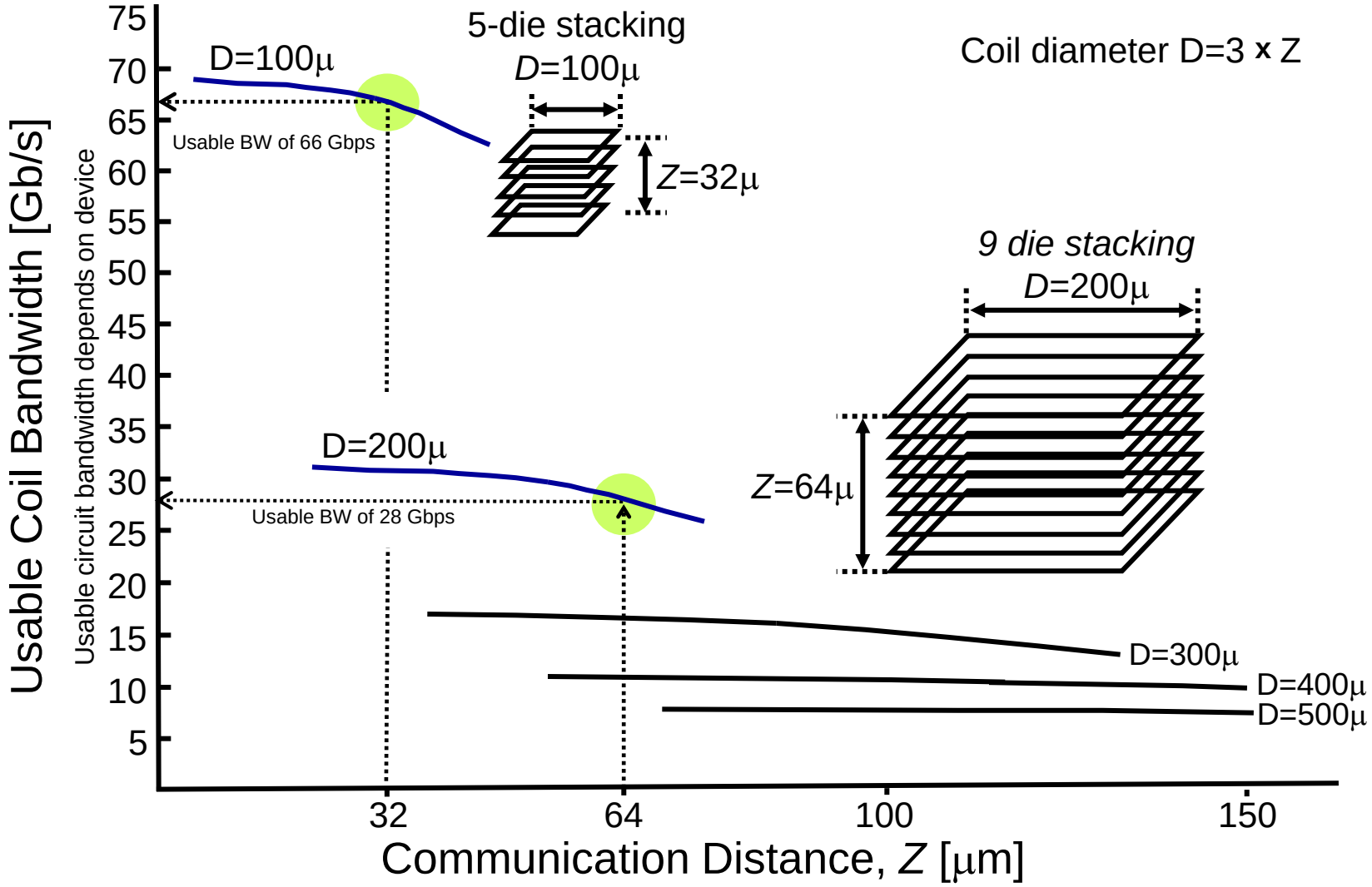
TCI coil example



3 chips with staircase stacking

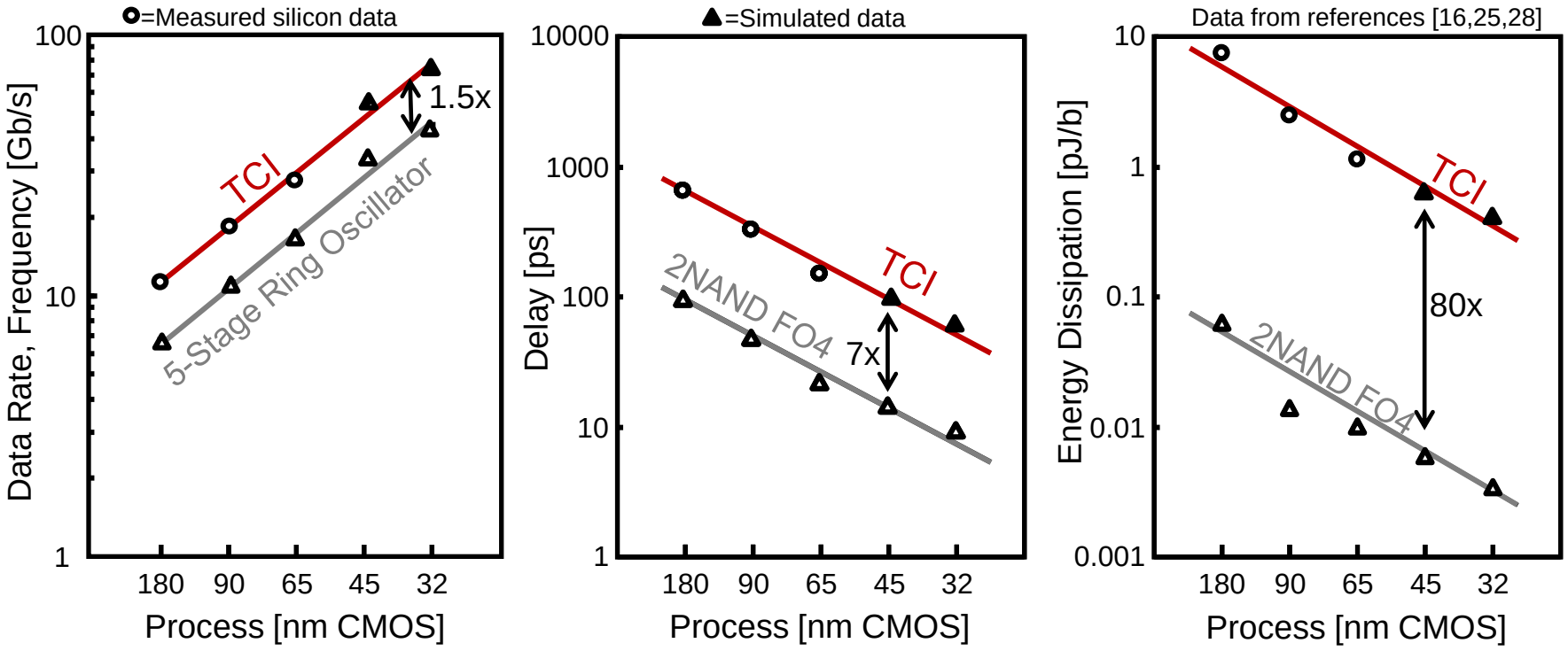
TCI Wireless Transceiver

TCI bandwidth vs communication distance



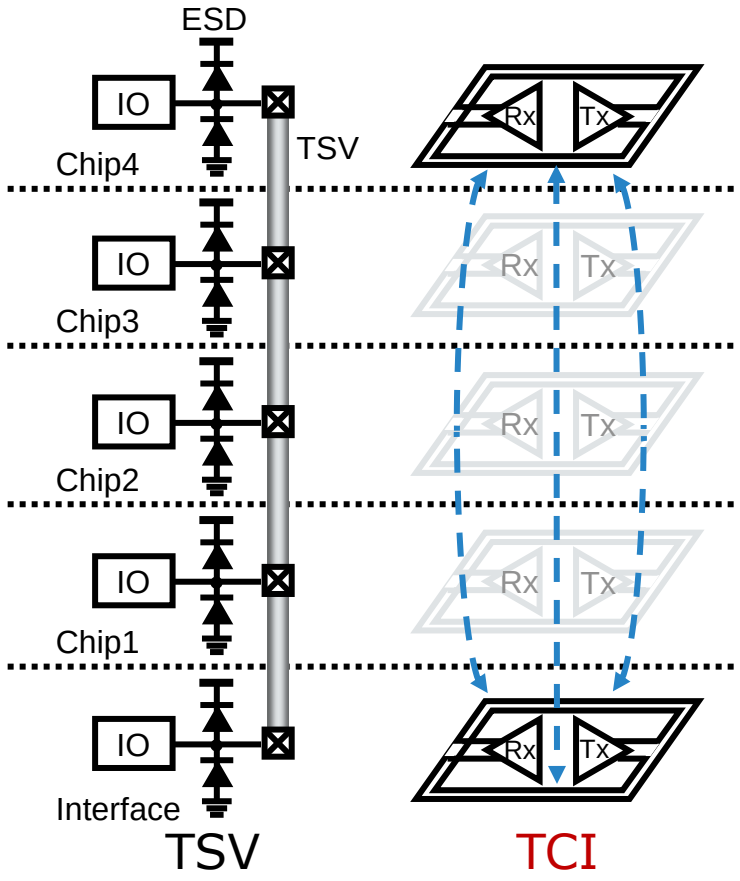
Assumes 8μ die pitch

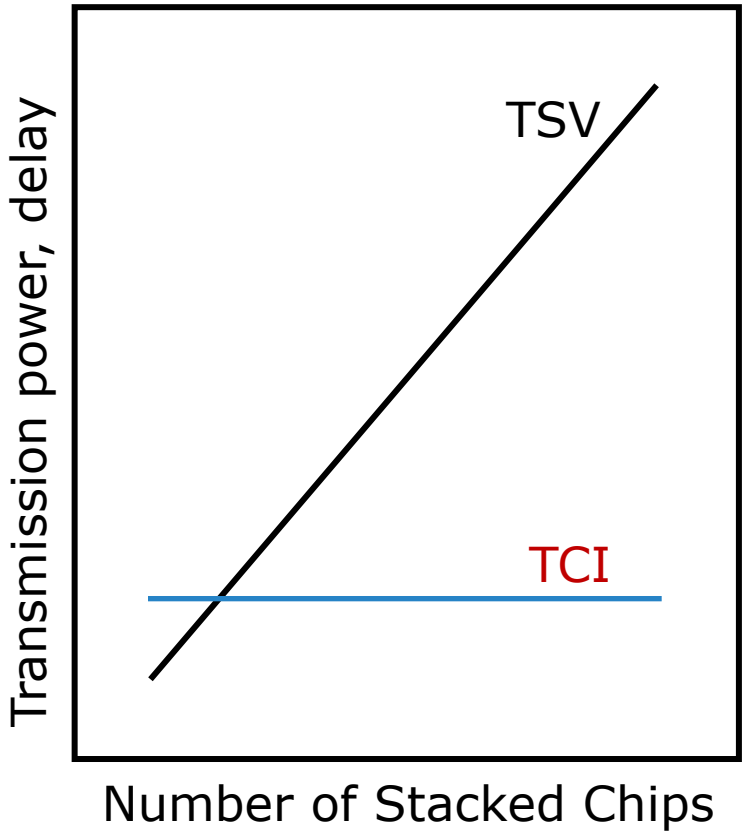
TCI scales with digital CMOS



- High BW: Data rate is equivalent to 1.5x of 5-stage ring oscillator
- Fast: Delay is equivalent to 7x of 2NAND FO4
- Low Power: Energy is equivalent to 80x of 2NAND FO4
- Small: Circuit layout area is equivalent to 36x 2NAND

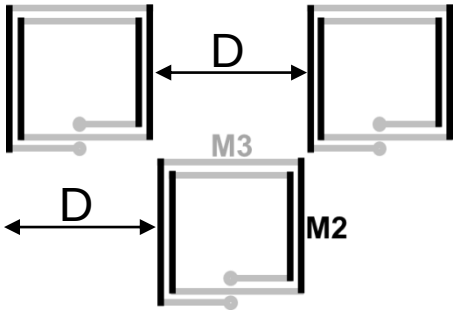
TCI broadcasting more efficient than TSV



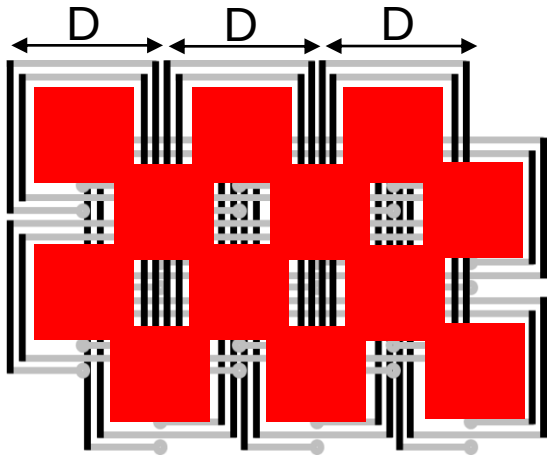


- TSV power and delay is increased in proportion to # of stacked chips.
- TCI transmitter consumes constant power and delay.

TCI Coils can be overlapped with QPDM

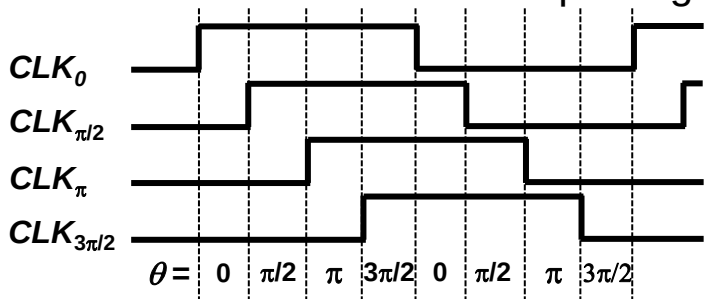


(a) Conventional TCI coil spacing



(b) Overlapping TCI coils

Quadrature Phase Division Multiplexing (QPDM)



1 D coil spacing avoids crosstalk

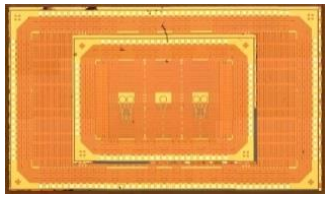
Can pack coils 4x denser with QPDM

Receiver circuits disable out-of-phase channels to further improve noise immunity[37].

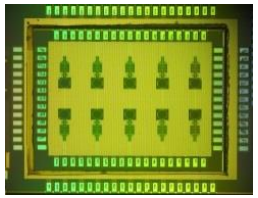
Area efficiency is improved by 4 times with overlapping coils

TCI demonstrated with 28 test chips

- High Speed

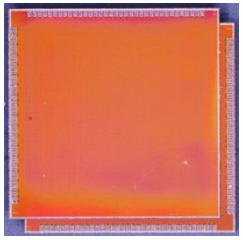


11Gb/s/ch
(180nm)
[13]



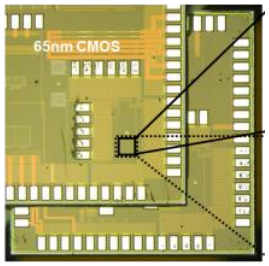
30Gb/s/ch
(65nm)
[38]

- High Bandwidth



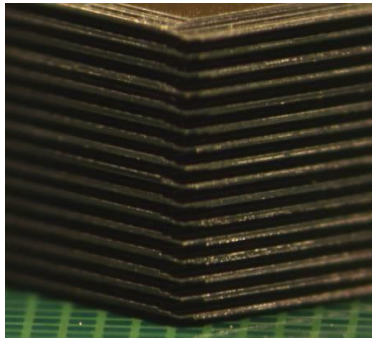
8Tb/s
(180nm,1000ch)
[25]

- Low Power



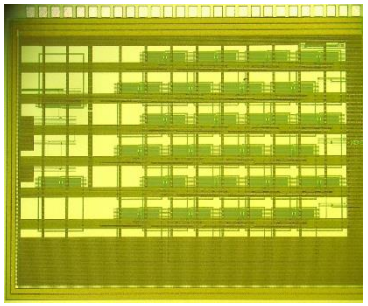
0.01pJ/b
(65nm)
[39]

- High Integration



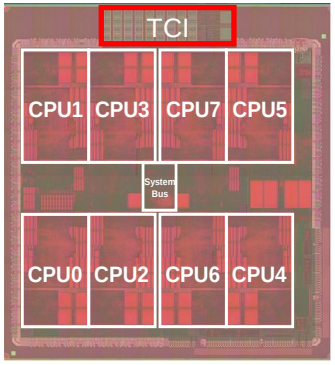
128-die stacking
[26]

- 4x coil density

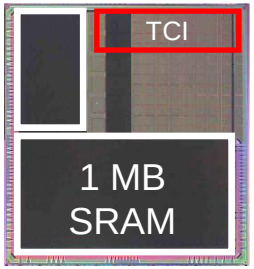


Overlaped coils with QPDM
(180nm)
[37]

- CPU/Memory



(90nm)



(65nm)

[17,18]

ThruChip introduces Highly Doped Silicon Vias (HDSV) for “Wireless” Power Delivery

HDSV: A new way to deliver power

- Ultra-thin wafers make inductive coupling for data very compelling
- Ultra-thin wafers are key to a novel mechanism for power delivery

- At <10μ thickness can create power vias by highly doping the silicon
- With high levels of doping, silicon regions are conductive like metal
- Can pattern front-to-back conductive regions with an ion implant mask

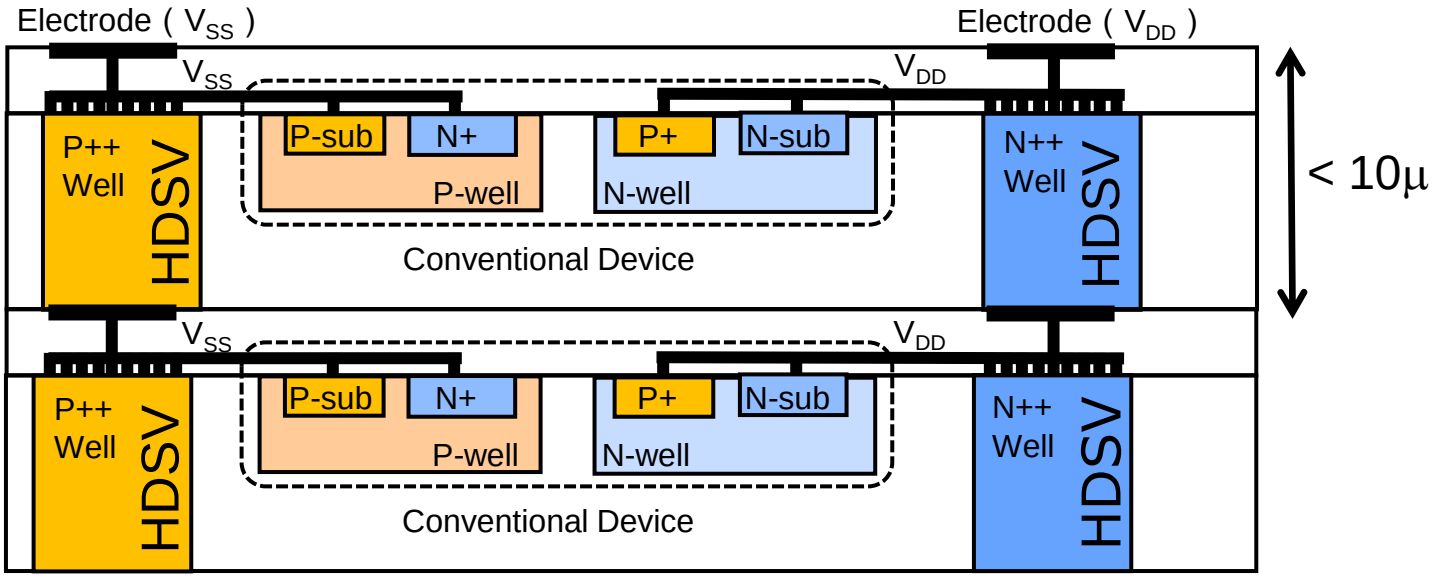
- P+ and N+ doping increased by ~10-100x in desired regions
- Can be done with standard fab equipment
- Low cost step, less expensive than wire bonds

- Let's look at an example of Highly Doped Silicon Vias (HDSV)

Highly Doped Silicon Vias for power distribution

Start with standard wafer
Add implants to create highly doped regions for power vias
Then add transistors and metal normally, metal caps on HDSV
Thin silicon to ~4 microns

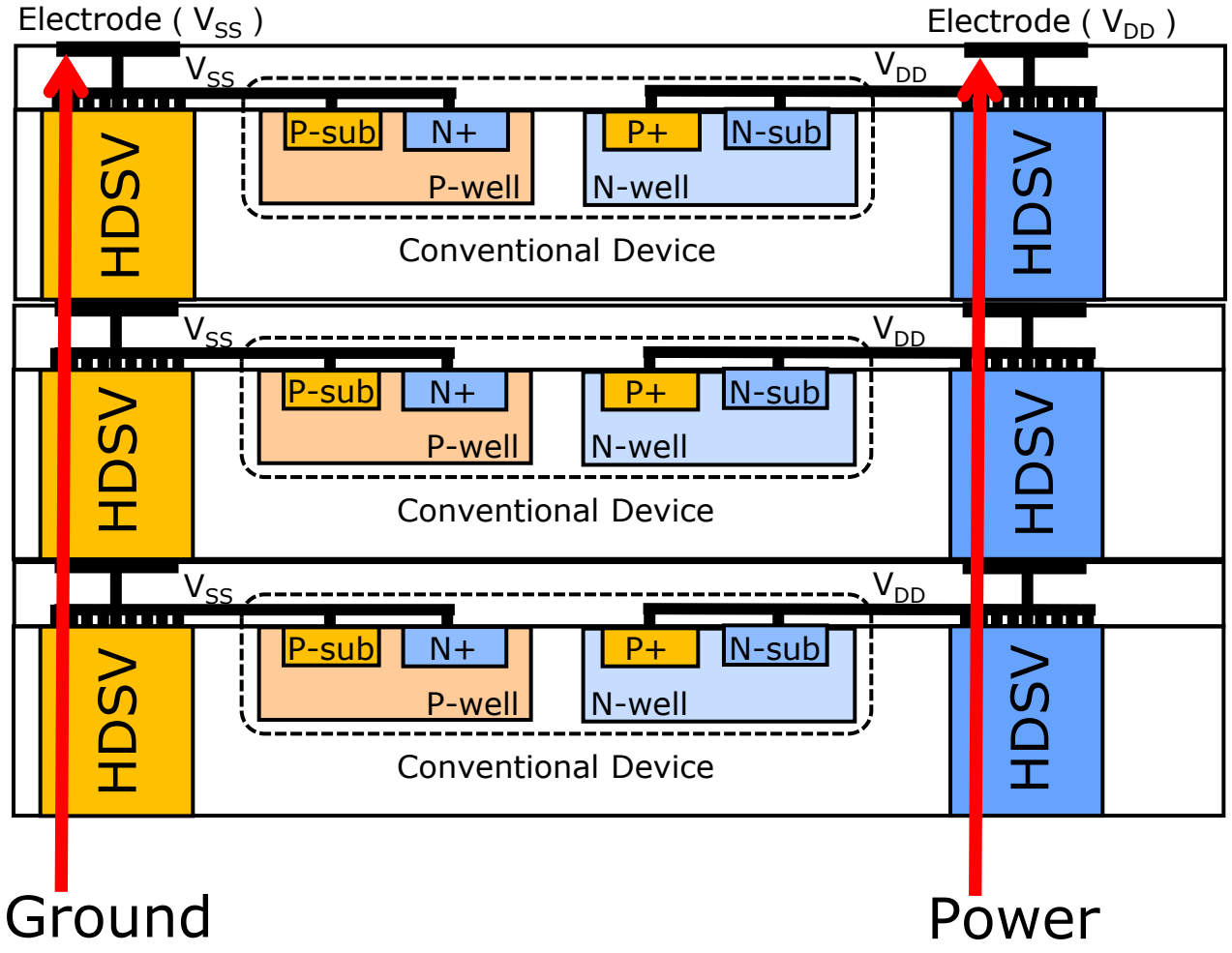
Highly Doped Silicon Vias for power distribution



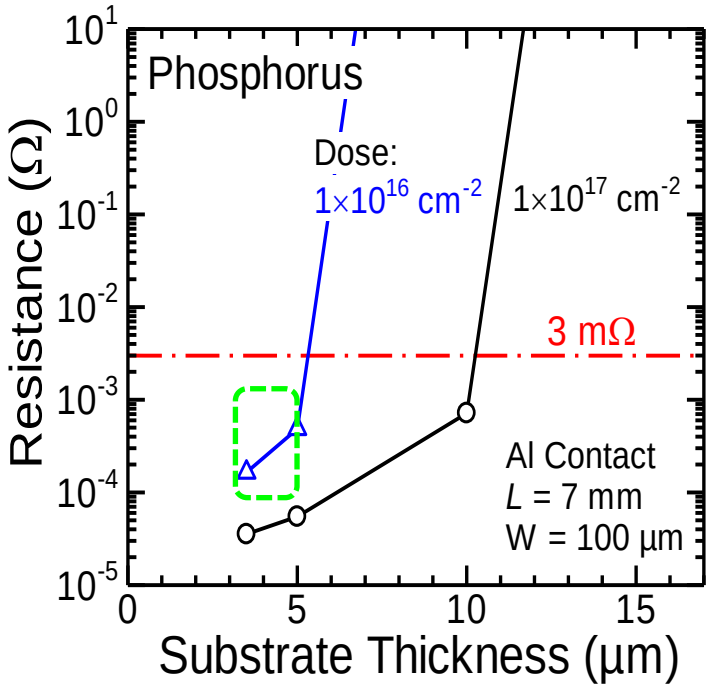
A deeper than normal, and more highly doped well is used to make a low resistance HDSV pathway directly through the thinned wafer using the silicon itself.

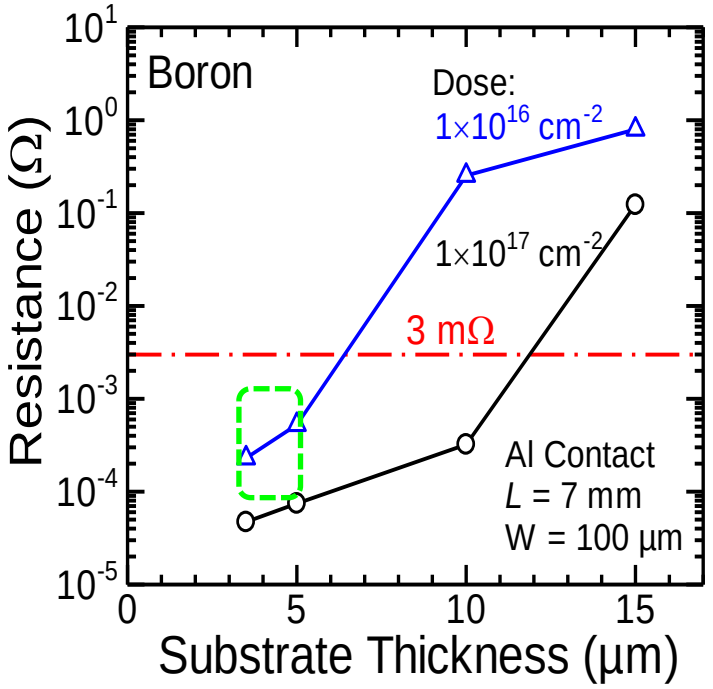
The HDSV on one die and the electrodes on the next die are connected by pressure from a Room-Temperature Wafer Level Bonding machine (solid intermetallic bonding by diffusion) to create larger stacks.

Highly Doped Silicon Vias for power distribution



TCAD modeling: HDSV resistance





- Desire < 3 milliOhms front to back resistance for HDSV with 4µ wafer thickness
- Front-to-back resistance can be made sufficiently low for power distribution
- Dose of 1x10^{16} can be done on conventional implant equipment (about 10x normal)
- HDSV probably not usable for high speed data due to high capacitance, need TCI

HDSV Wireless Power Distribution

- No metallic TSV's, no wire bonds, no solder bumps
- Just stack chips and connect the stack to power
- Very loose alignment requirements on both data and power
- Data transmitted wirelessly with near field inductive coupling
- Power and ground go directly through the silicon, by using high levels of doping on ultra-thin die.
- Since silicon provides the power conduits instead of "metal wires", the power distribution is "wireless" ;-)
- HDSV should be low cost, extra implants are the only change to chips

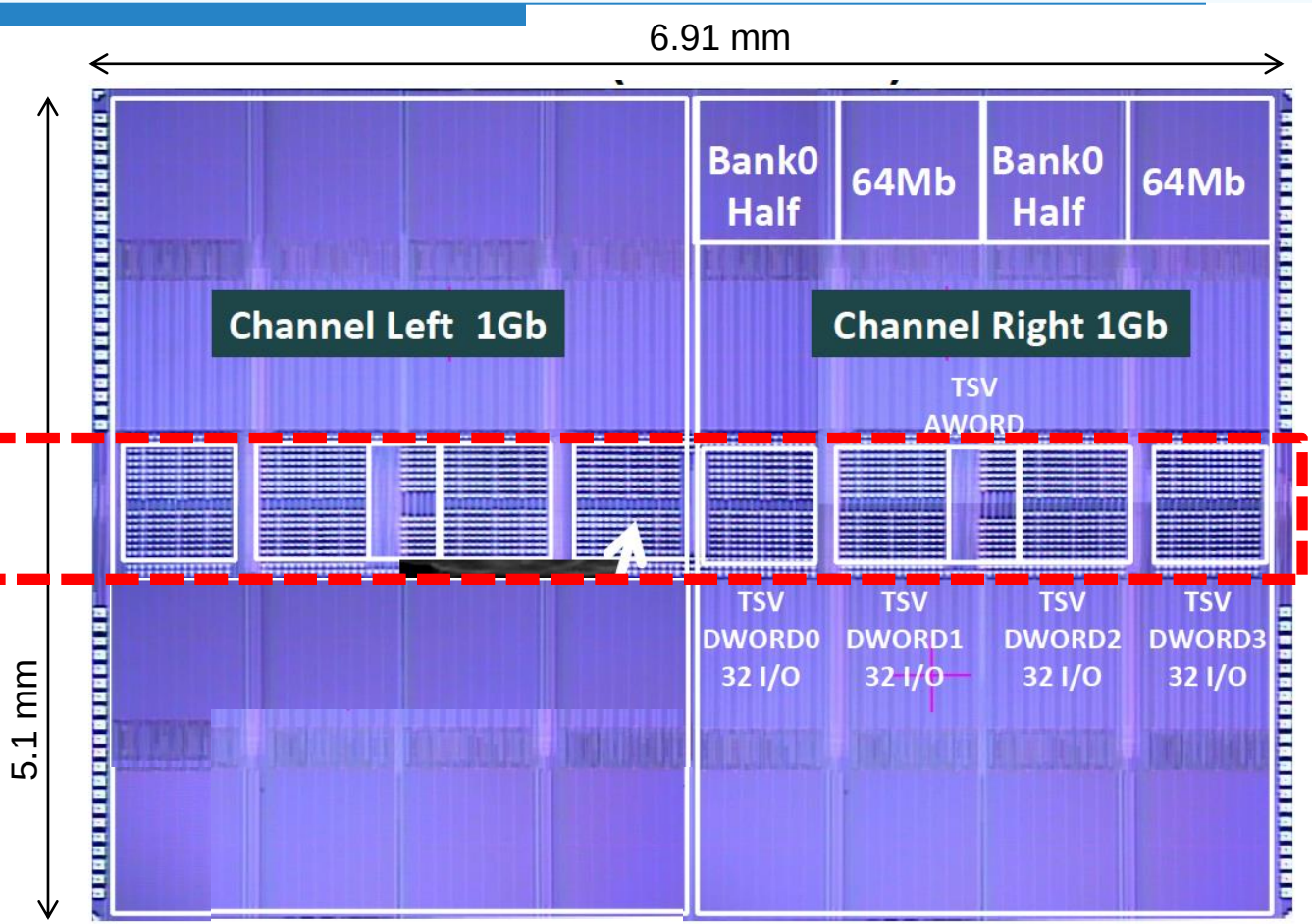
Comparison Example

Stacked HBM DRAM
TSV vs TCI/HDSV

Example HBM DRAM with TSV

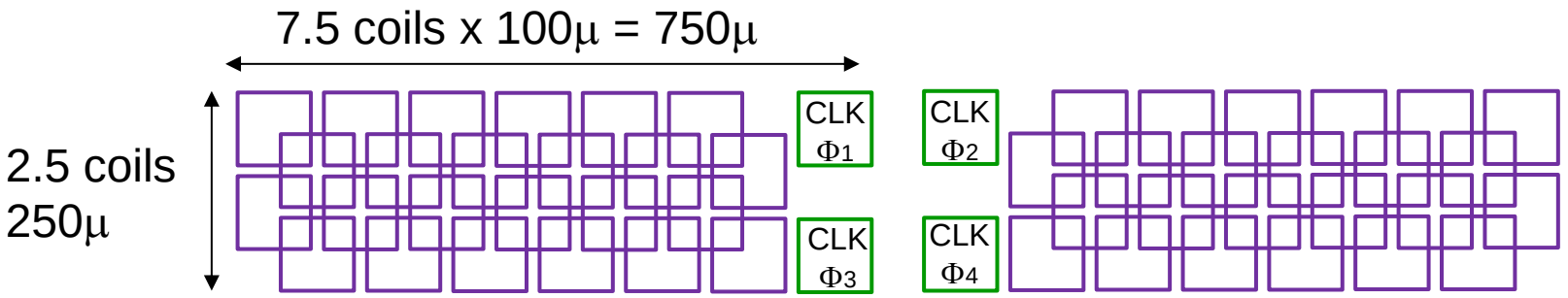
This is a simplified hypothetical example using Hynix HBM as a point of comparison for stacking 5 die.

~ 18% of die area dedicated to TSV IO



TSV's provide 8 channels of independent 128-bit I/O
Total of 1024 TSV I/O at 1 Gbps for 128 GB/s

Replace TSV signals with TCI coils



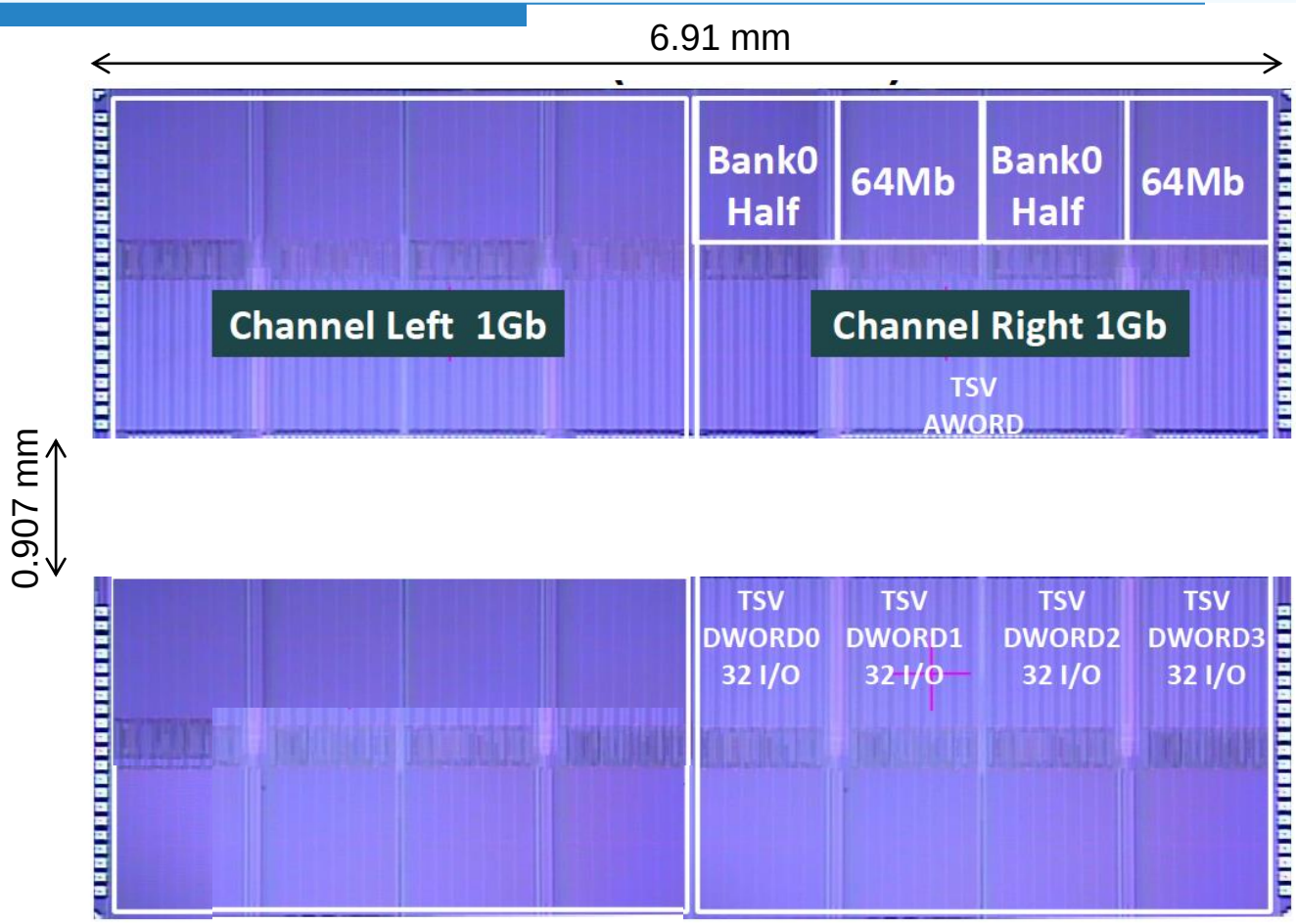
TCI coil layout for two of eight DRAM-channels

Each TCI coil is 100μ x 100μ
Each TCI coil can run at 8 Gbps with slow DRAM transistors

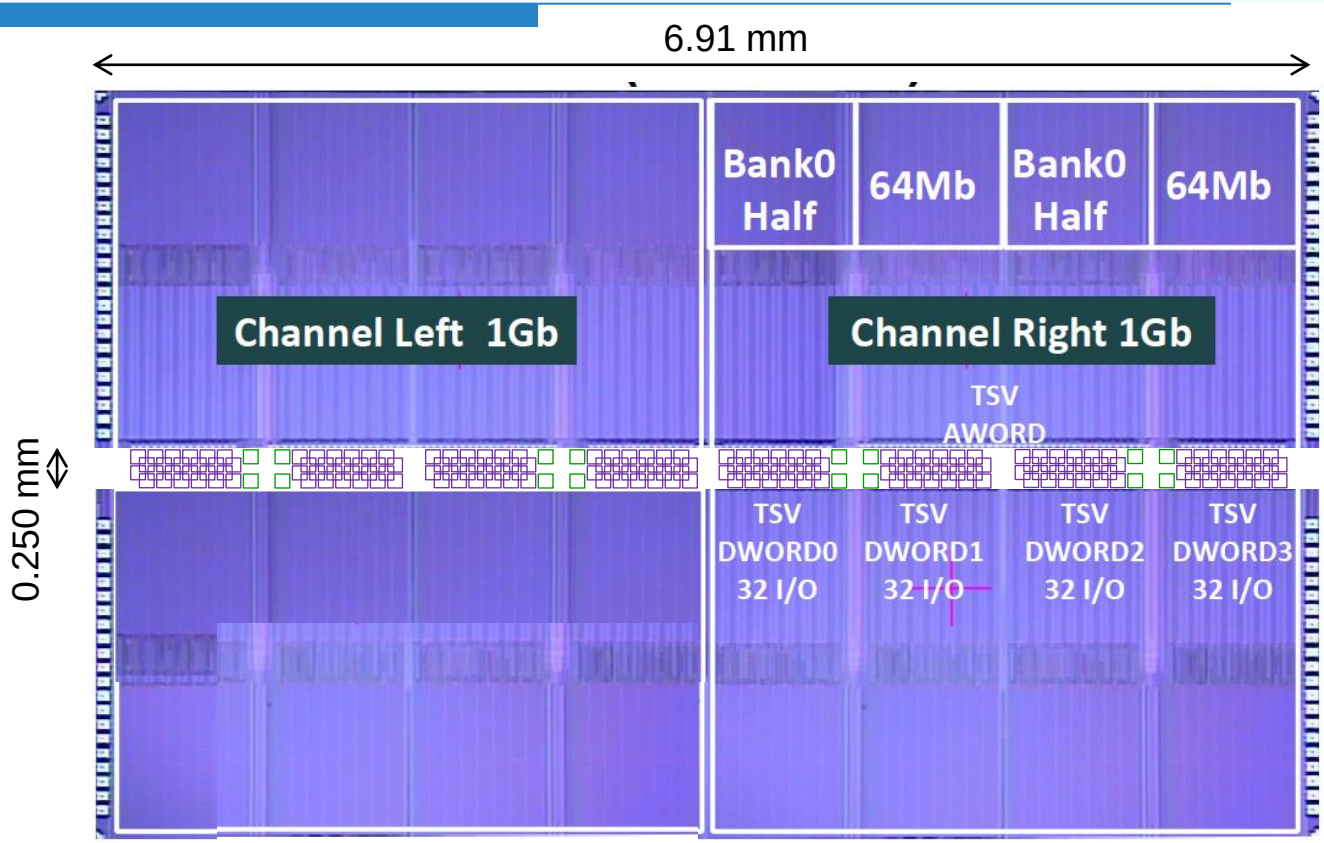
26 coils/DRAM-channel provide the same bandwidth as HBM

- 16 coils for data x 8 Gbps/coil = 128 Gbps / DRAM-channel
- 8 coils for 64 address/control signals
- 2 coils for half of QPDM clocks (4 in a pair)

Remove TSV section



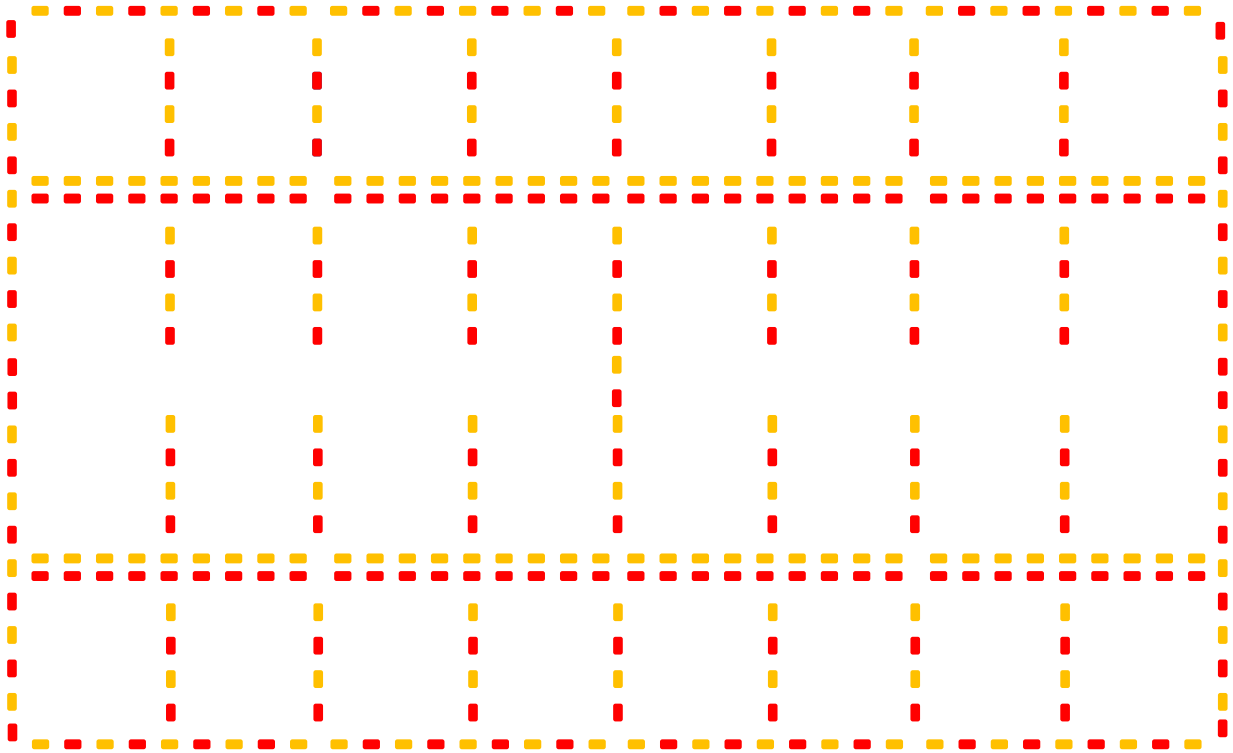
Add TCI IO and shrink die area



Define Power/Ground with HDSV

Vss

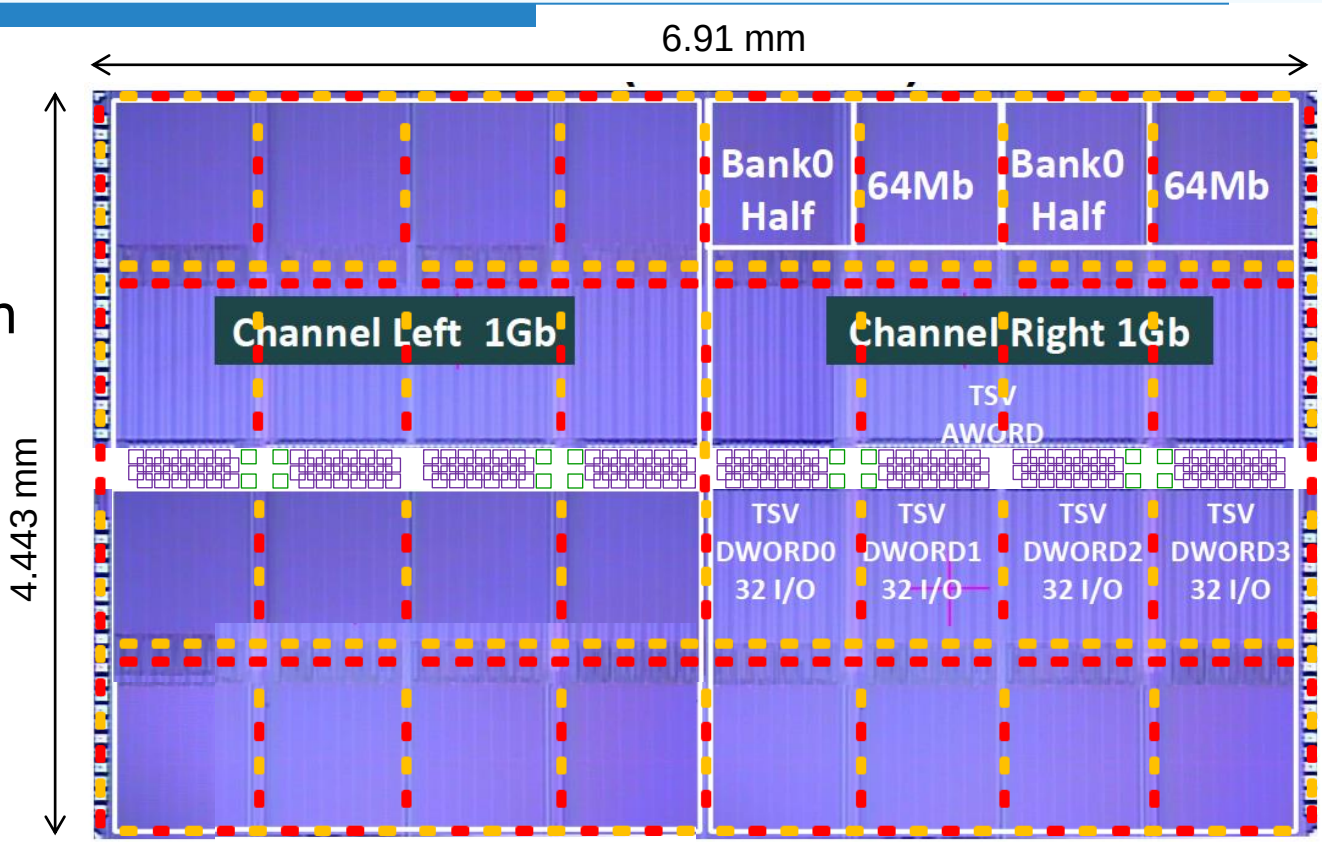
Vdd



These are the mask patterns for low resistance implants for HDSV conduits from the front to back side of each die.

Add HDSV for Vdd/Vss

13% area reduction is a significant cost reduction.

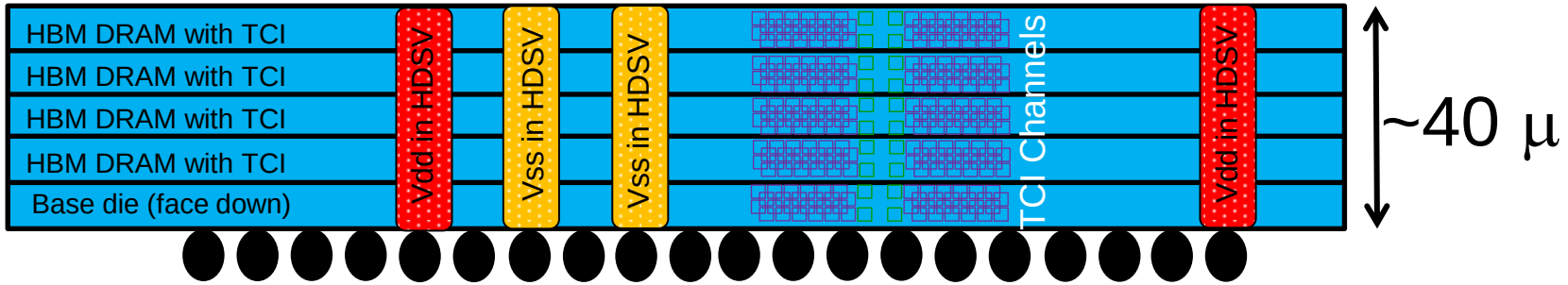


Original die size with TSV = 35.241 mm^2

Die size with TCI & HDSV = 30.701 mm^2

Area savings = 4.540 mm^2, -13%

Final stack DRAM example



Assumptions:

- Each die 8μ thick, 4μ silicon and 4μ metal stack.
- Data sent wirelessly with TCI inductive coupling links.
- Power passes through existing silicon with Highly Doped Silicon Vias.
- Base die can translate to standard IO or TCI link to a SoC.
- Smaller die size provides significant cost reduction.
- Cost of implants for HDSV and circuits for TCI relatively negligible.
- Seems likely this will result in a net cost reduction when using this stacking approach.
- No vertical metal wires! Wireless 3D stacking.

Summary

- The synergy of ultra die thinning, TCI wireless data communication and Highly Doped Silicon Vias for power provides a future path for cost reduction using 3D stacking.
- Wireless TCI near-field inductive coupling has been well proven with 28 silicon test chips.
- Power distribution when using TCI can be done with proven techniques such as wire bond, TAB or even TSV.
- Power distribution for TCI with Highly Doped Silicon Vias is a new and still untested technique, which offers great promise for lowering 3D stacking costs. Help us make it happen.

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