5th Generation Touchscreen Controller for Mobile Phones and Tablets

Hot Chips 2013
Milton Ribeiro
John Carey
August, 2013

CYPRESS
PERFORM

Design Goals

- Quick design of derivatives
  - Platform-based design
  - Scalable analog front-end (AFE)
  - Scalable DSP datapath
  - Flexible hardware platform
- Superior noise suppression performance
  - Display noise: DCV com, AC Vcom, OLED
  - Finger-couple noise (charger noise): > 40 Vpp
- Innovation acceleration thru flexible hardware
  - Glove and hover support
  - Robust water rejection and wet finger tracking
  - Passive stylus support
  - Active stylus support

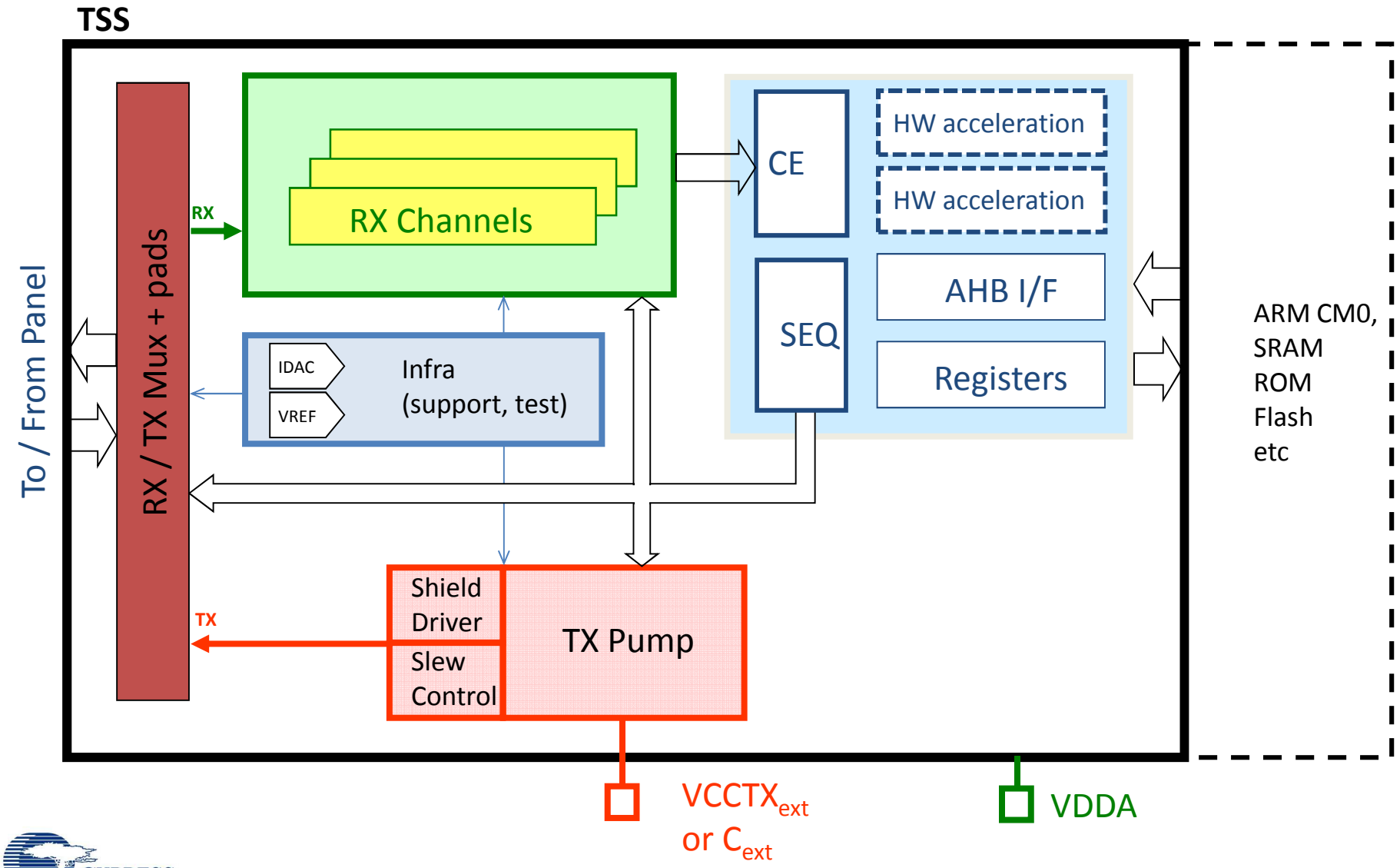
Architectural Elements (I)

- CPU
  - Cortex M0 @ 48 MHz
  - Support for flash memory (scalable)
  - Support for SRAM (scalable)
  - Support for ROM memory (scalable)
- Low-power microcontroller infrastructure
  - Support for Hibernate, Deep-sleep, Sleep, Idle and Active modes
  - On-chip power generation (LDO and voltage pump)
- Robust analog front-end (AFE)
  - Large on-chip integration capacitors
  - Signal attenuators in each channel
  - Large charge handling capability: > 240 pC per cycle
  - High-speed operation: up to 1 Msps

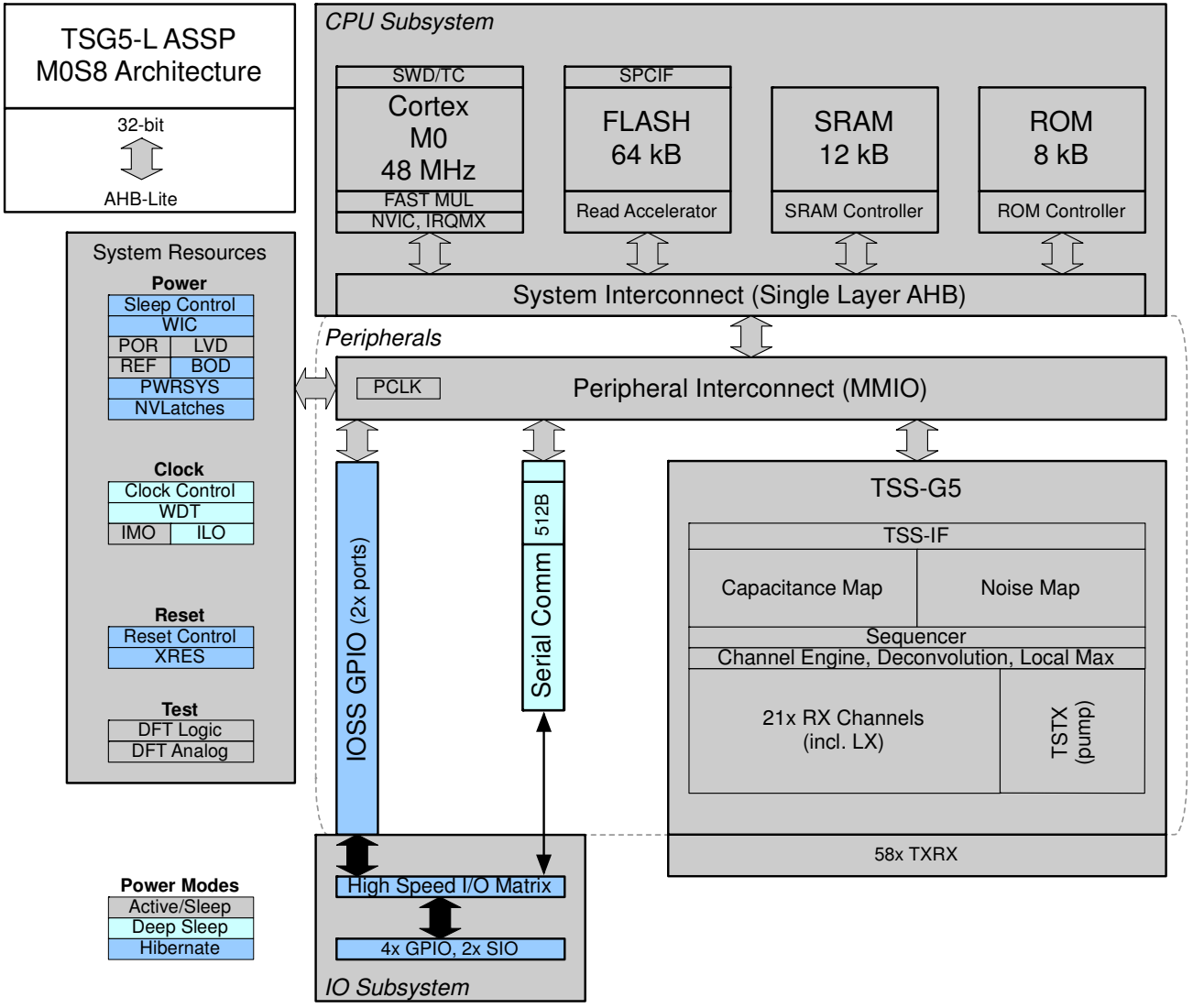
Architectural Elements (II)

- High-voltage signal generation
  - On-chip charge pump for 10V generation
- Configurable DSP datapath
  - Low-power linear and non-linear filtering
    - FIR and window filters
    - Median filtering
  - Digital quadrature demodulation for active stylus
  - Real-time noise-metrics
  - 2D image processing algorithms: filtering, peak-search, etc.
- Table-driven sequencer
  - Flexible timing generation enables advanced scanning modes
  - Easy integration with DDI ASICs for incell and oncell integration

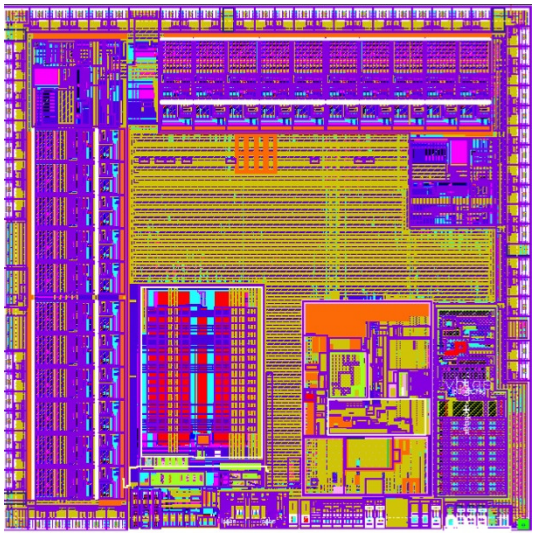
Gen5 Architecture Overview



TSG5_L Touchscreen Controller

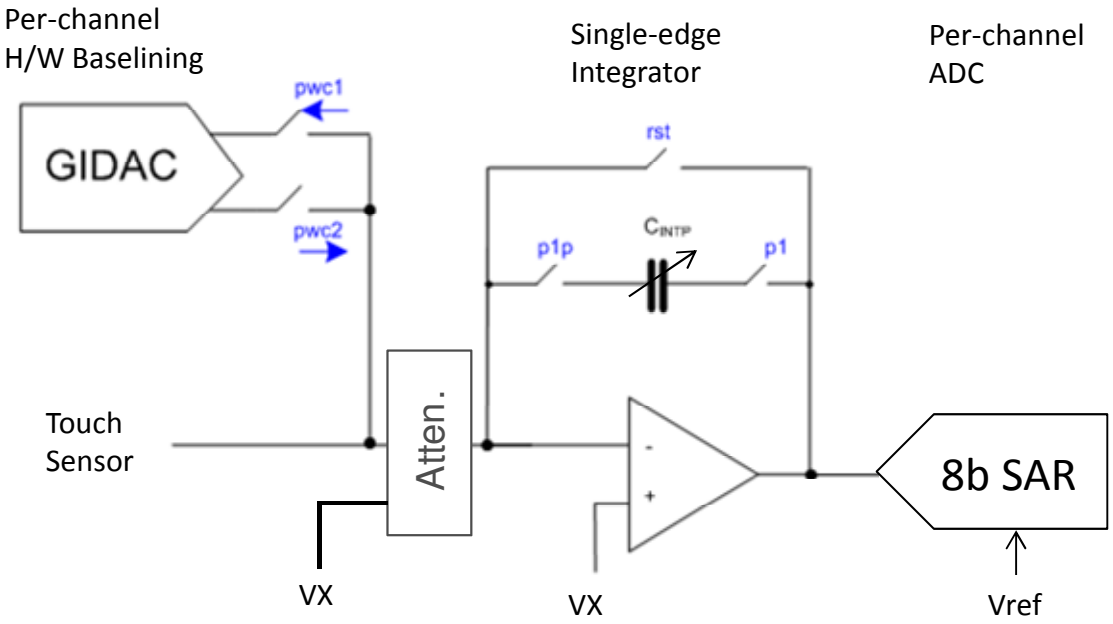


- ARM CM0
- ARM Debug
- Low power
- CY S8 Process
  - 130nm
  - FLASH
  - 10V capable



TSG5 RX AFE Architecture

Per-edge signal processing, 40V charger noise



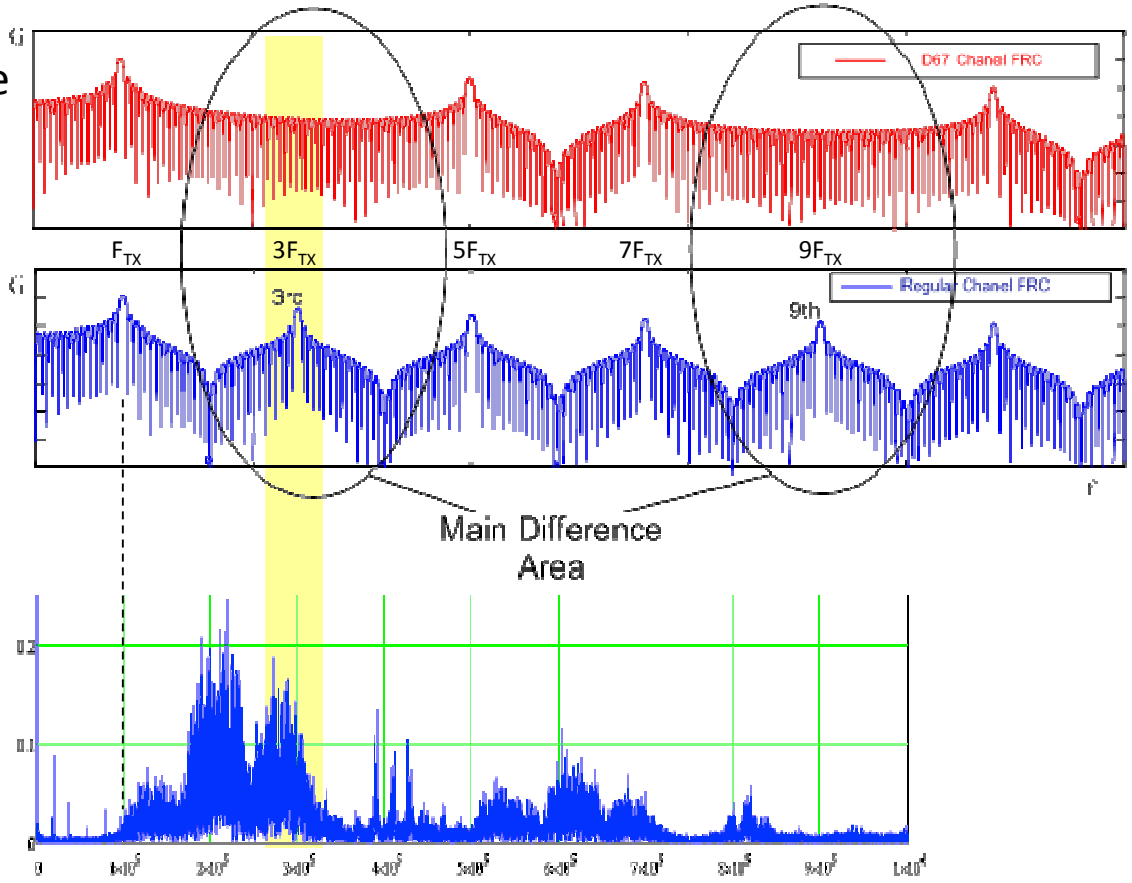
Gen5: Application of Flexible Timing Generation

- D67 = integrate for 2/3 of the period, or 67% duty cycle
  - Removes 3rd/6th/9th harmonics, e.g. for F_{TX}=100kHz that's 300/600/900kHz
  - Esp. effective for slow panels. 1.5x noise immunity for all the higher-freq noise

Channel response @ F_{TX}=100kHz With D67

Without

Duracell Charger



Gen 4/5 Comparison

Feature	Gen 4	Gen 5
TX drive (square wave)	2.6-10V	2.6-10V,C_{ext} or V_{TX}
MPTX	4	Full axis
TX frequency	≤ 300kHz	≤ 500kHz
Max RX sample rate	≥2 TX (sub-int)	½ TX (=per edge)
HW Baseline Cal.	Yes	Yes, larger
Max RX charge	8pC/edge	30..200pC/edge
RX ADC	10b SAR, shared	8b SAR per ch.
LX channel	Yes	Yes
LCD sync	Int/ext	Int/ext
Signal processing	M0 CPU, 32b	CPU or CE
Noise metric	CPU	CPU or CE
Autom. sequencing	Yes	Yes, table driven
Self & Mutual Cap	Yes	Yes
V_{DDD}	1.71 – 5.5V	1.71-5.5V
$V_{CCA\ (core)}$	2.4V	2.65-5.5V

Current Status and Future Developments

- Smartphone and tablet devices available **today**
  - TGS5_M: 36 I/Os and 11 channels, supporting phones up to 4.7”
  - TSG5_L: 58 I/Os and 21 channels, supporting phones and tablets up to 9”
- Large tablet and notebook device available later in the year

Thank You

mrib@cypress.com
jonc@cypress.com