NAND Technology

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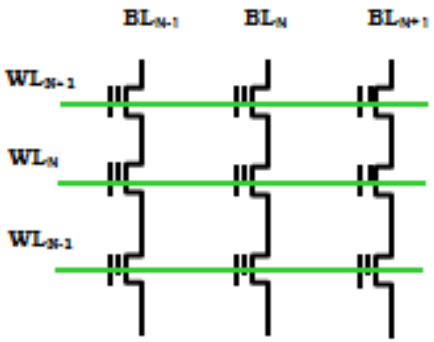
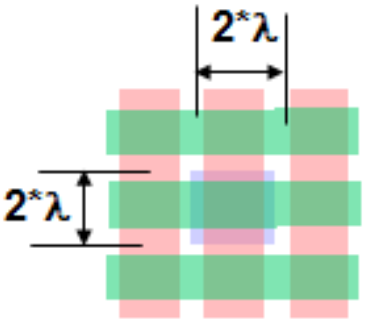
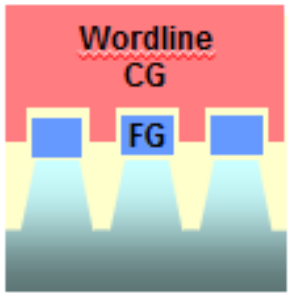
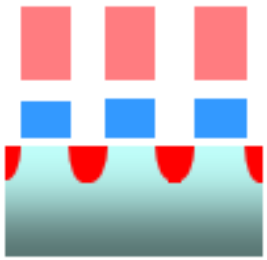
NAND Flash

- Key Attribute: Non-volatile memory, Read access times of 10's of us, Write/ Erase times of ~ms, Page Programming, Block Erase, 10's of K cycles W/E endurance
- Key applications: Data Storage, SSDs
- NAND has a simple cell and array structure
- NAND Flash has been leading in driving the Semiconductor technology scaling → low cost leader

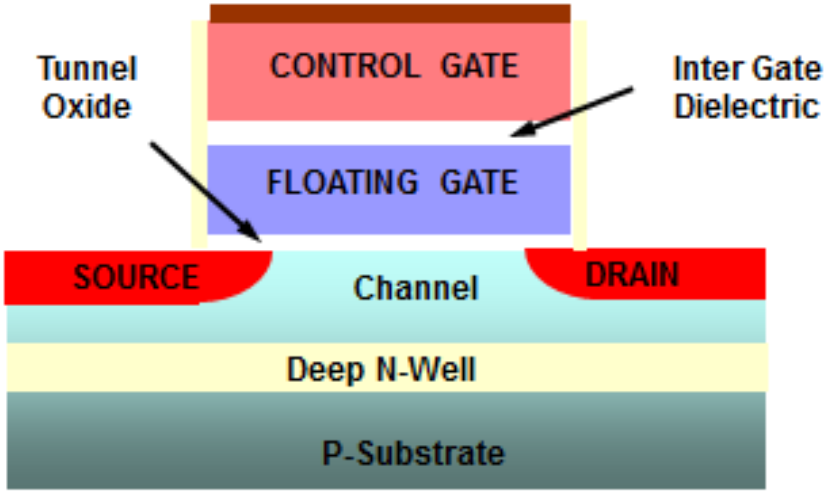






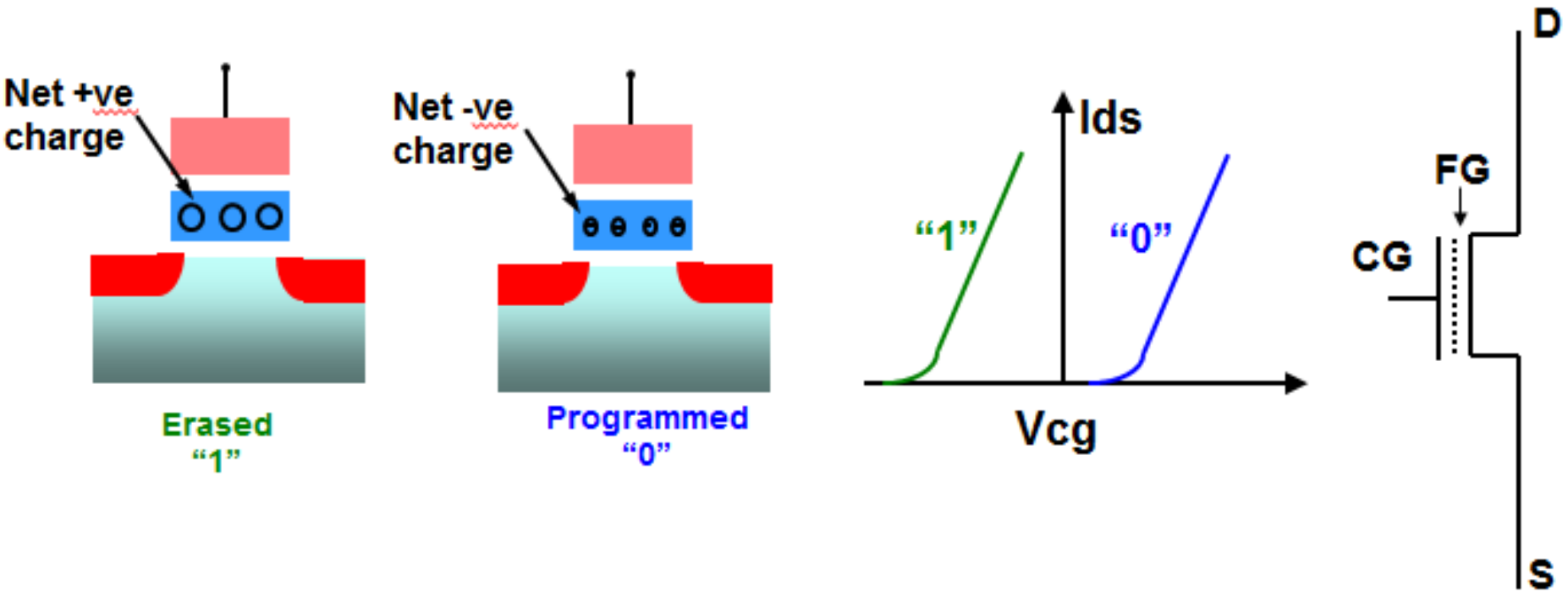


Floating Gate Flash Memory Device



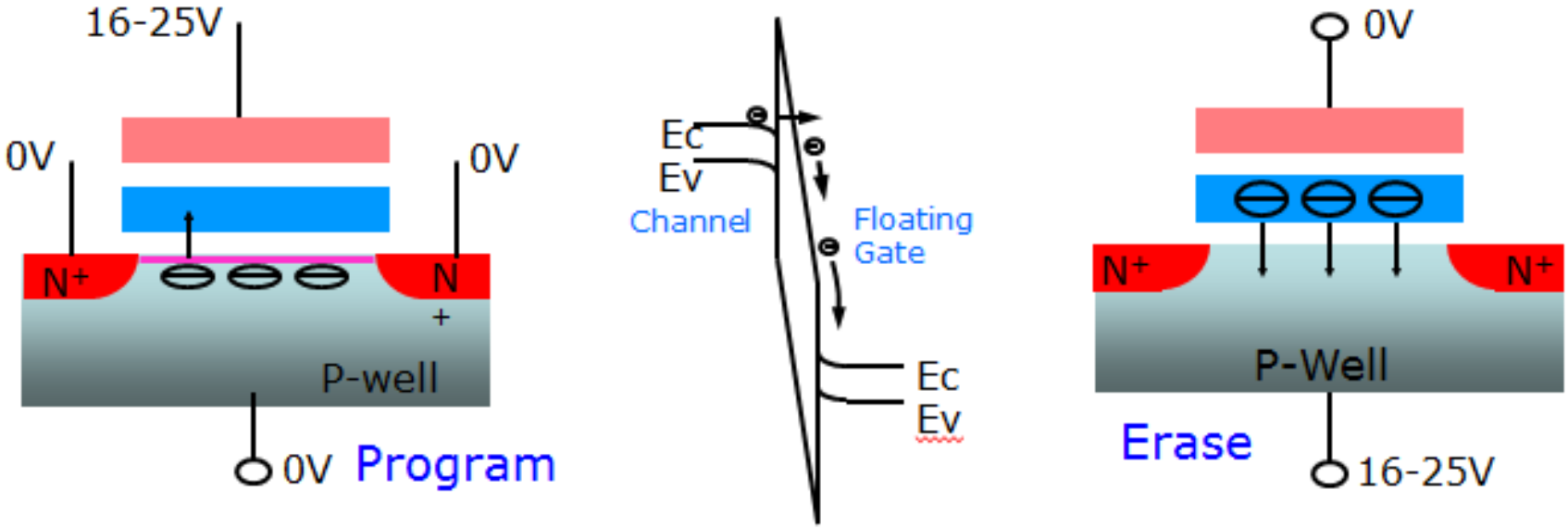
- Stacked Gate NMOS Transistor
  - Floating Gate for charge storage
  - Control Gate for accessing the transistor
  - Silicon dioxide for gate oxide (Tunnel oxide)
  - Oxide-Nitride-Oxide (ONO) for the inter gate dielectric

Flash Memory Cell



- Program = Electrons Stored on the Floating Gate → High Vt
- Erase = Remove electrons from the Floating Gate → Low Vt
- Read = Look for current through the cell at given gate bias

NAND Flash Program/Erase

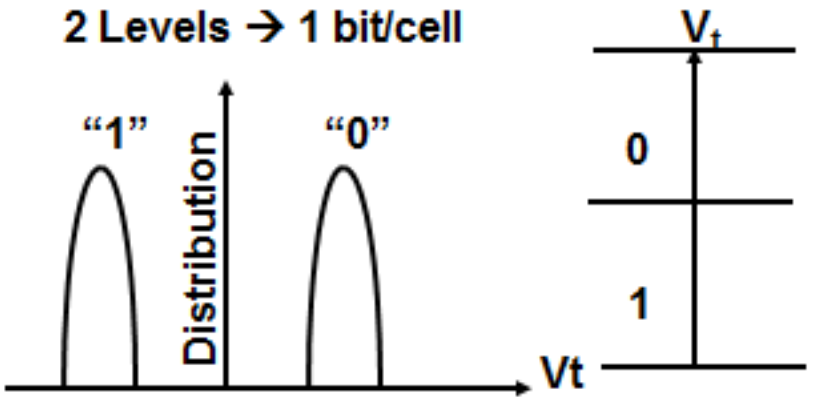


- Programming is by tunneling electrons through the Tunnel-ox by applying a high gate voltage and grounding well & Source/Drain.
- Erase is by tunneling electrons through the Tunnel-ox by applying a high Well voltage and grounding the gate.

Multi Level Cell

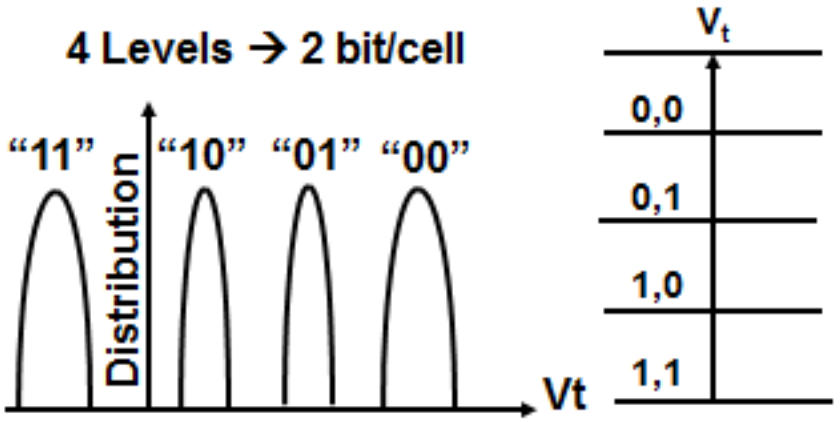
1 bit/cell: 2 states:

- Level 0 = Erased
- Level 1 = Programmed



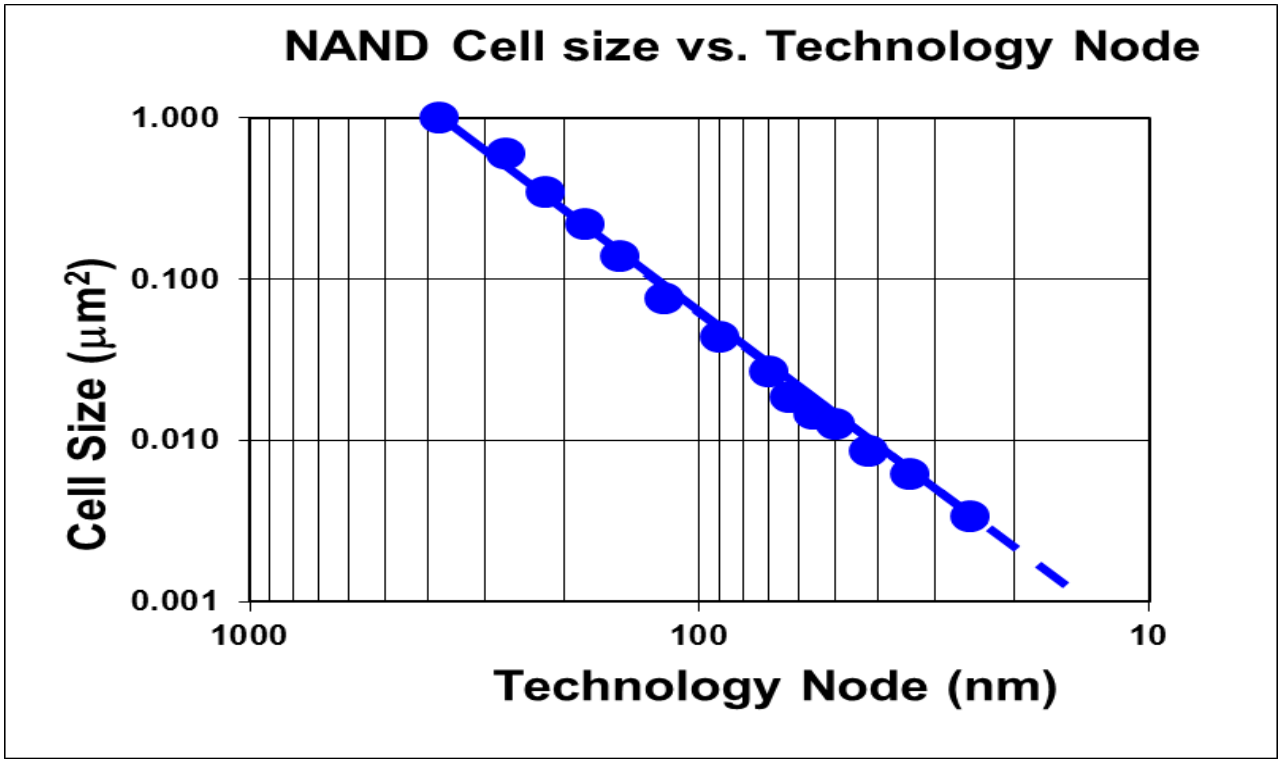
2 bits/cell: 4 states:

- Level 0 = Erased
- Level 1 = Programmed to L1
- Level 2 = Programmed to L2
- Level 3 = Programmed to L3



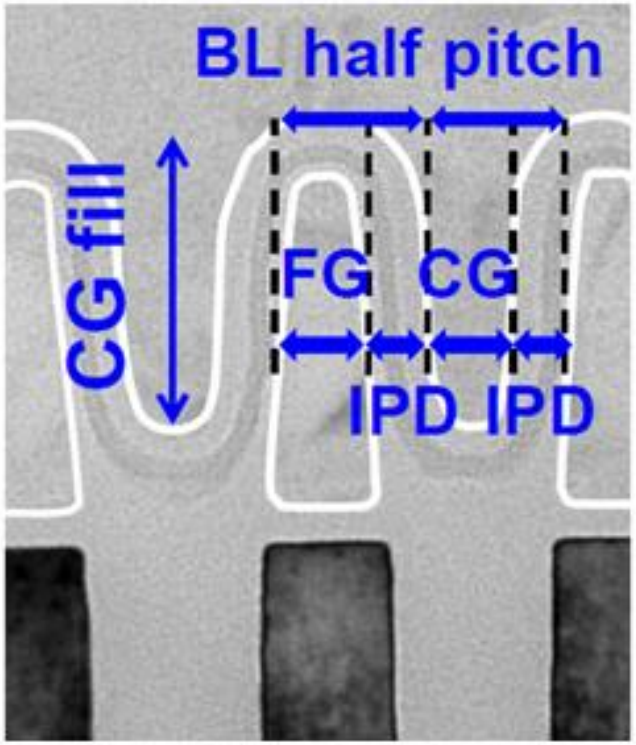
Having the threshold voltage of the cells defined to 2^n different levels allows for storing n bits per cells

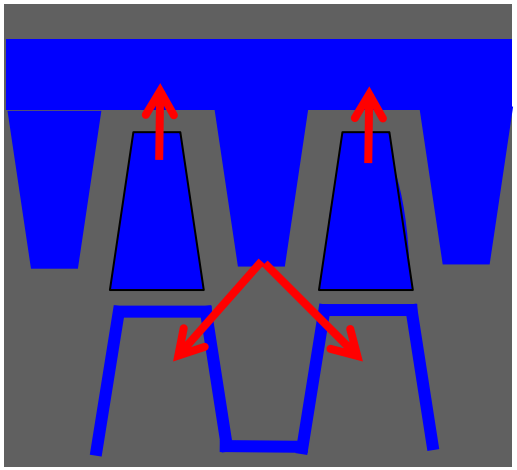
Technology Scaling

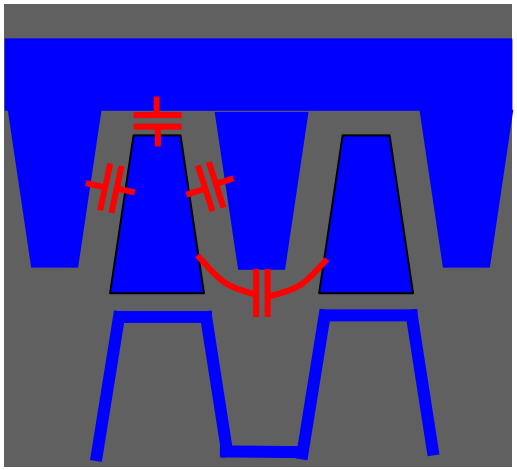


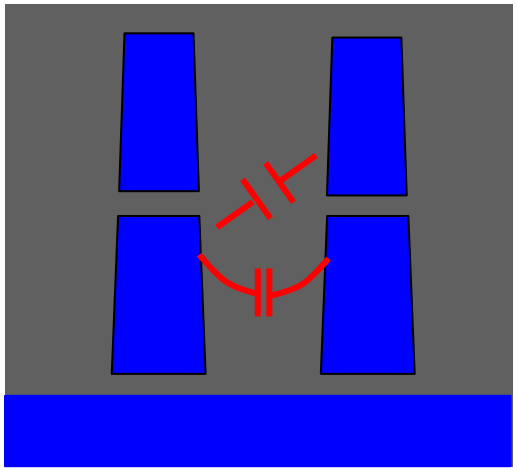
- Retention limits the dielectric scaling and Pgm/Ers voltage have remained high around ~20V
- Yet cell area has scaled per Moore's law prediction into the mid 20nm without much difficulty

NAND Cell Scaling Issues At ~20nm



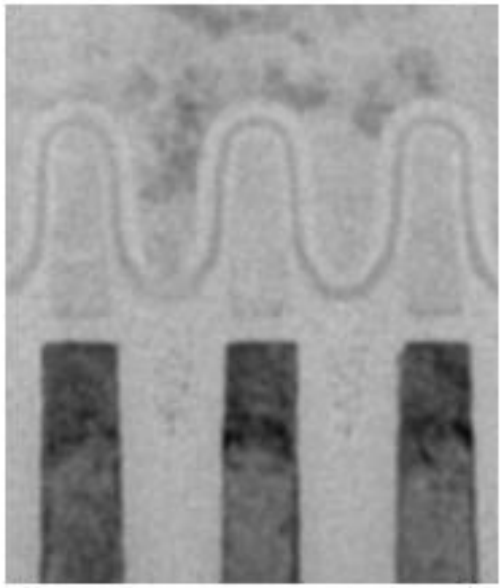


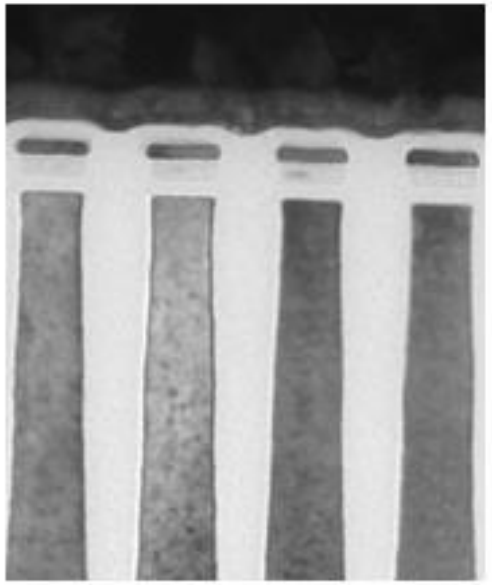


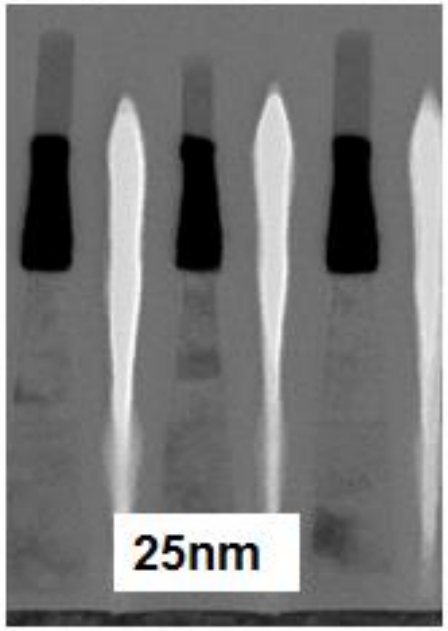


- Significant structural complexity as "wrapped" cell scales to 20nm half-pitch
- High E field issues are exacerbated in the "wrapped" cell with scaling
- Interference concerns with the wrapped cell

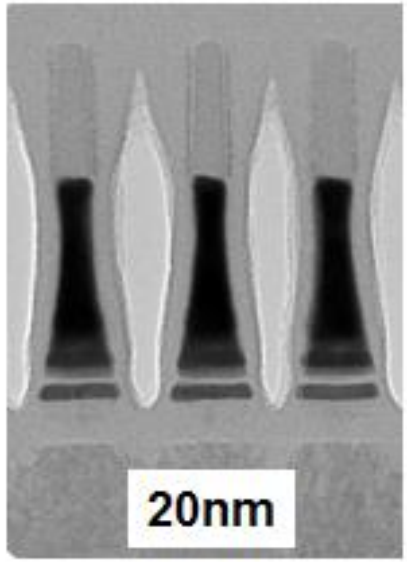
Planar FG Cell For 20nm And Below



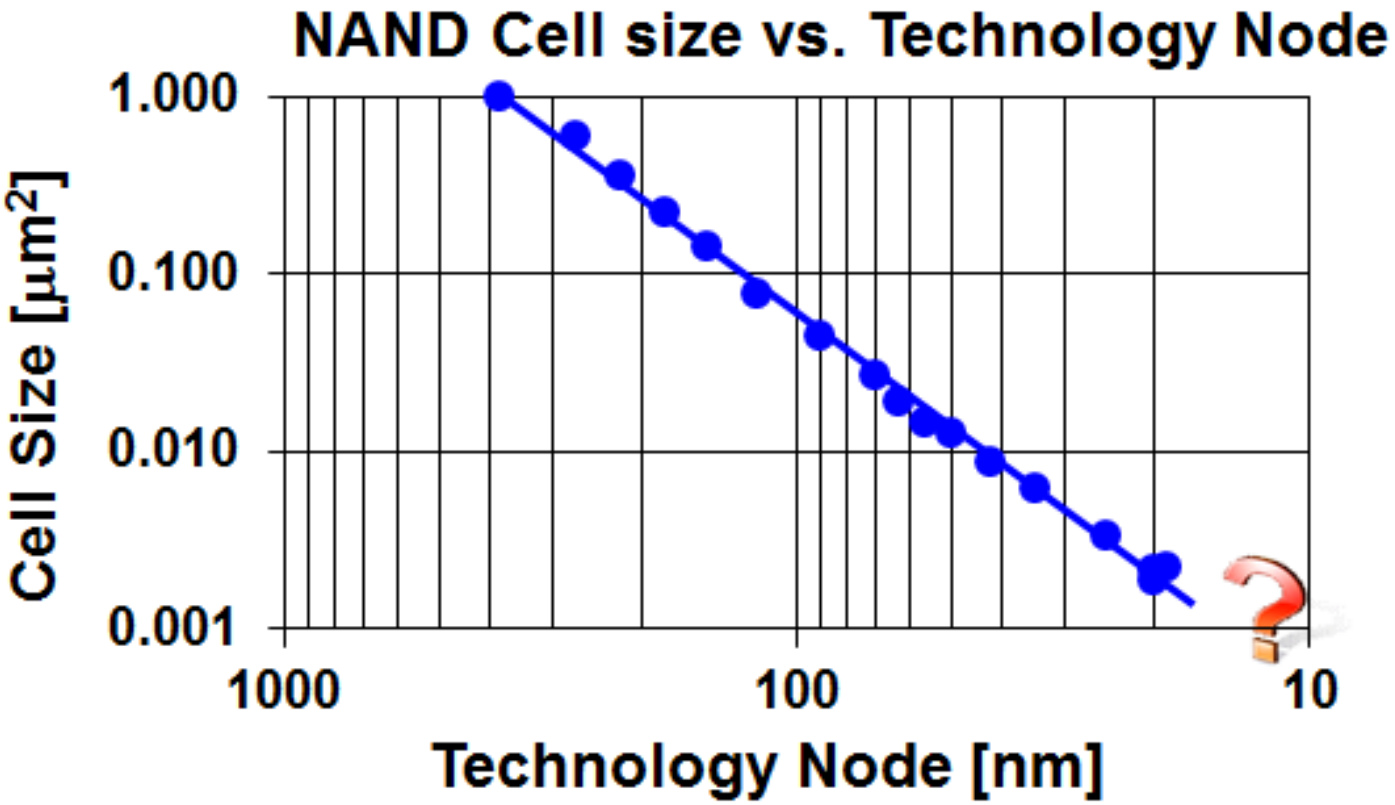




Planar Floating Gate Cell with Hi-K/Metal Gate successfully overcomes the scaling hurdle for 20nm and beyond

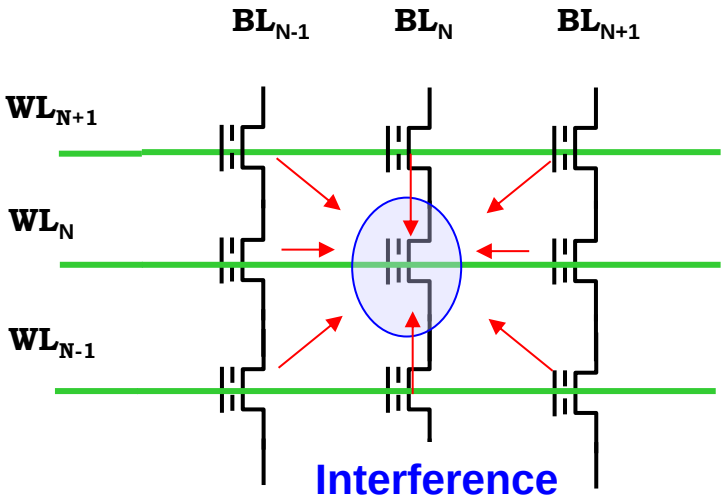


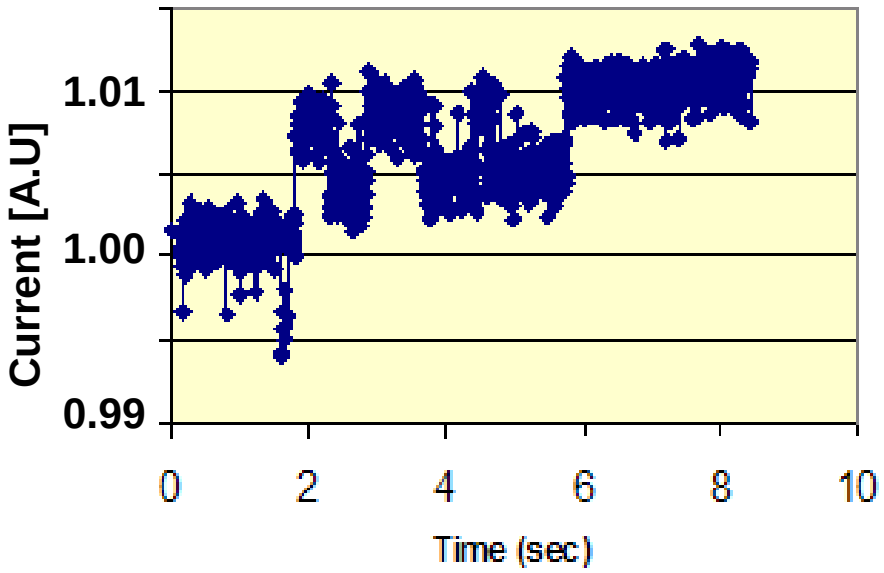
NAND Cell Scaling



- 2D NAND cell scaling has reached below 20nm
- The planar cell structure addresses many of the scaling issues with the scaling of the conventional scaling
- So, how does the future of scaling look?

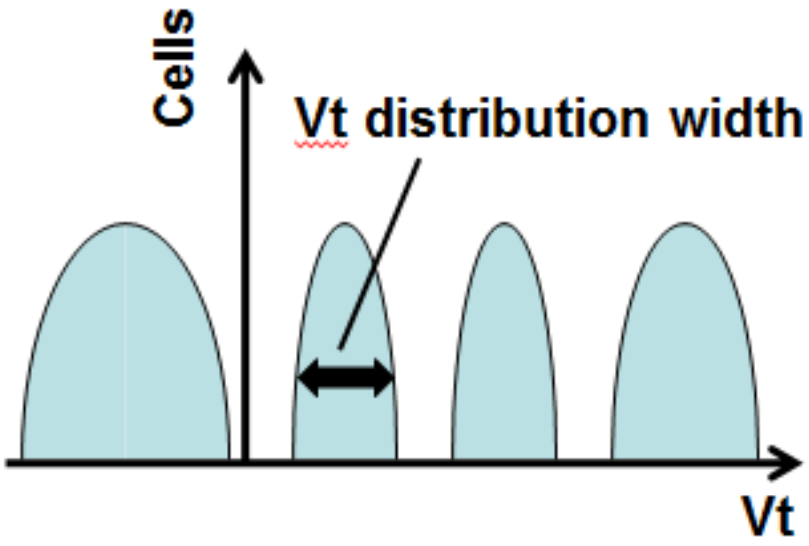
Scaling Effects

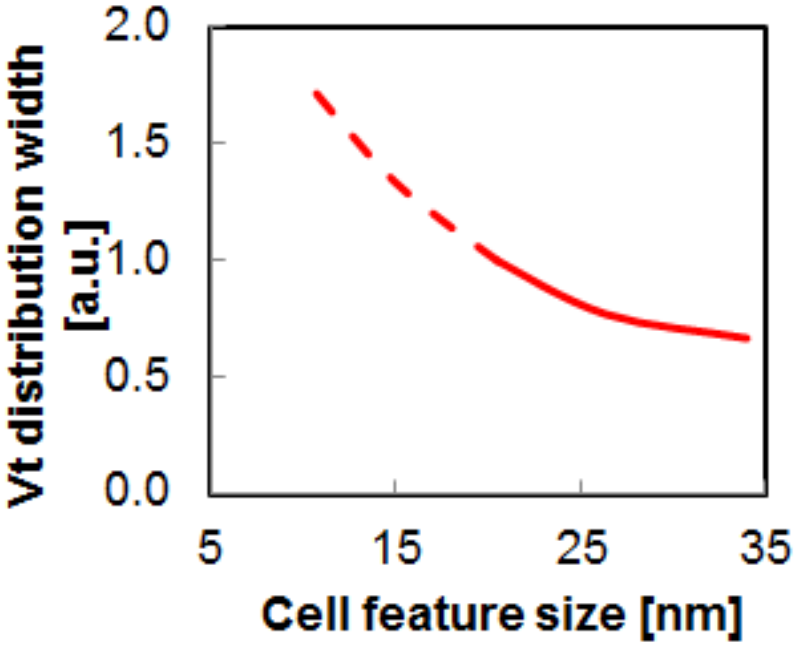




- As the cell dimensions scale:
  - Increased proximity leads to higher coupling to neighboring cells
    - interference from neighboring cells
  - Cell capacitance and hence number of electrons scale.
    - Higher impact of single electron events
  - The channel area scales.
    - Higher impact of 1/f noise
  - Less number of dopant atoms in the channel
    - Larger spread in native Vt due to doping fluctuations

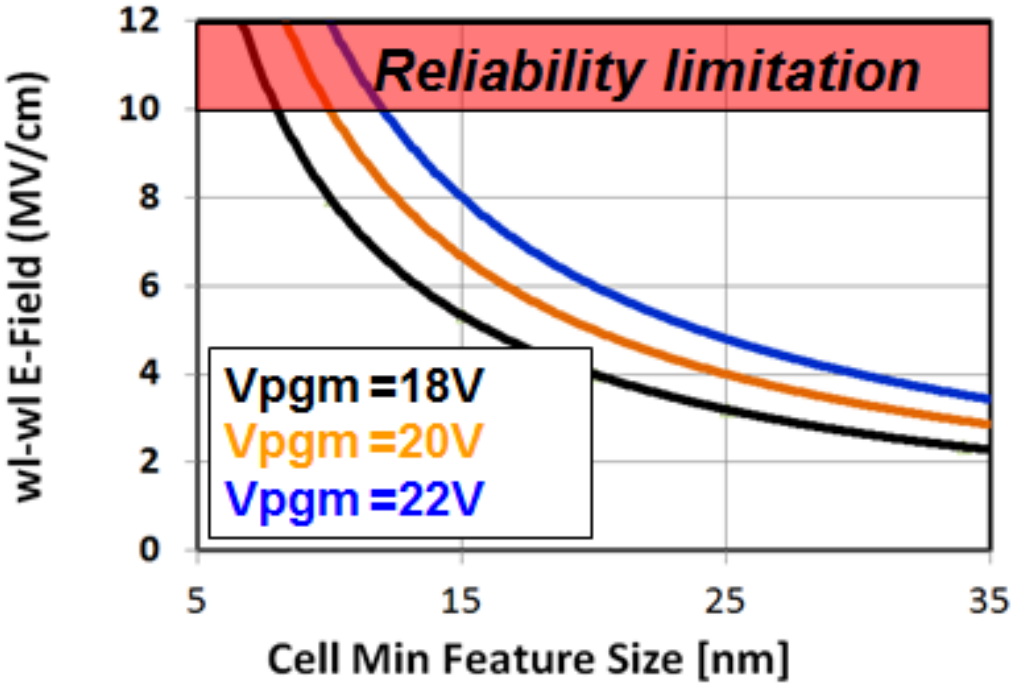
Vt Distribution Widening

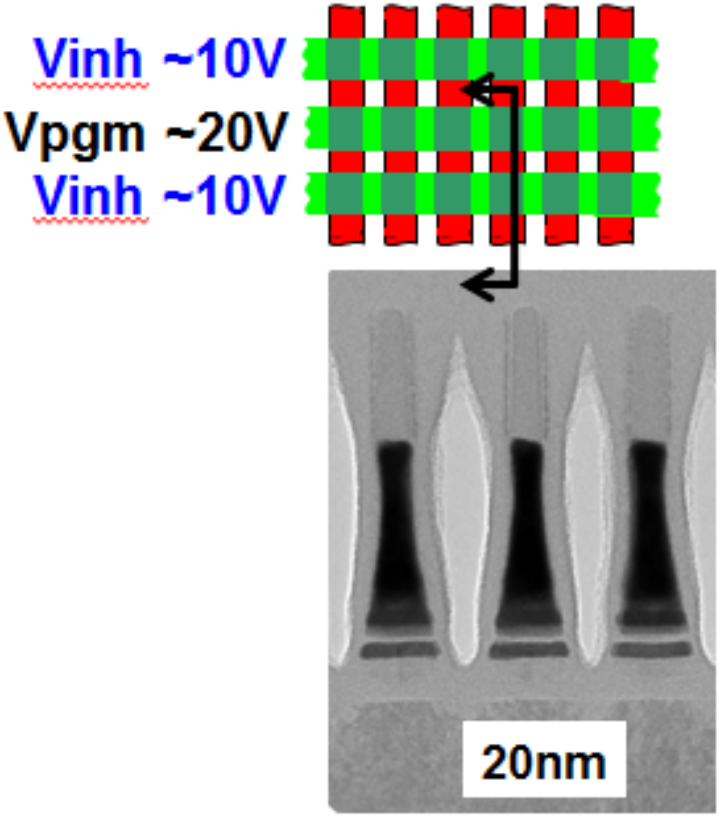




- As the physical cell size is scaled these parasitic issues – interference, single electron effects, trapping/de-trapping, disturbs, distributional effects – become worse
- Continued degradation in Vt distribution width from cell scaling will eventually become unacceptable

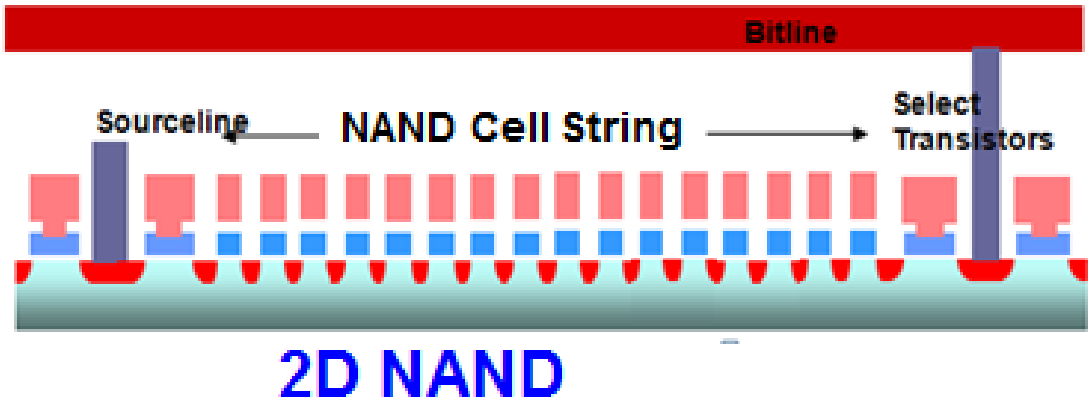
Voltage Scaling

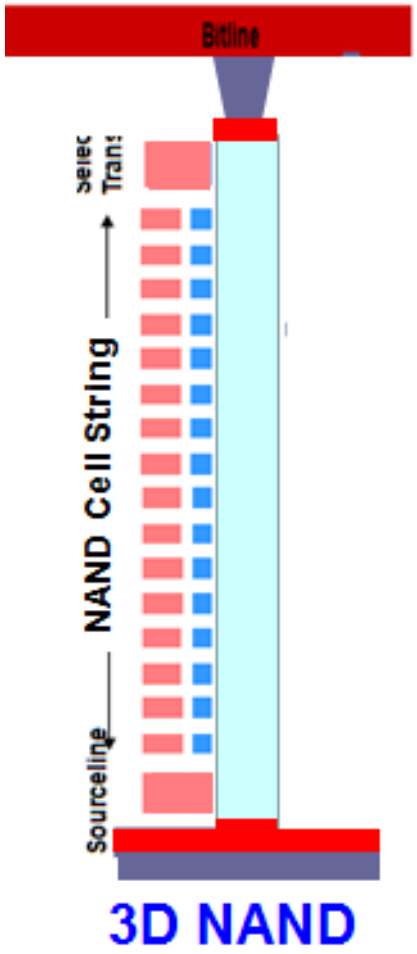




- Program/Erase voltages ~20V
  - ➢ Large voltage + small pitch = Reliability risk
  - ➢ At ~10nm, WL-WL Electric field ~10MV/cm

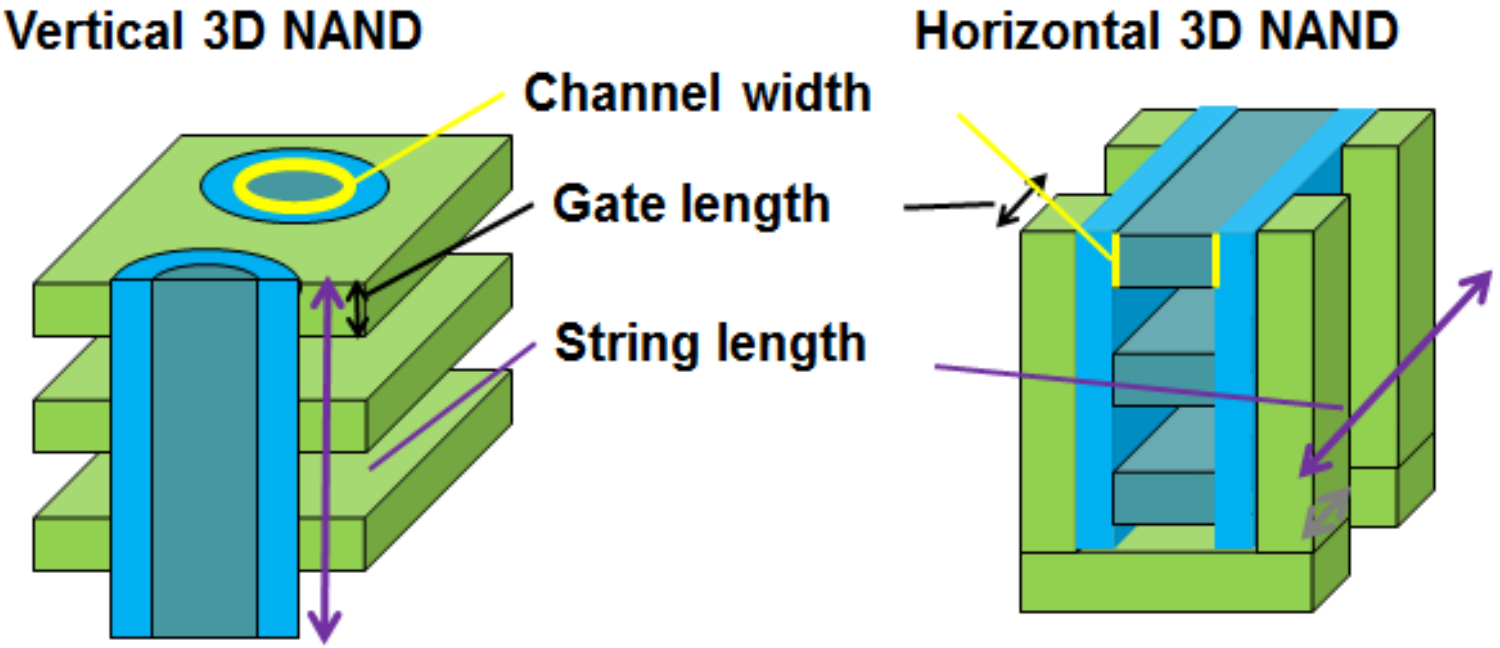
2D NAND → 3D NAND





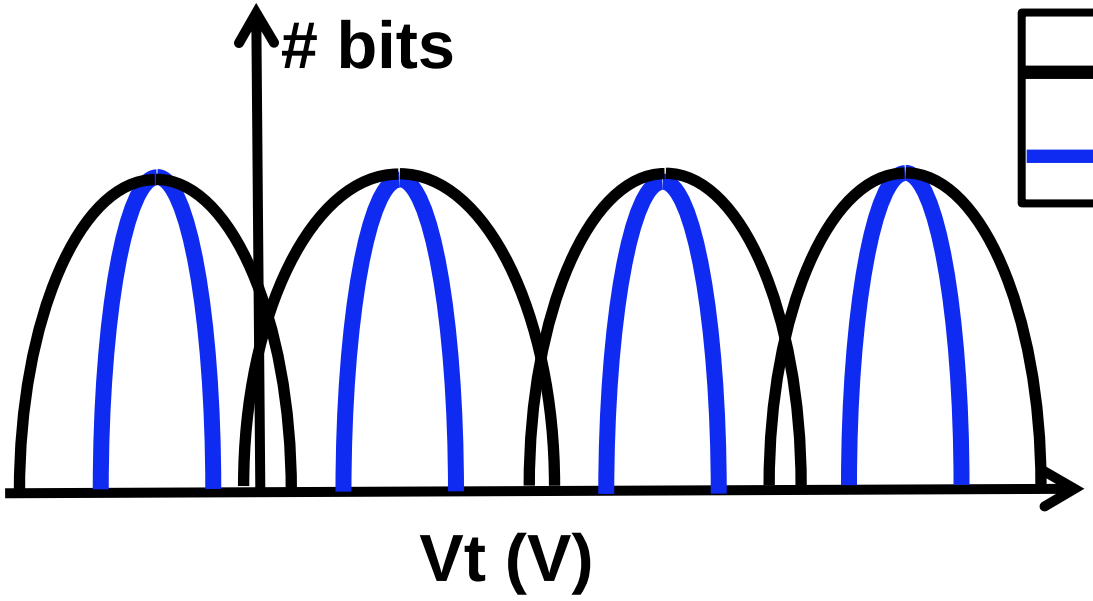
- Vertical NAND string
- Conductive or dielectric charge storage node
- Deposited poly-silicon channel
- Large foot-print of the 3D Cell will require quite a few layers to be stacked to achieve effective cell area scaling
- Increased demands on process technology – very high aspect ratio etches and fills

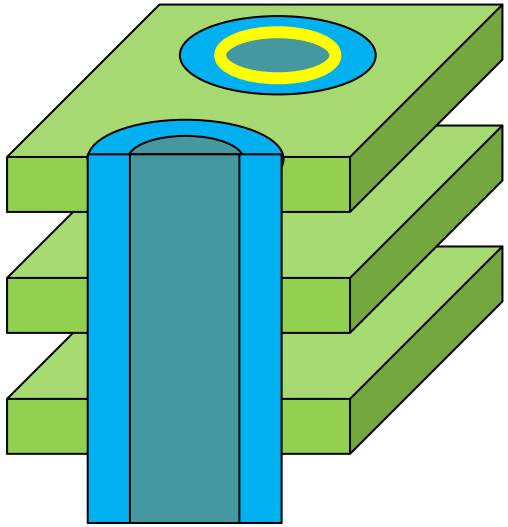
3D NAND Options



- Competing 3D Cell structure options exist:
  - Vertical String vs. Horizontal String
- Vertical string is more attractive for electrical properties
- Horizontal string is more attractive for cell size
- Either case will lead to increased block sizes

Vertical NAND MLC Scaling Benefit





- Vertical NAND String:
  1. Relaxes lithography constraint
  2. Relaxes voltage scaling constraint
- Larger physical cell size means less parasitic effects
- Channel quality and dielectric integrity must be engineered

➢ **Potential for preserving MLC window while scaling cost**

Summary

- NAND Flash has a simple array structure which has been highly amenable to scaling
- NAND Flash leads the industry in scaling
- Lithography induced scaling limits were overcome using advanced pitch reduction techniques
- Interference issues were contained through incorporation of air-gap at critical locations
- Wrap cell limits were overcome with planar FG cell using High-K dielectric / Metal gate
- 2D scaling can continue into the mid to low ~10nm
- Scaling beyond can come from transitioning to 3D

Acknowledgements

- I would like to thank the members of the Intel & Micron NVM team for helpful discussions as well as contribution to the material presented here