A Scalable 3D Heterogeneous Multi-Core Processor with Inductive-Coupling ThruChip Interface

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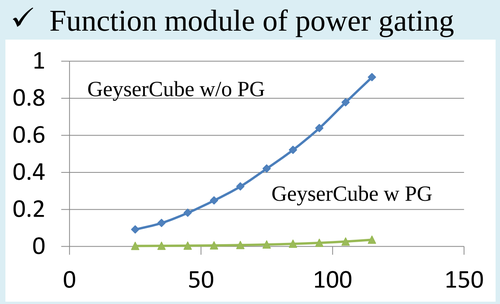
Introduction

Recent battery driven IT devices including smart phone and tablets require versatile functions and high performance with low energy consumption. On the other hand, the initial cost of LSI for design and mask development has increased rapidly, and development of an SoC (System-on-a Chip) for each product has become difficult. Although flexible reconfigurable architectures can be a solution, the performance scalability is also necessary to cope with the wide performance range of products. As a solution, heterogeneous multi-core system using a 3-D wireless inductive coupling interconnect is proposed. This system consists of a MIPS-R3000 compatible embedded CPU and reconfigurable accelerators. Since chips are connected with wireless inductive coupling channels, the number and types of accelerators can be tailored easily depending on the requirement of the product.

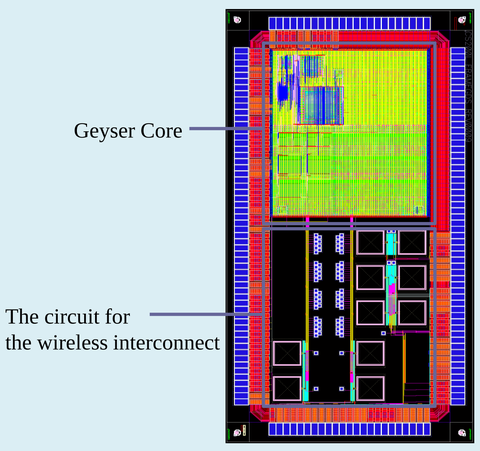
Cube: a scalable 3D heterogeneous multi-core processer with inductive-coupling thruchip interface

Geyser Core

- ✓ MIPS-R3000 compatible CPU core
- ✓ 8KB instruction/data cache
- ✓ 16 entry TLB
- ✓ CoProcessor0
- ✓ Function module of power gating



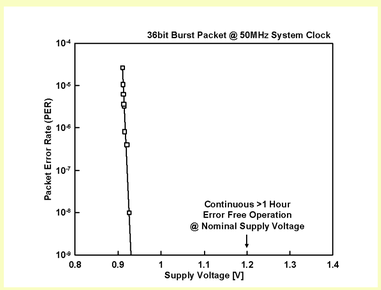
GeyserCube Leakage Reduction



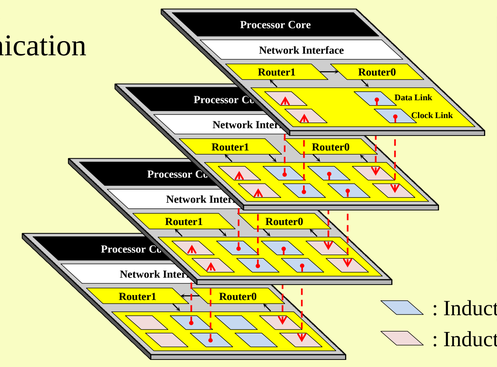
Layout of Geyser-Cube

3D Interconnect

- ✓ Routers for topology free NoC with bubble flow control
- ✓ Inductors for the wireless interconnect
  - High speed communication
  - Stable and reliable communication



Bit Error Rate



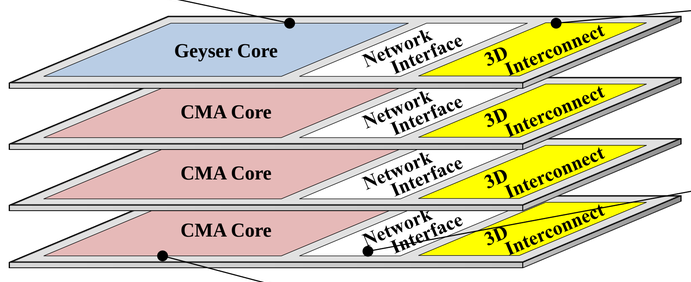
Structure of NoC with wireless interconnect

Chip Stacking Method

- Chips are stacked with a certain length of gap
- The gap can be used for bonding wires to supply voltage, ground and system clock
- A unidirectional ring packet switching network is formed

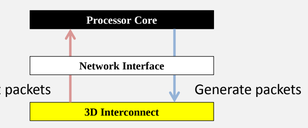
The host CPU chip, Geyser-Cube is placed at the top for more bonding wire.

The number of accelerator chips, CMA-Cubes can be changed at low cost. Now, at most 3 CMA-Cubes is available.



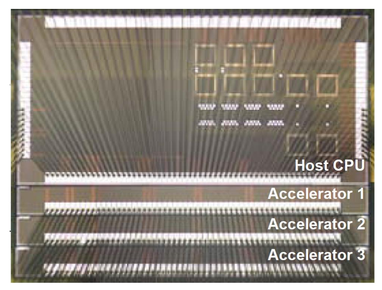
Network Interface

- ✓ Packet Generator
- ✓ Packet Interpreter



Overview of Network Interface

Cube on Real Chip



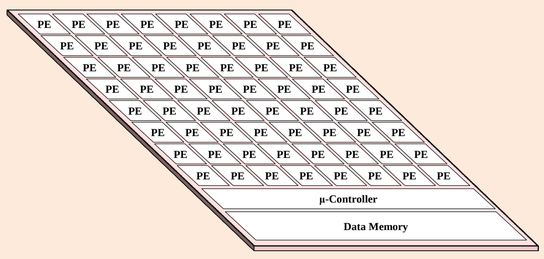
Photograph of Cube

Specification of Cube

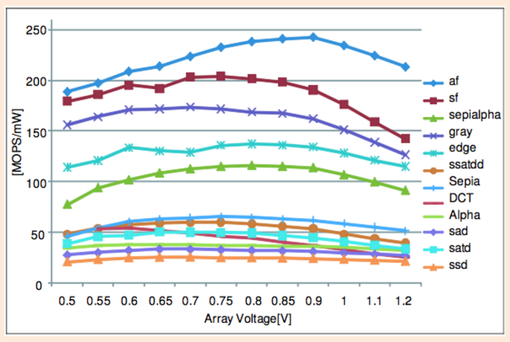
Process	Technology	Fujitsu e-shuttle 65-nm 12-metal CMOS
	Chip Area	2.1mm x 4.2mm
	Core Area	1.5mm x 3.6mm
Geyser-Cube	Clock Freq.	200MHz
	Supply Voltage	1.2V
	I/O	3Gbps TCI 100MHz 32bit I/O
CMA-Cube	Clock Freq.	200MHz
	Supply Voltage	PE Array: 0.5V - 1.2V Other: 1.2V
	I/O	3Gbps TCI

CMA Core

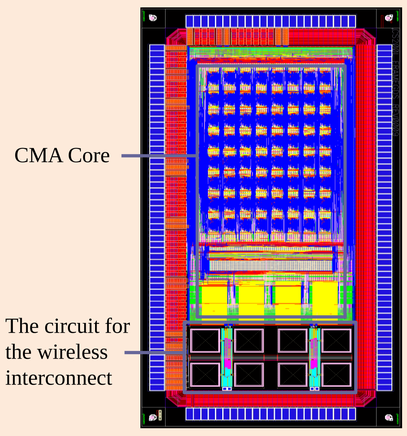
- ✓ PE Array with no memory element (8 x 8)
- ✓ µ-controller for data management (14bits x 64 instruction)
- ✓ 25bits x 1K data memory (2 bank)



Structure of CMA Core



Performance versus Array Voltage Applications



Layout of CMA-Cube

CMA Core Controlling Method

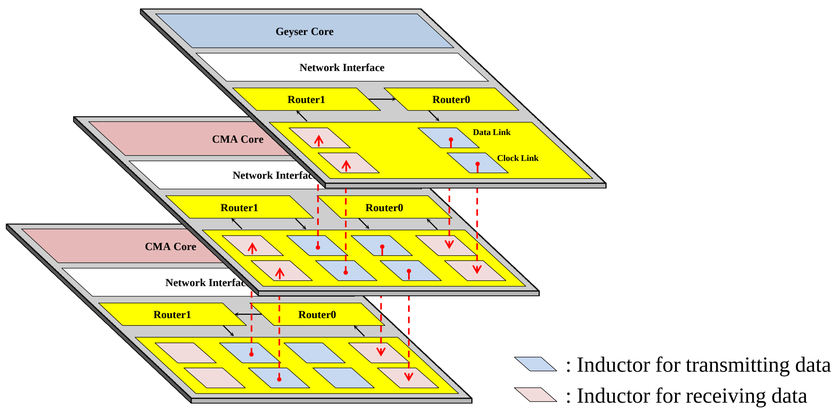
① the delay time of the PE array
② the data handling time taken by the micro-controller

In case that ①<②,
the supply voltage for the PE array is scaled to reduce the power consumption without degrading the performance.

In case that ①>②,
wave-pipelining is applied to enhance performance of the PE array.

Achievement

- ✓ A Cube with 3-chips is available.

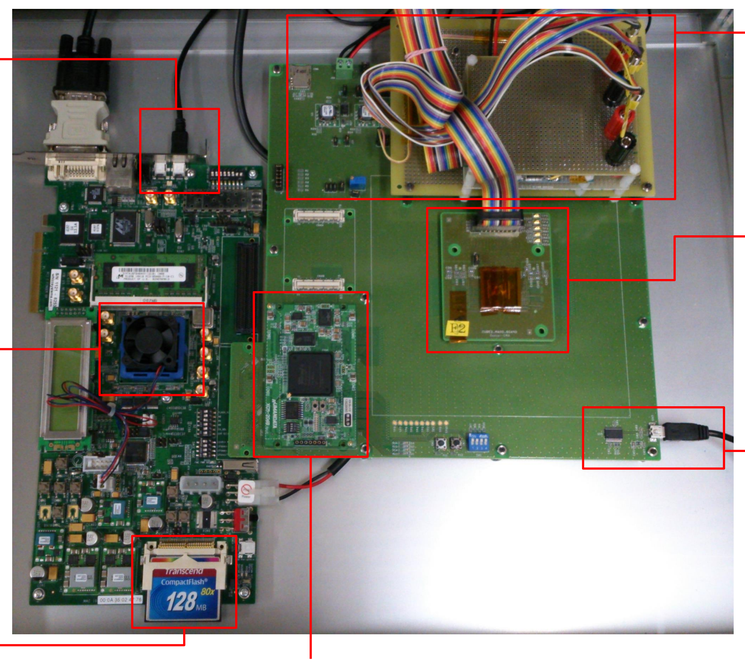


Structure of 3-stacked Cube

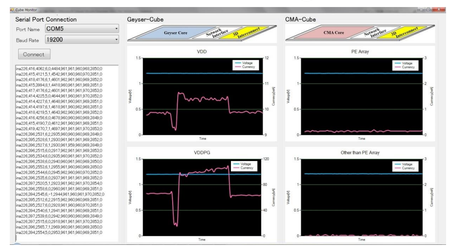
Now, practical application programs using 3-chip system is under development

Demonstration

- ✓ 2 types of image processing on 2-stacked Cube and electric current of each chip will be demonstrated. The effect of power gating is also shown.



Clock Freq.: 50MHz
Execute following application
- α-Blending
- Sepia Filter



Reference

[1] Y. Koizumi, et al, “CMA-Cube: a scalable reconfigurable accelerator with 3-D wireless inductive coupling interconnect”, *In Proceedings of FPL*, Aug. 2012.
[2] D. Ikebuchi, et al., “Geyser-1: A MIPS R3000 CPU core with Fine Grain Runtime Power Gating”, *In Proceedings of ASSCC*, Nov 2009, pp. 281–284.
[3] N. Ozaki, et al, “Cool Mega Arrays: Ultralow-Power Reconfigurable Accelerator Chips", *Micro.IEEE*, vol. 31, no. 6, pp. 6–18, Nov-Dec 2011.