Optical Backplanes with 3D Integrated Photonics?

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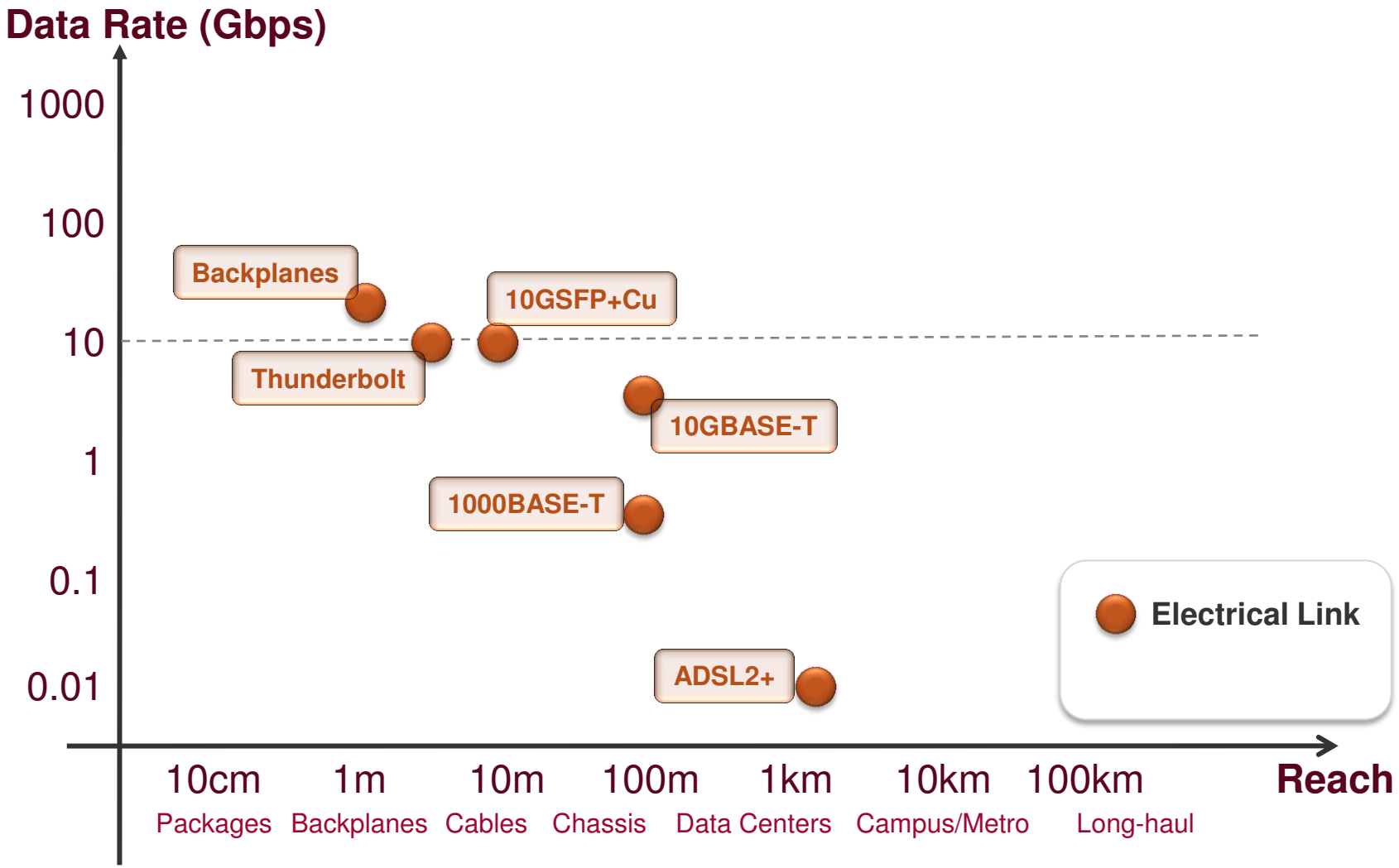
Hot Chips 24, August 2012

Overview

1. Electrical vs. Optical Backplanes
2. Optical vs. Optical Backplanes
3. Chip Stacking: a Means to an End

100Gbps-m Electrical-to-Optical Crossover



•Data points from author. Dotted line from Krishnamoorthy, *et al.*, "Progress in Low-Power Switched Optical Interconnects," *IEEE J. Selected Topics in Quantum Electronics*, vol. 17, no. 2, 2011.
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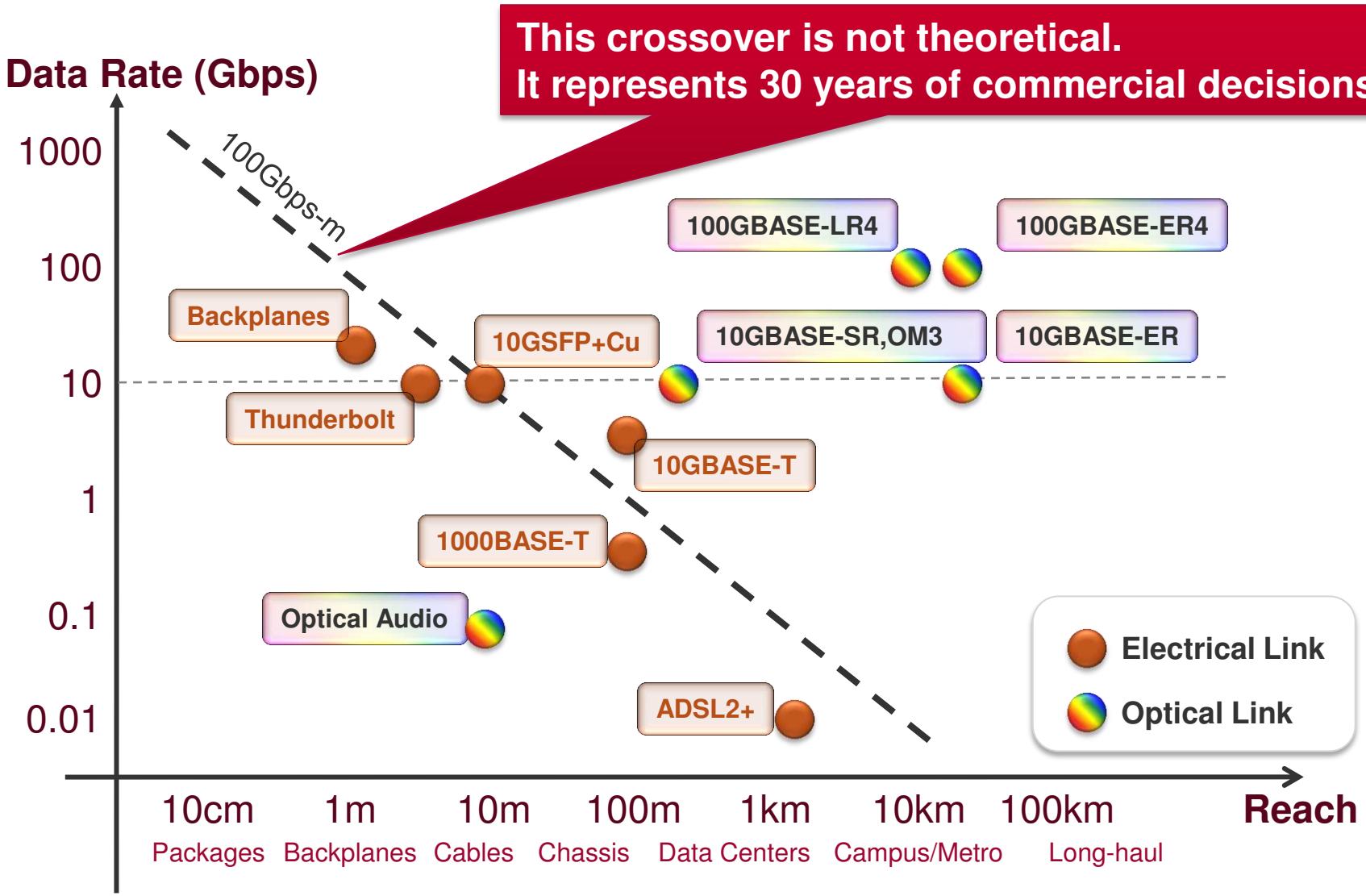

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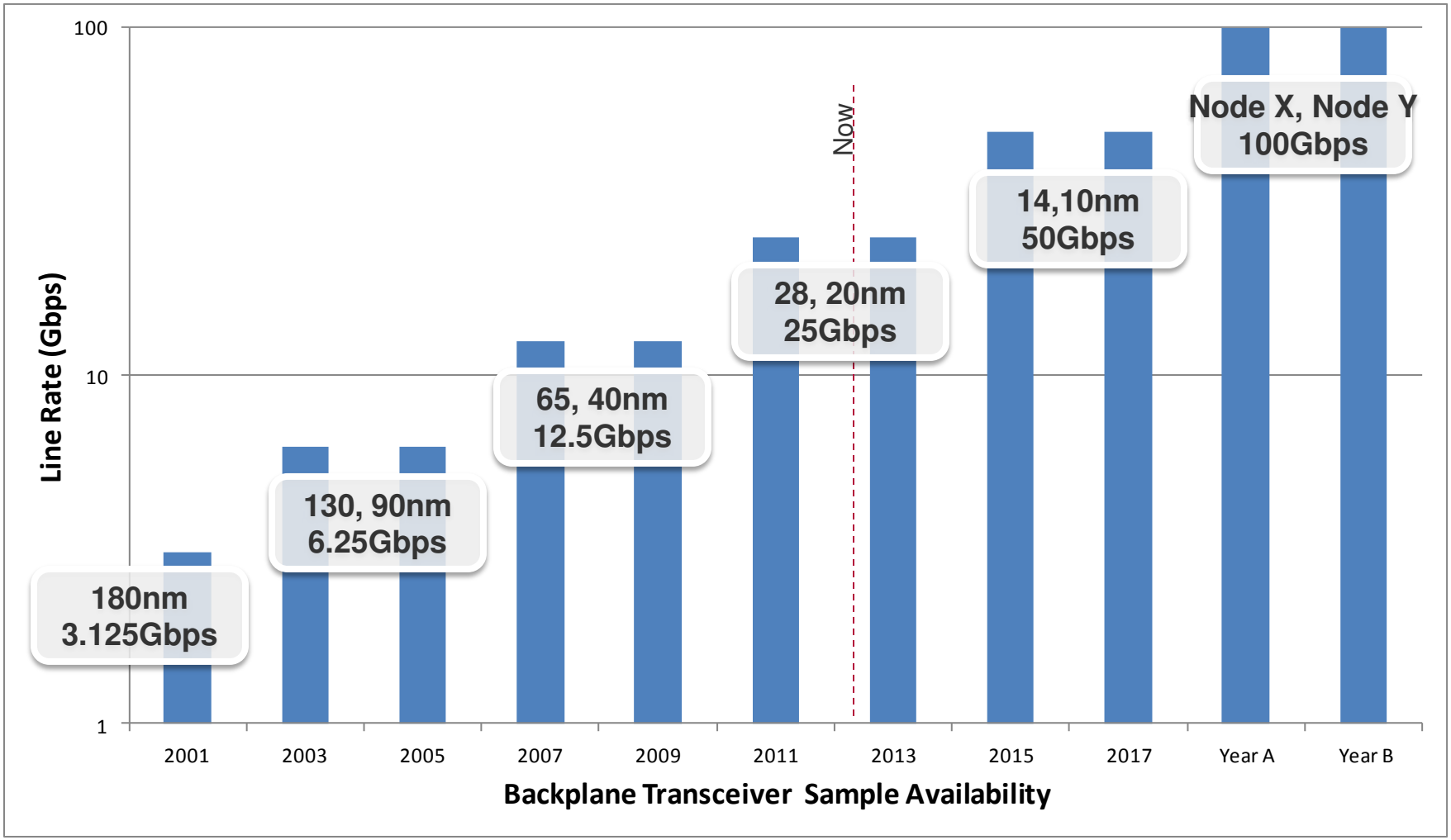
The Industry Has Managed to Double Backplane Line Rates Every Two Nodes



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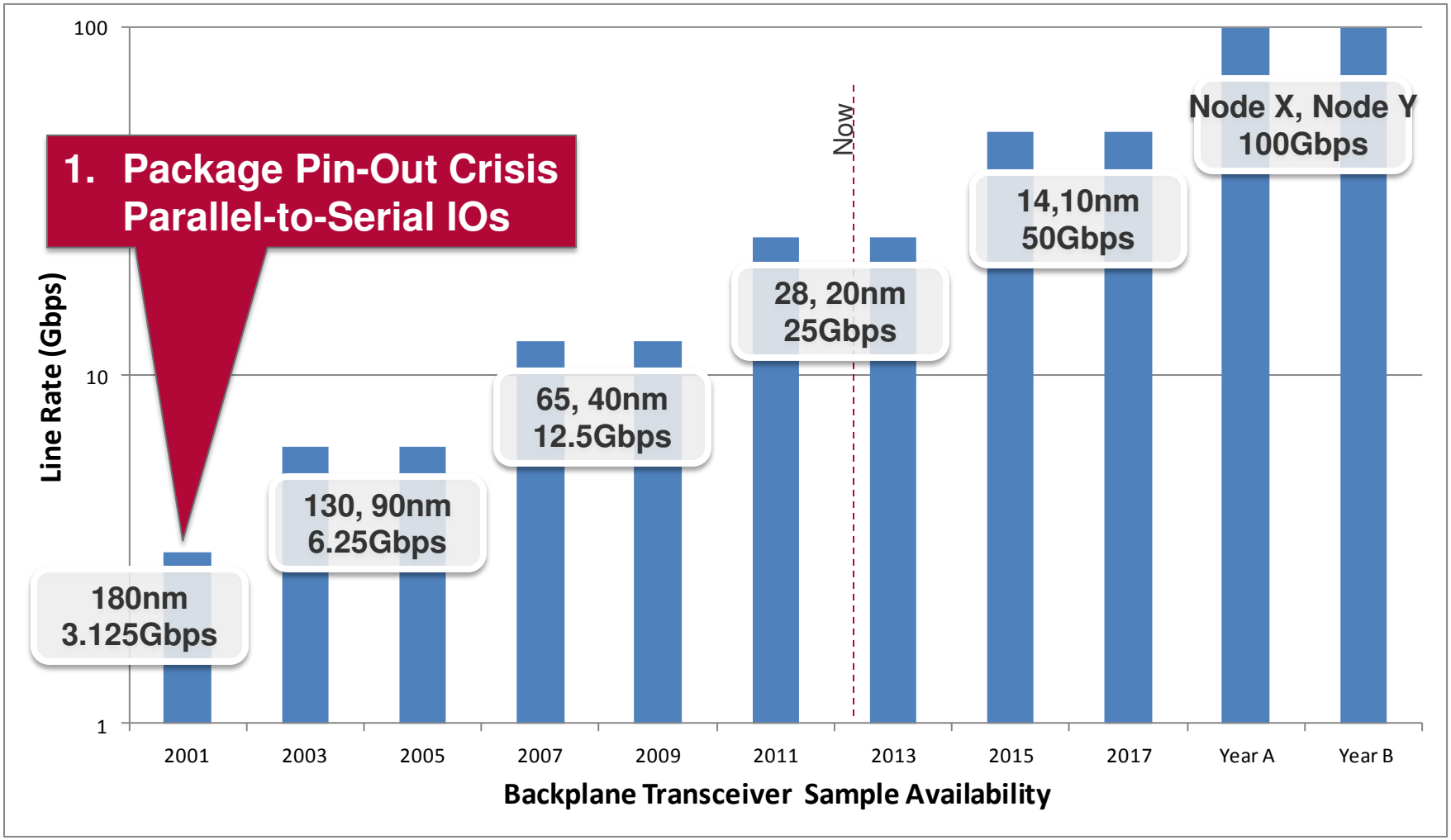

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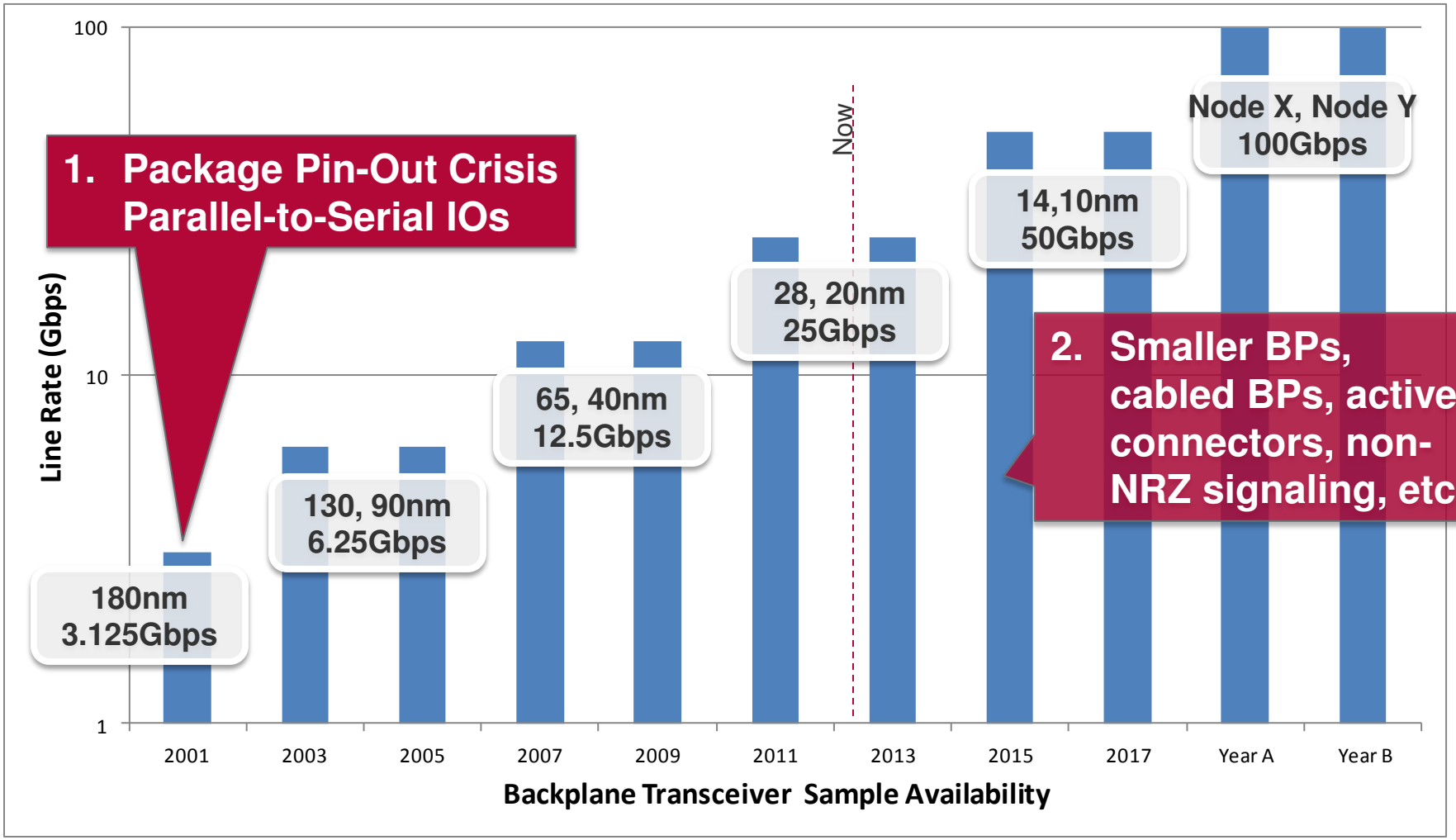

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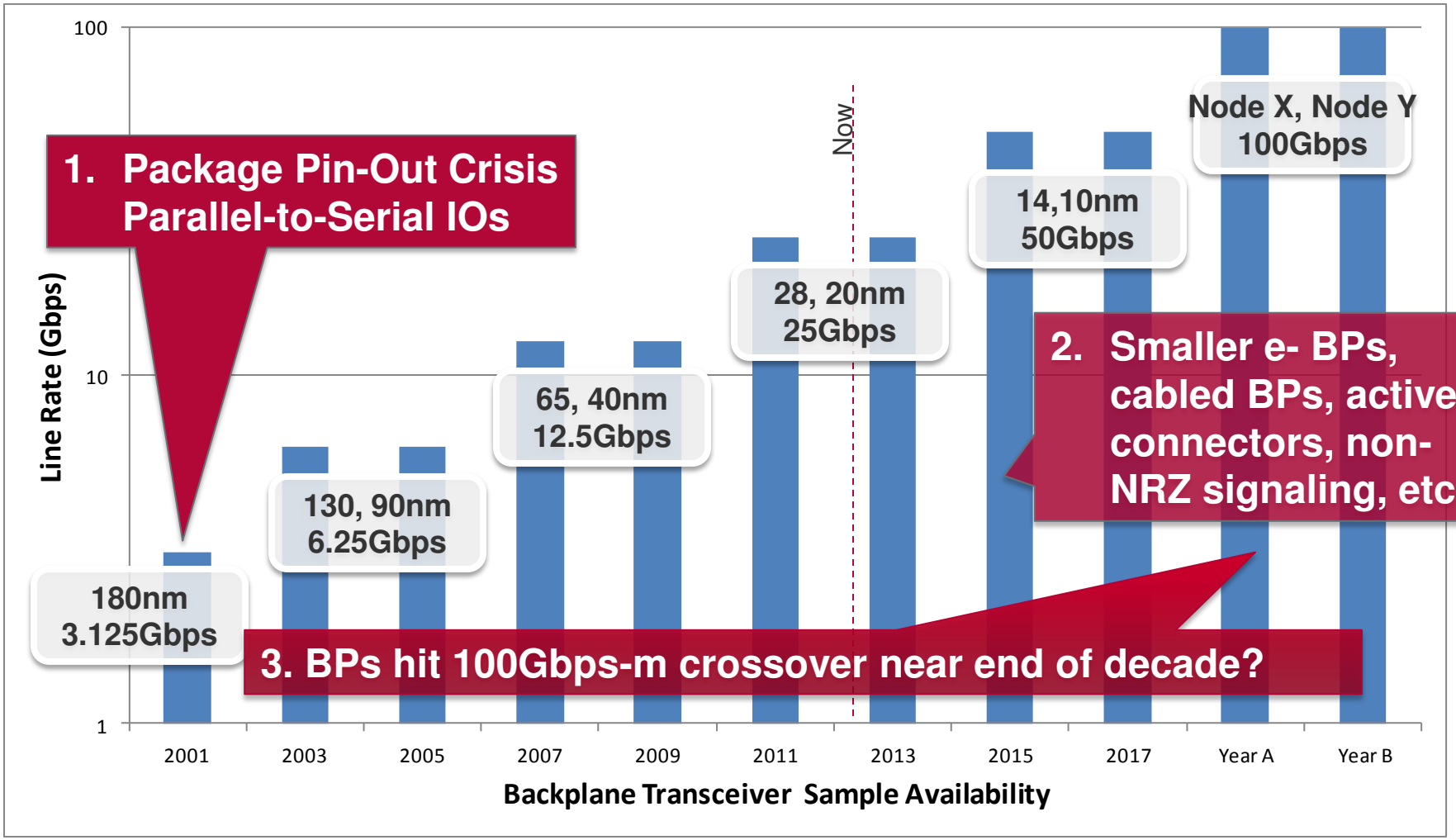
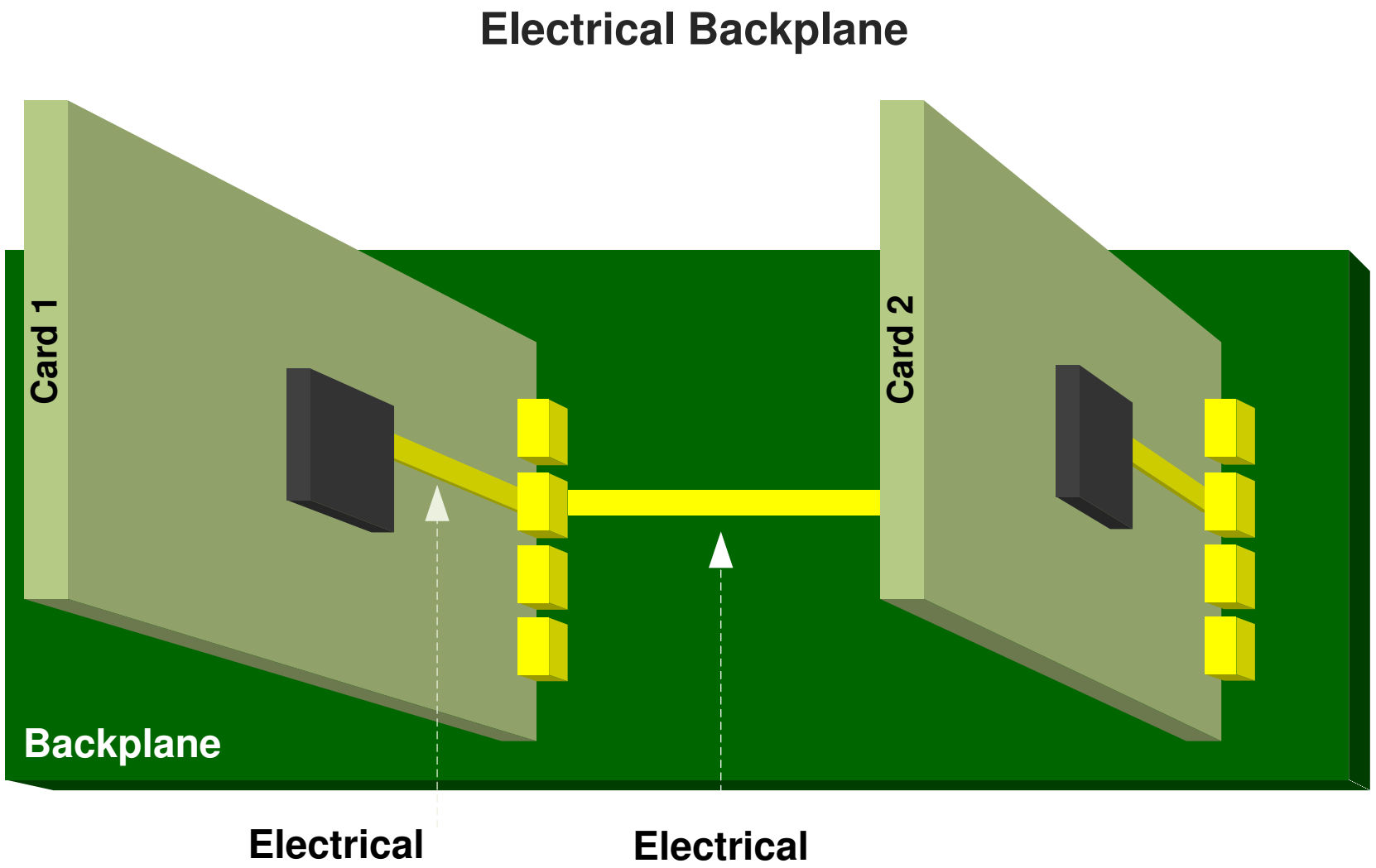


Electrical vs. Optical Backplanes



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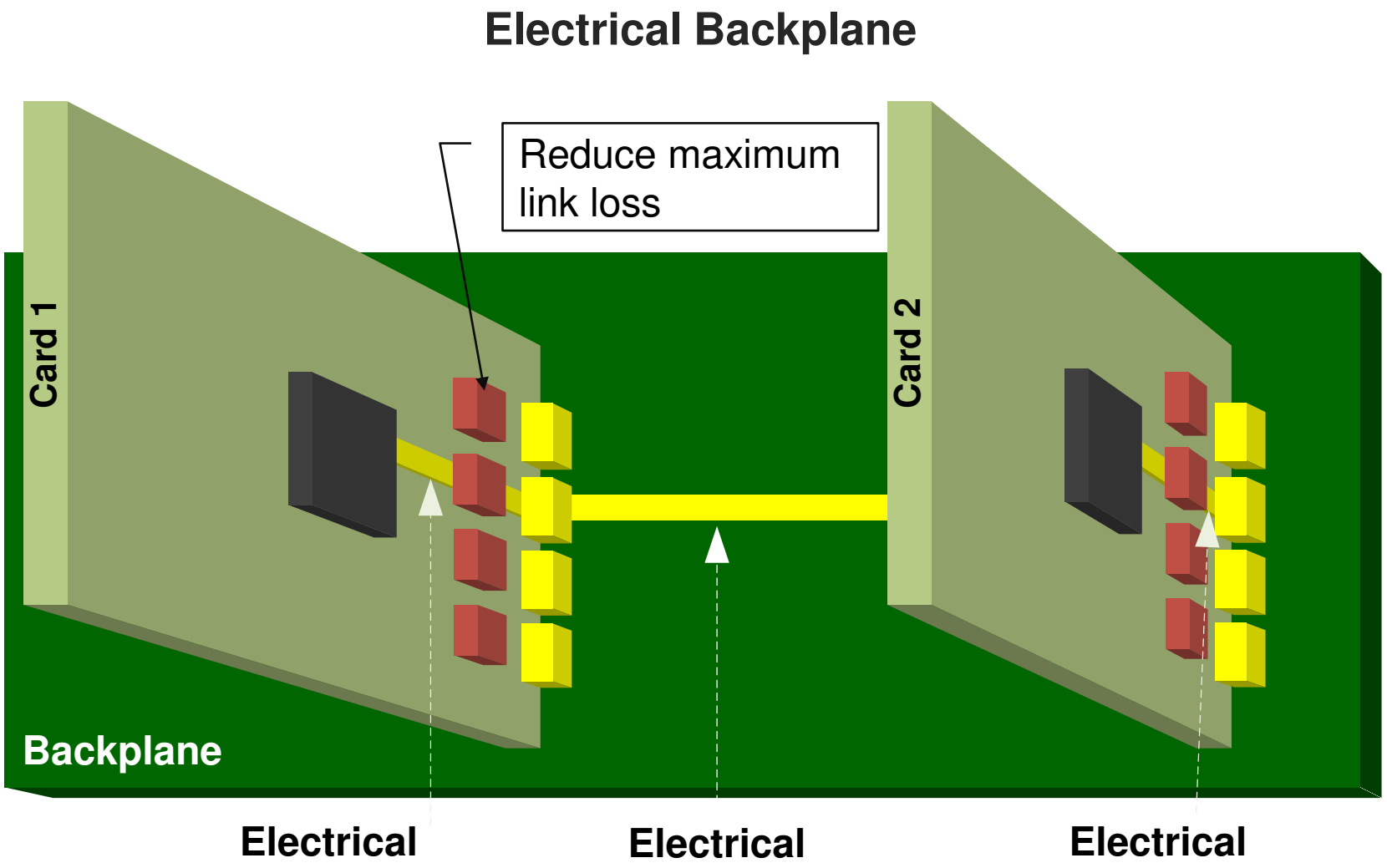

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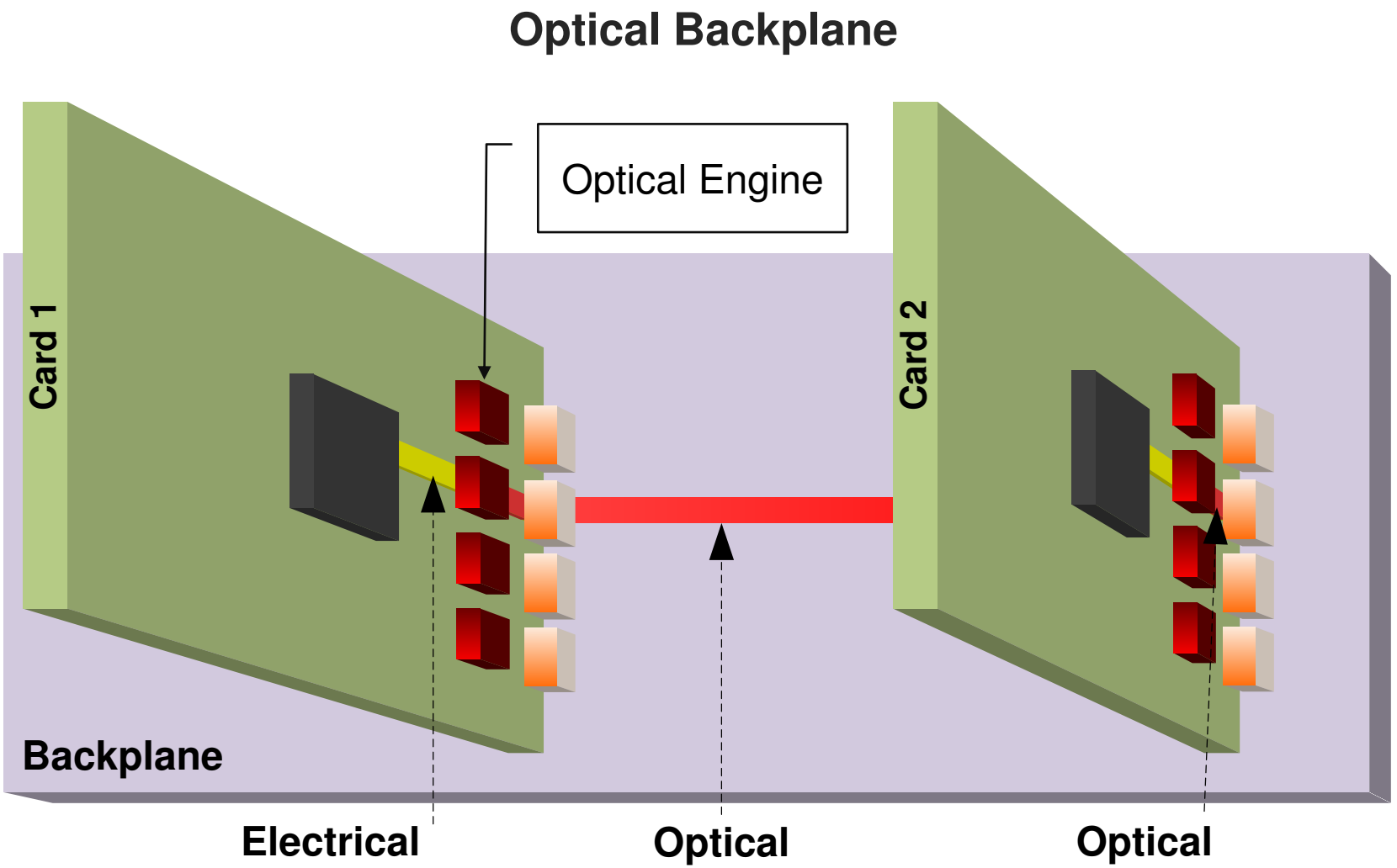

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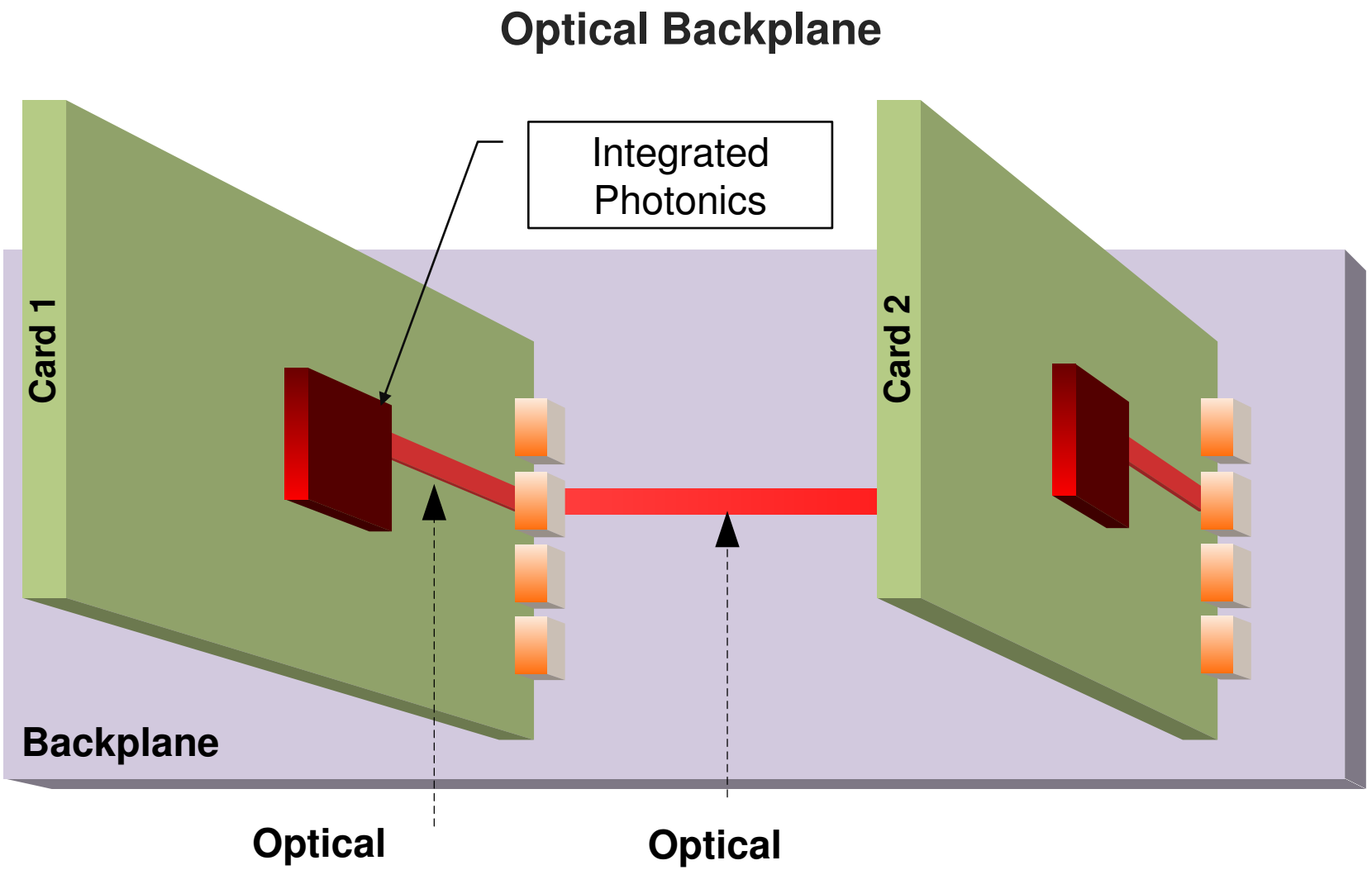
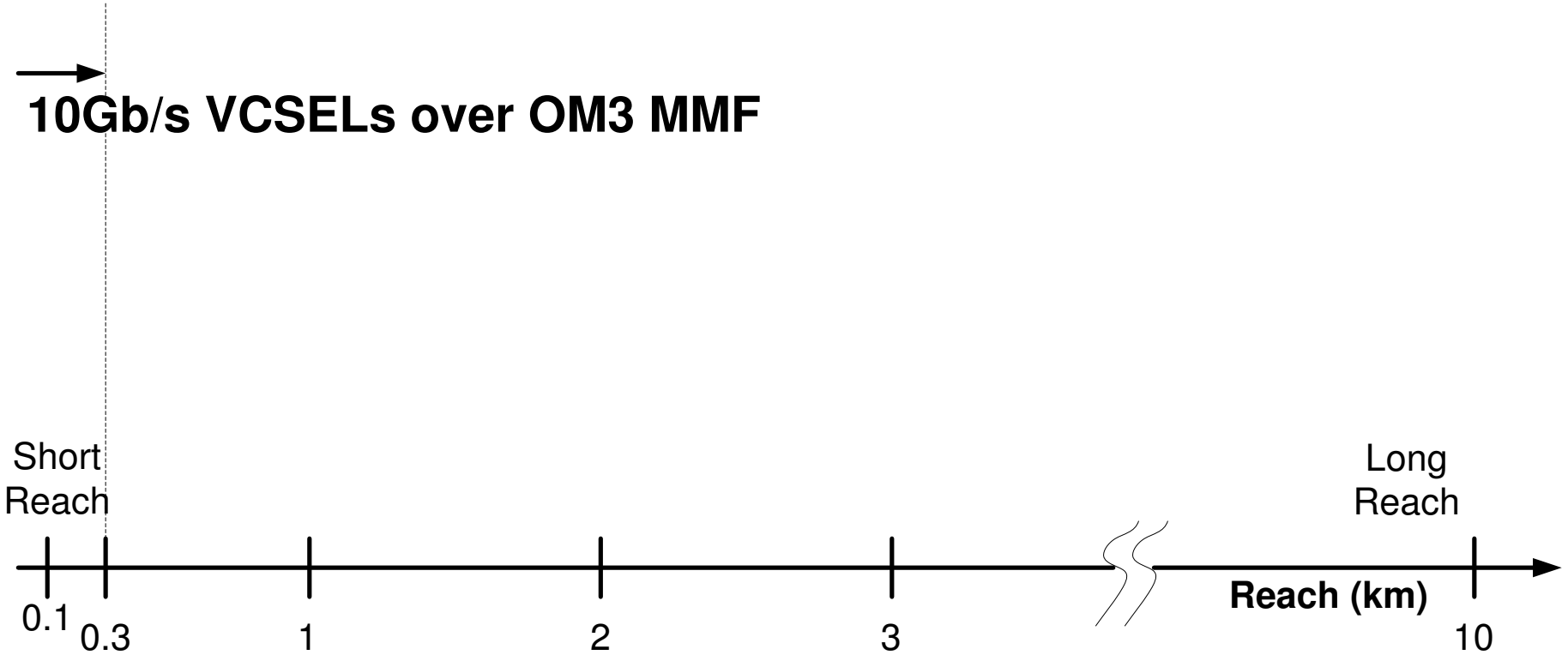
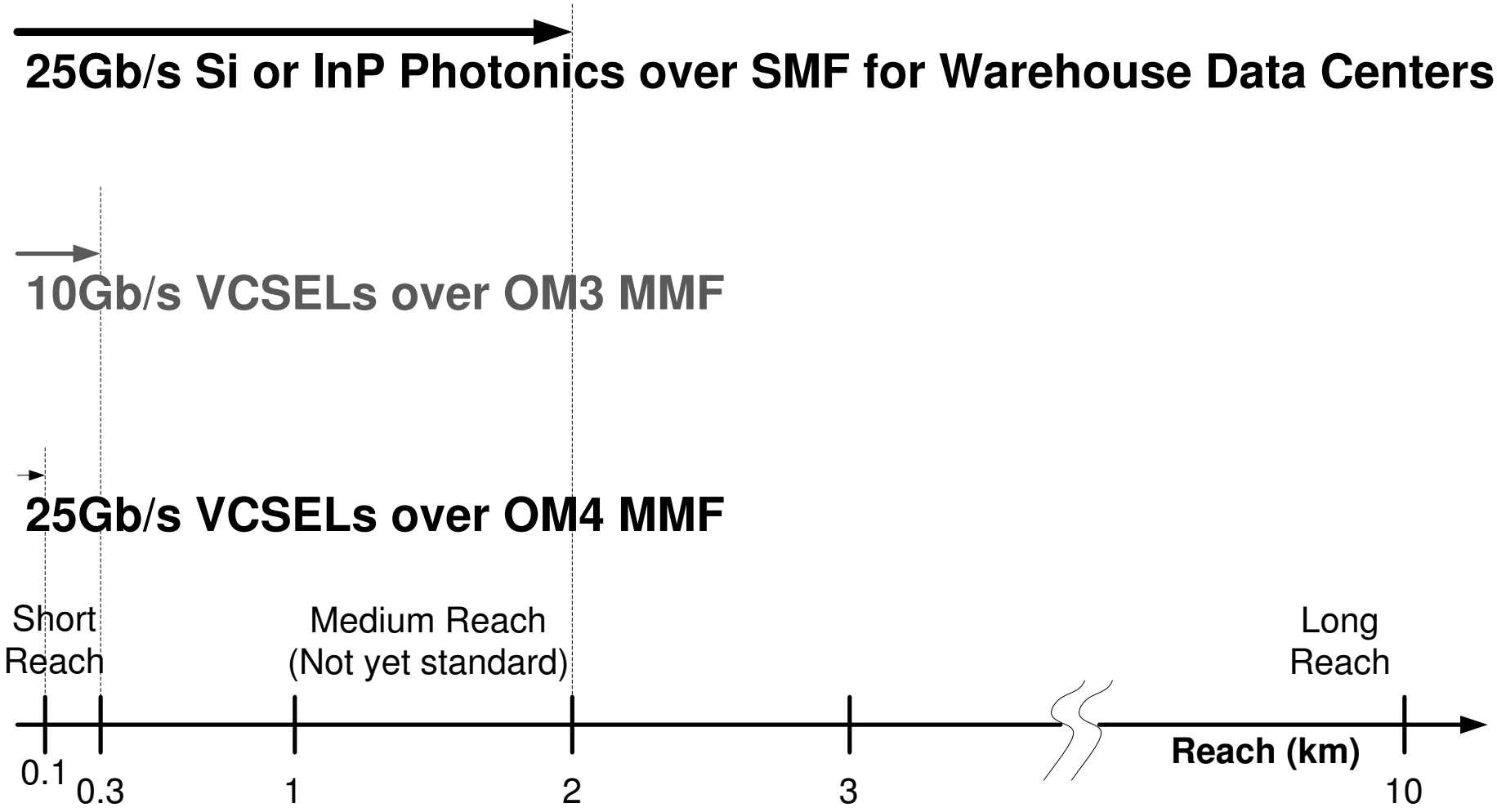


Optical vs. Optical Backplanes (MMF vs. SMF)

VCSELs: the Incumbent at 10 Gb/s



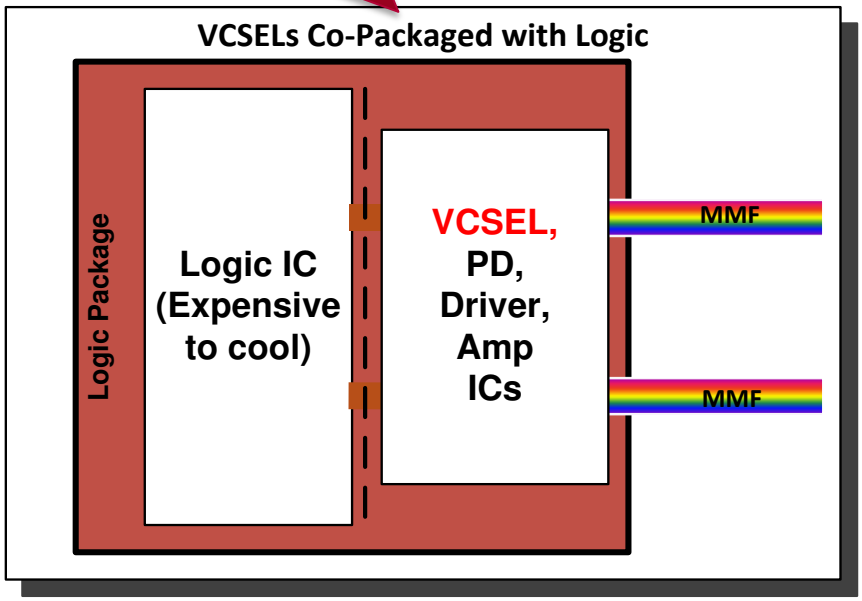
Optical vs. Optical Backplanes
Challengers at 25 Gb/s

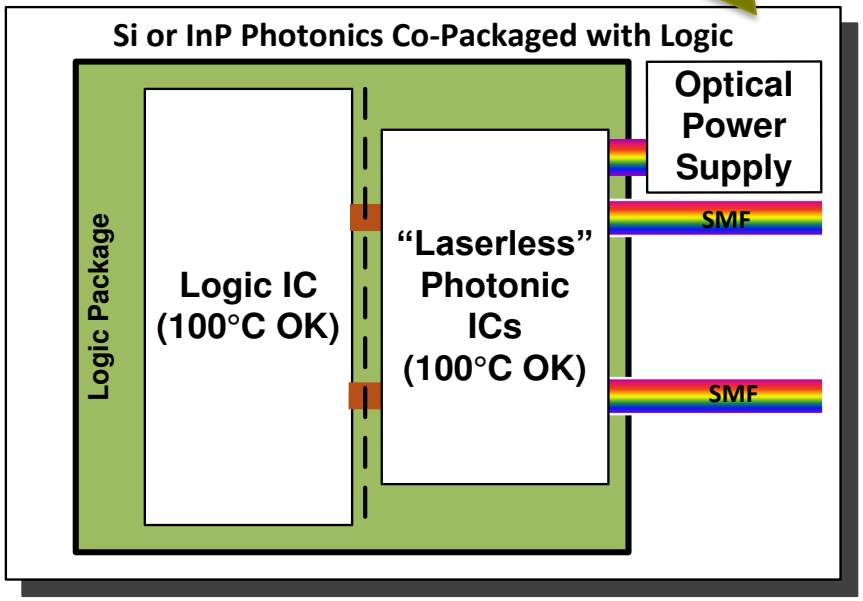


Optical vs. Optical Backplanes
Options in Stacked Photonics

VCSELs: Laser is Thermal Bottleneck
70°C 850nm MMF to 90°C 1550nm SMF?

Off-Package Optical Power Supply
Evict thermal bottleneck (laser) from package.

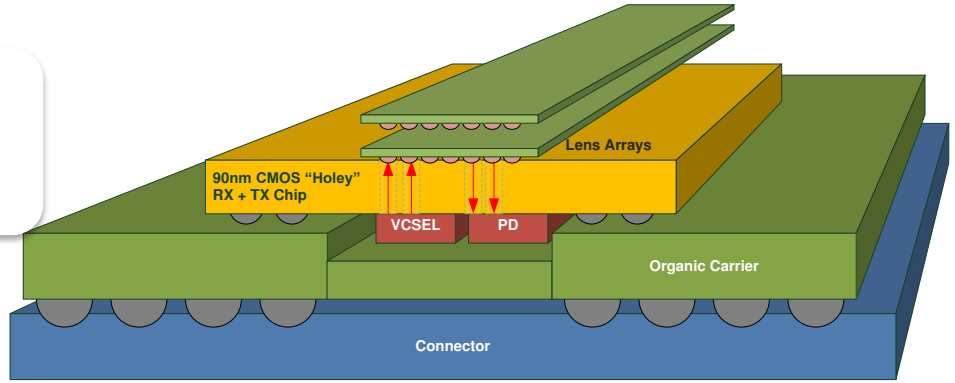




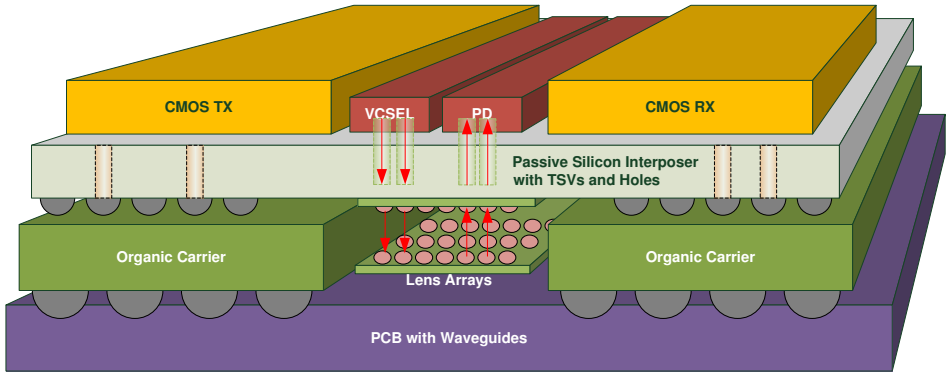
Which technology will scale better?

Stacking Photonics
Who faces up and who faces down?

- Photonics up for fiber attach
- Electronics down and with optical vias (holes)



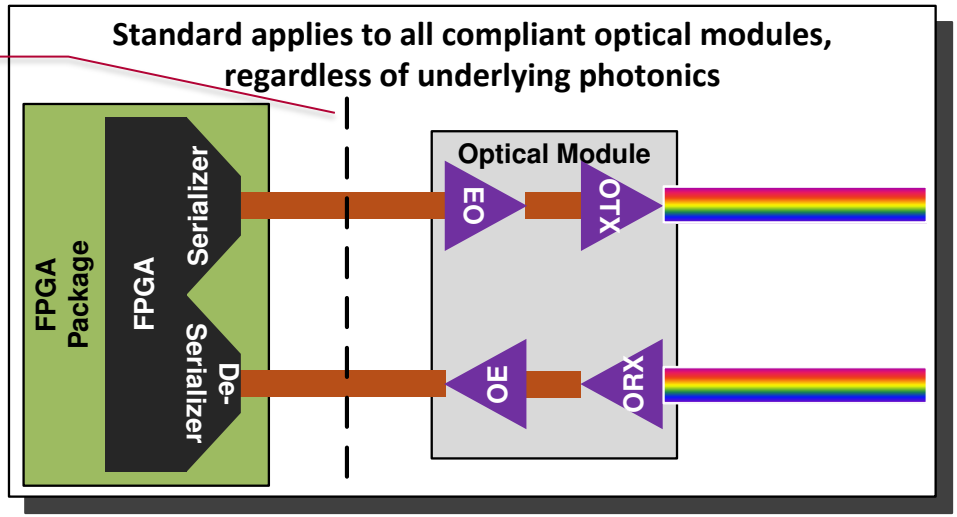
- Photonics down for PWB
- Electronics down
- Si interposer with holes



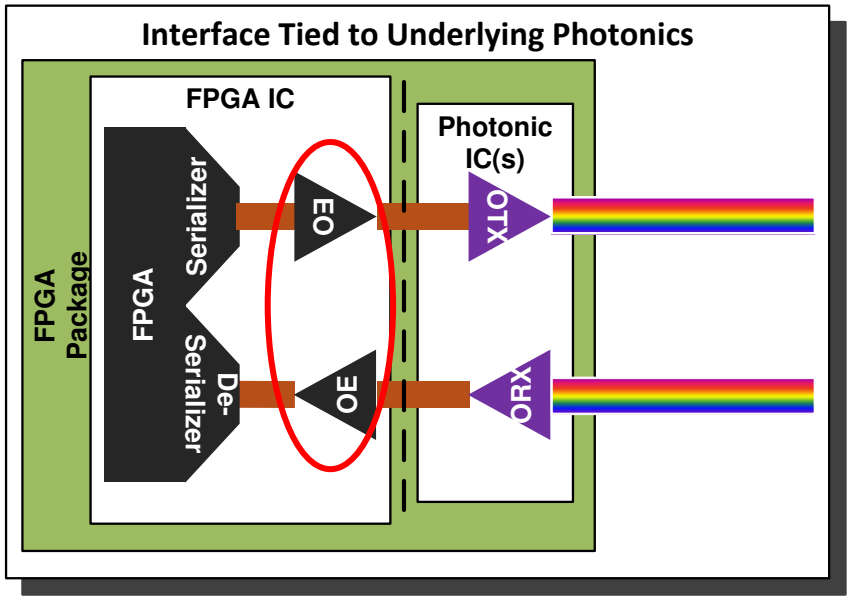
F. Doany, et. al., "Dense 24 TX + 24 RX Fiber-Coupled Optical Module Based on a Holey CMOS Transceiver IC," *60th Electronic Components and Technology Conference,* pp. 248-255, 2010.
F. Doany, et. al., "300-Gb/s 24-Channel Bidirectional Si Carrier Transceiver Optochip for Board-Level Interconnects," *58th Electronic Components and Technology Conference*, pp. 238-243, 2008.
Diagrams redrawn by Xilinx based on papers.

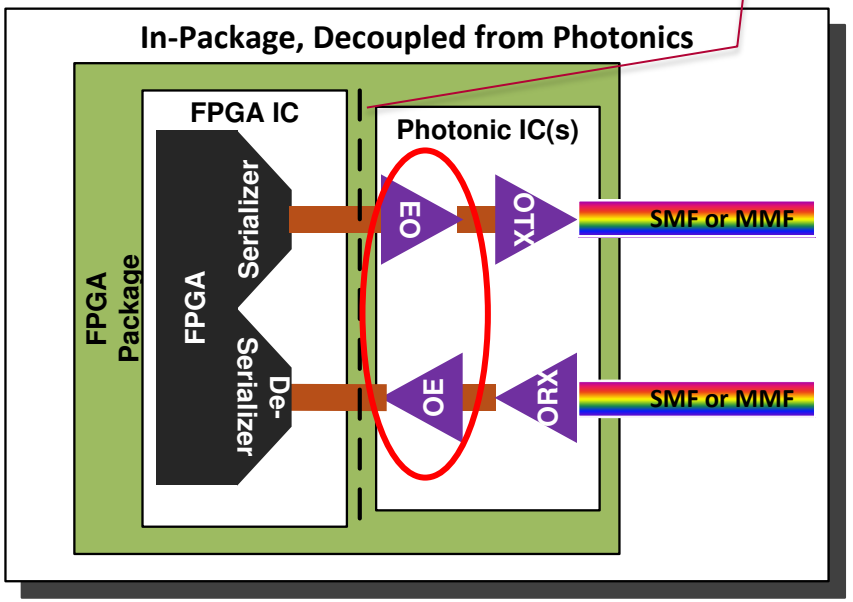
Integrated-Photonics Interface Standards

Example Today: CEI-28G-VSR

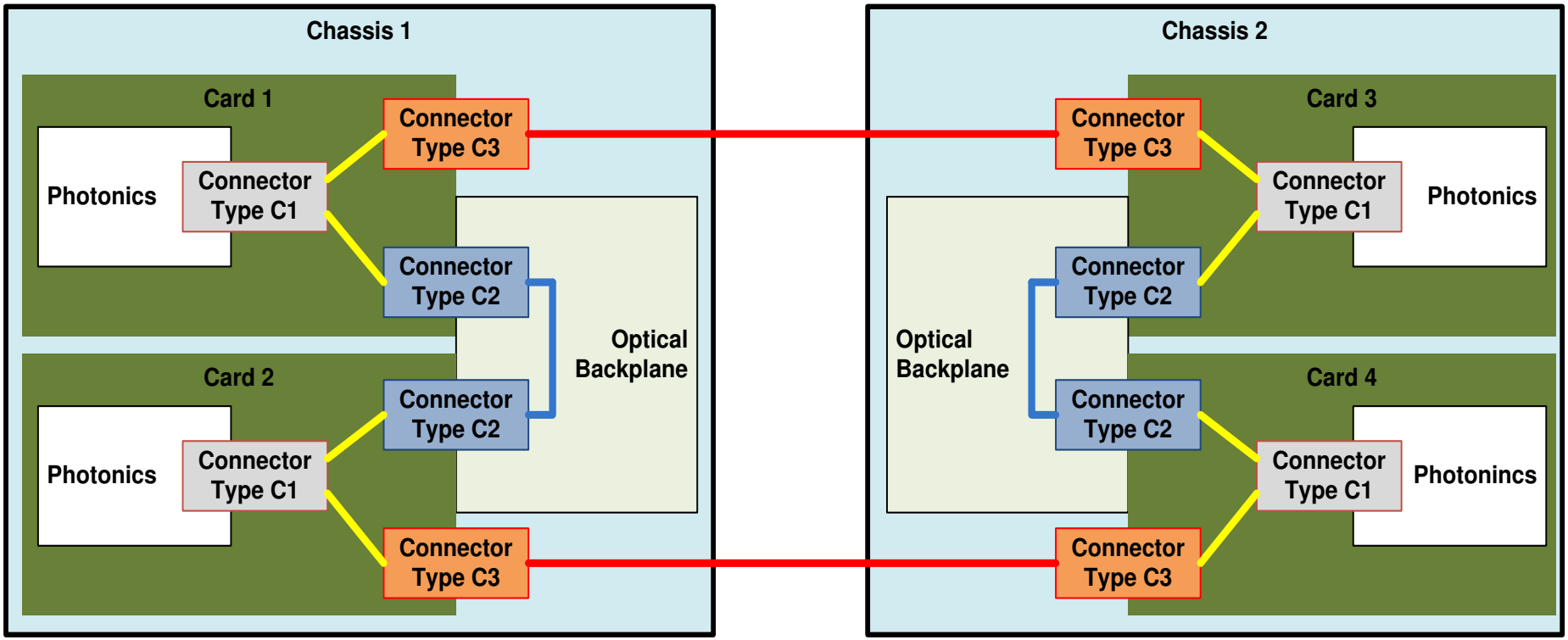


Common electrical inter-IC signaling standard





What Happens Outside the Chip Matters



Link loss at connectors: Distance-Cost Trade-offs

Opto-Electronics Supply Chain Needed

Xilinx Stacked-Silicon Supply Chain

FPGA, Interposer, & Package Design
XILINX

28nm FPGA & Interposer
tsmc

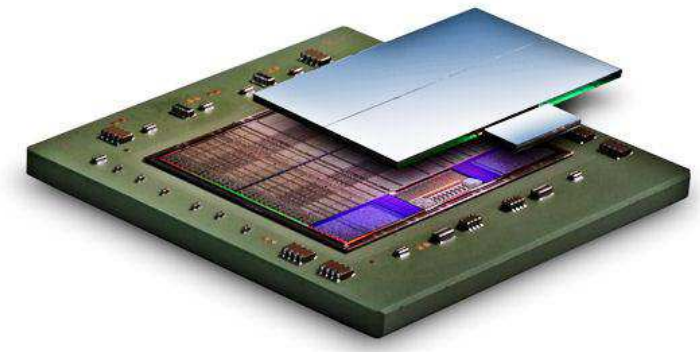
Package Substrate
IBIDEN
KYOCERA

µBump, Die separation
CoC/CoWoS, & Assembly
Amkor Technology
tsmc

Final Test of Packaged Part
XILINX

Opto-Electronics Design
[Names Here]

Opto-Electronics OSAT
[Names Here]



Summary

1. **Electrical vs. Optical Backplanes**
   Mainstream backplanes to reach crossover near end of decade

2. **Optical vs. Optical Backplanes**
   Choice of VCSELs, InP, and Si Photonics impacts costs & scalability

3. **Chip-stacking is just a means to an end**
   Electrical-to-optical migration: focus on systems and supply chain