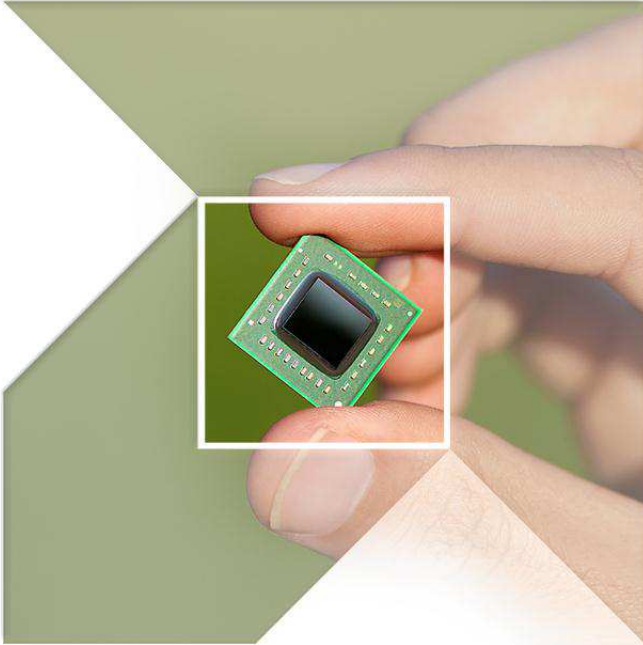


DIE STACKING AND THE SYSTEM

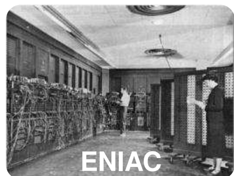
August 27th, 2012

DIE STACKING IS SUFFERING THE DISRUPTIVE TECHNOLOGY CHALLENGE

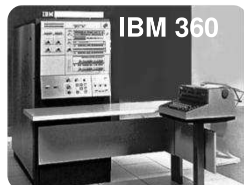
Die stacking seems expensive and risky but the industry needs it

Competing technology evolution seems cheaper, less risky, and good enough but will always be more area, more power, and less performance

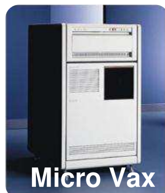
SYSTEM TRENDS IN THE INDUSTRY



Source: Wikipedia



Source: uh.edu



Source: microsoft.com

Source: ibm.com

Source: laptopsarena.com

Source: applefriend.com

40's — 60's — 80's — 90's — Now

Increasing Performance Density

- The industry is driving performance density
- Improvements in performance density are driving new form factors
- New form factors enable new usage models
- Without new usage models the industry stagnates

MOORE'S LAW ENABLES SI INTEGRATION DRIVING NEW FORM FACTORS

μProcessor

Intel 4004

Source: proyectoyautja.proboards.com

Multi-Media

Intel P5

Source: gecko54000.free.fr

Graphics

AMD "Ontario"

Source: AMD

South Bridge is Next

1971 — 1989 — 1993 — 2003 — 2010

Cache & FPU

Intel 486

Source: gecko54000.free.fr

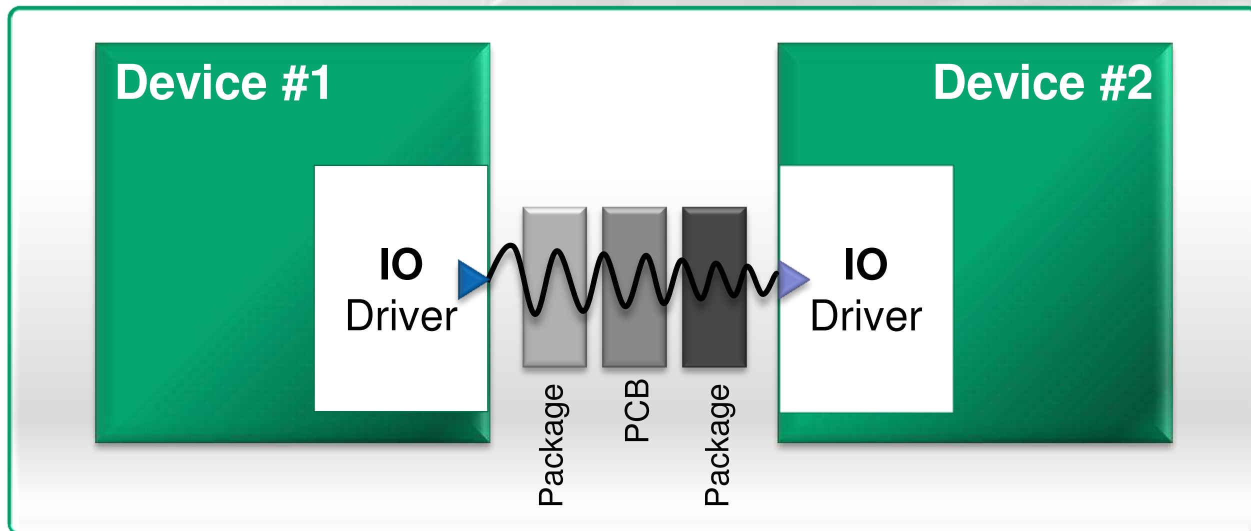
North Bridge

AMD K8

Source: barcelona.com

THE OBVIOUS ADVANTAGE OF INTEGRATION

- Communication is overhead costing power, latency, and footprint



- Interface power is proportional to bandwidth and the link RCs
- And... BW is limited by the off die interface which doesn't scale fast
- But… off die BW demand increases with transistor density

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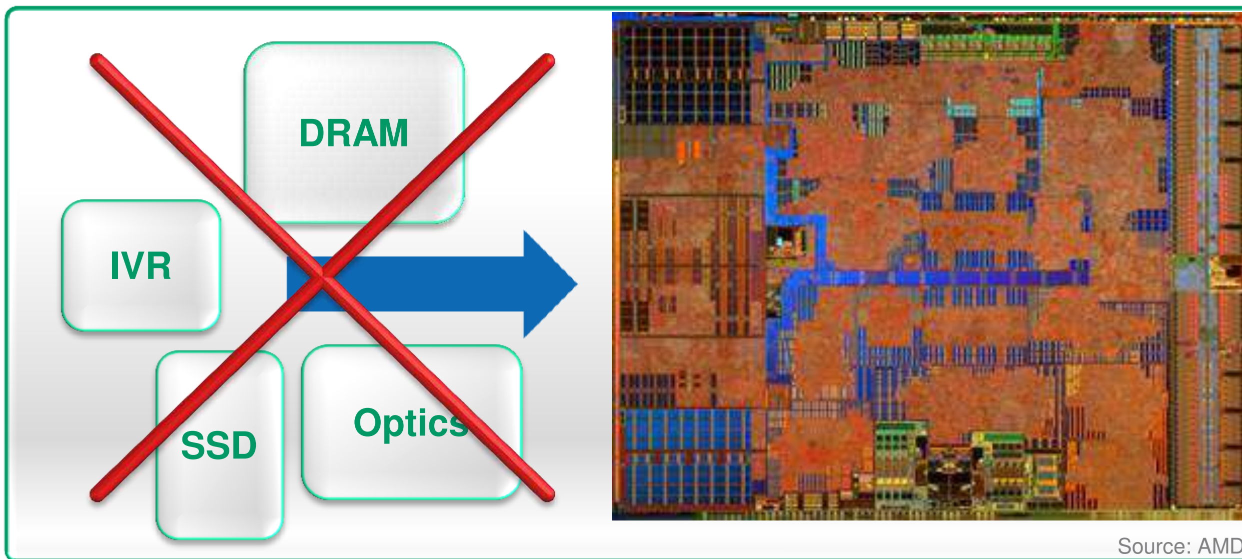
SI INTEGRATION IS RUNNING OUT OF GAS!

- Moore's Law will continue but there is a limitation
  - All similar technology components have been integrated such as Cache, FPU, Multi-Media, NB, GPU, SB, etc…
  - Only disparate technologies such as DRAM, SSD, IVR are left



Source: AMD

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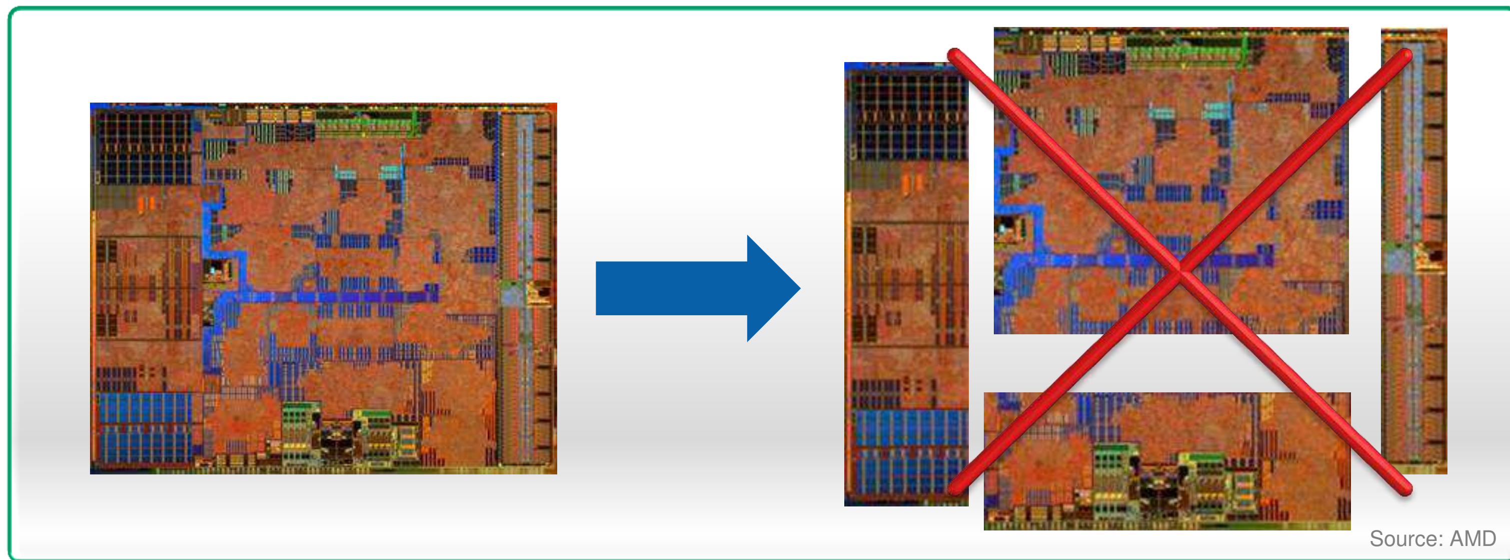
SI INTEGRATION IS RUNNING OUT OF GAS!

- Moore’s Law will continue but there is a problem
  – Process scaling is going to stop supporting diverse functionalities on a single die such as fast logic, low power logic, analog, and cache
  – The single die will want to break into specialized components to maximize the value of new and existing process nodes



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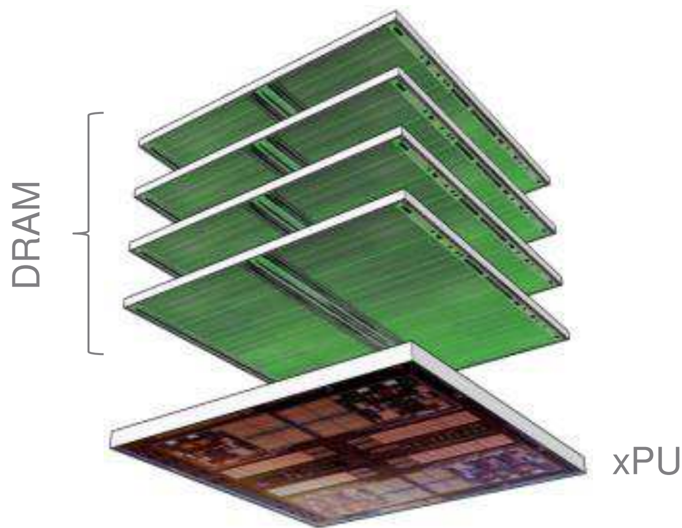
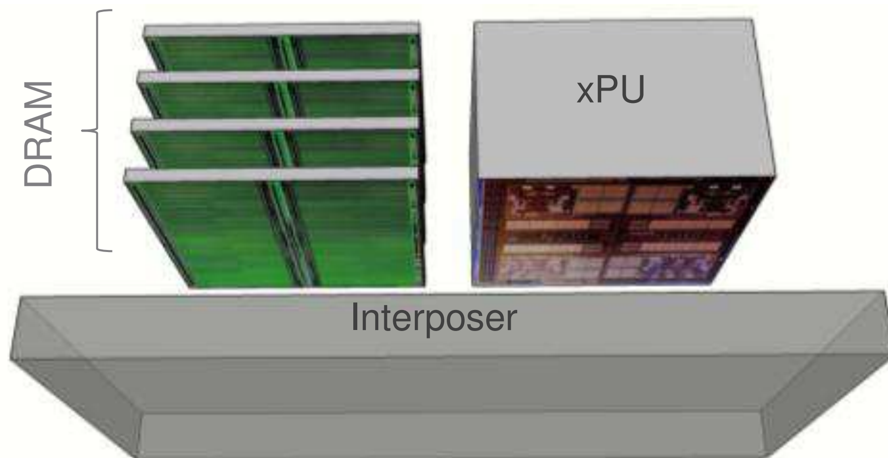
TWO TYPES OF DIE STACKING

- Very similar technologies that reduce metal interconnect and improve proximity of disparate technologies allowing new levels of integration and process specialization





VERTICAL STACKING (3D)

INTERPOSER STACKING (2.5D)

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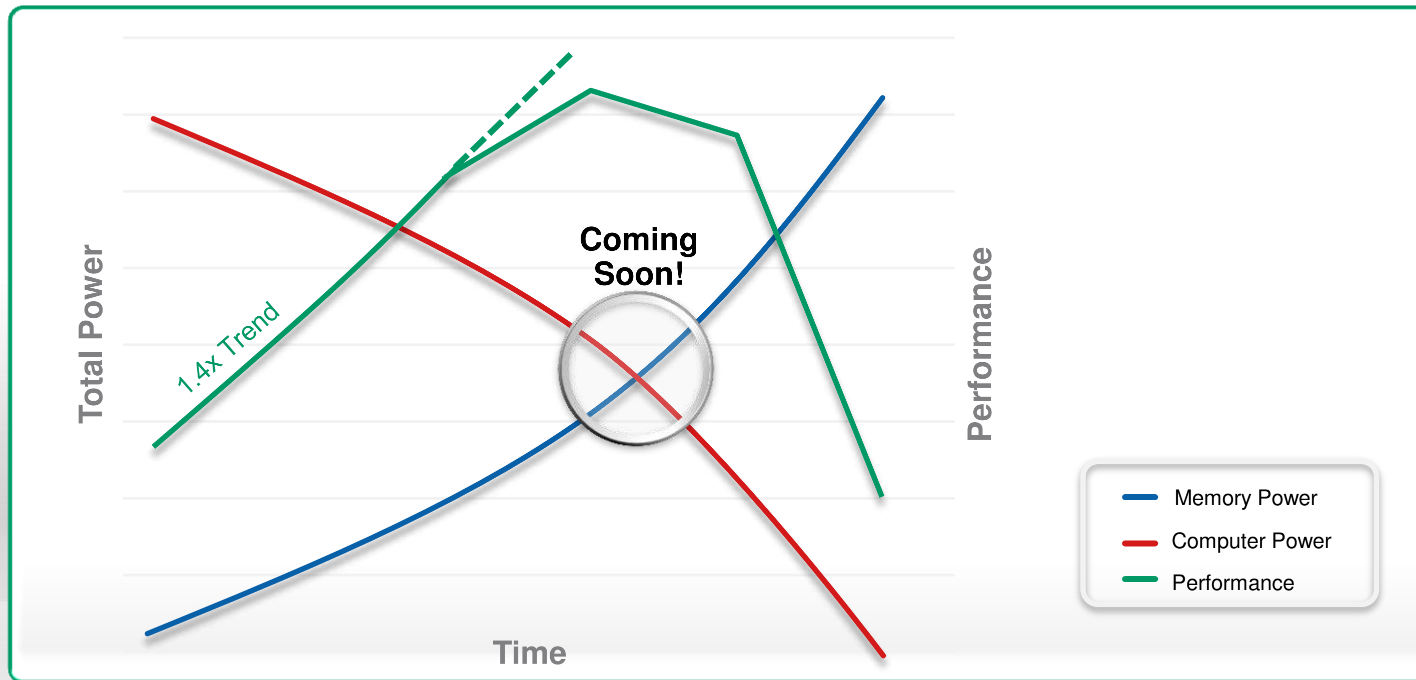
DIE STACKING MOTIVATION (MEMORY INTEGRATION)



- System power is fixed in all platforms
- Compute performance in all platforms is proportional to memory BW
- Memory BW power increases with demand

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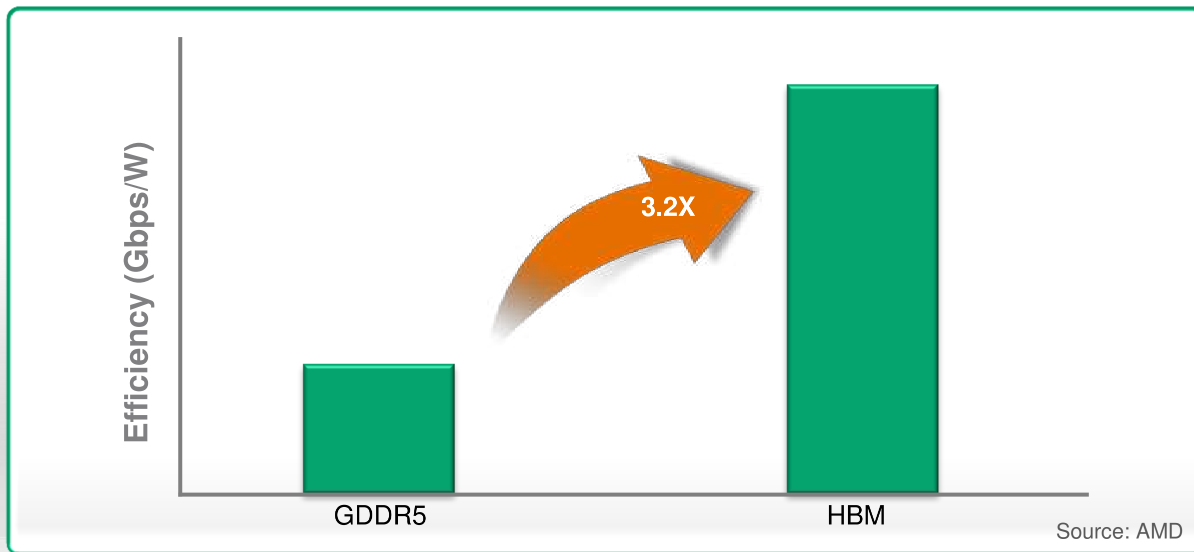
IMPROVING BW/WATT WITH DIE STACKING



- Die stacking helps improve the proximity of the DRAM to Compute
- Dense and fine pitch interconnect enables simple low power interfaces as well as fine grain power control of the DRAM

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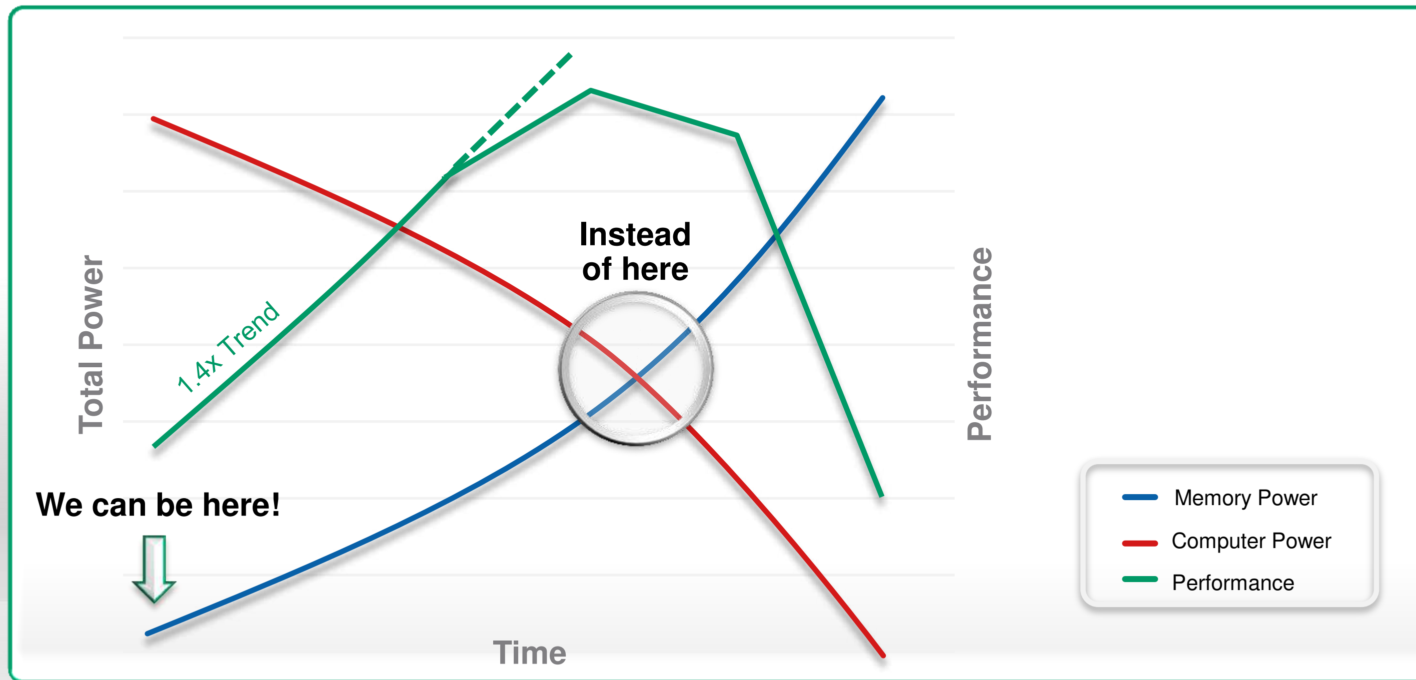
DIE STACKING MOTIVATION (MEMORY INTEGRATION)



- Dramatically improved memory BW/W rolls back the impact of recent memory system power growth and can help provide years of future scaling

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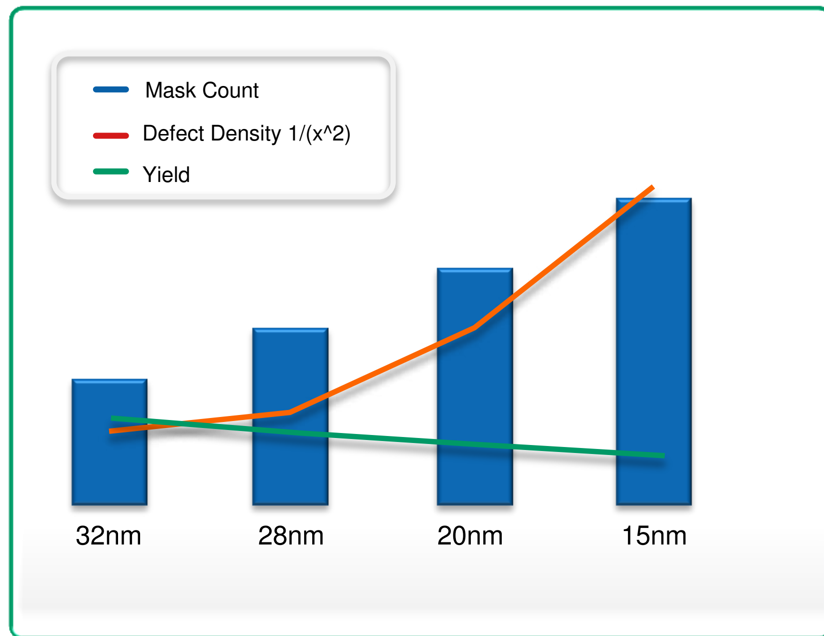
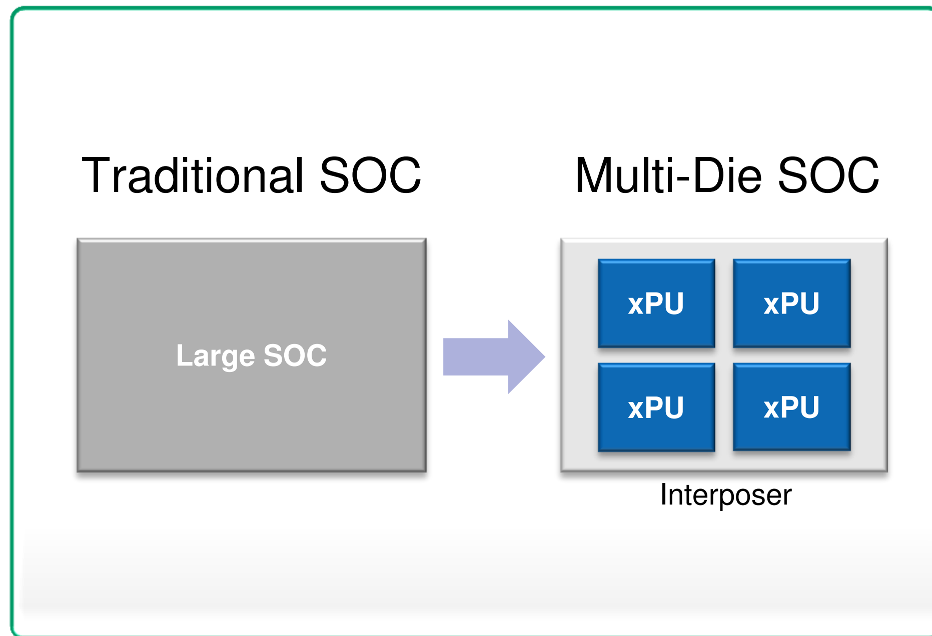
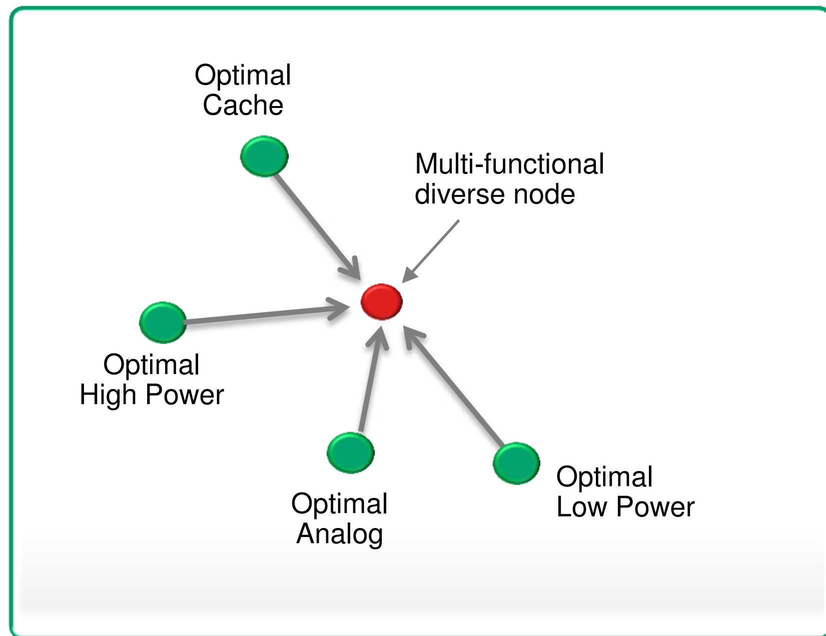
DIE STACKING MOTIVATION (LARGE DIE YIELD IS GETTING WORSE)

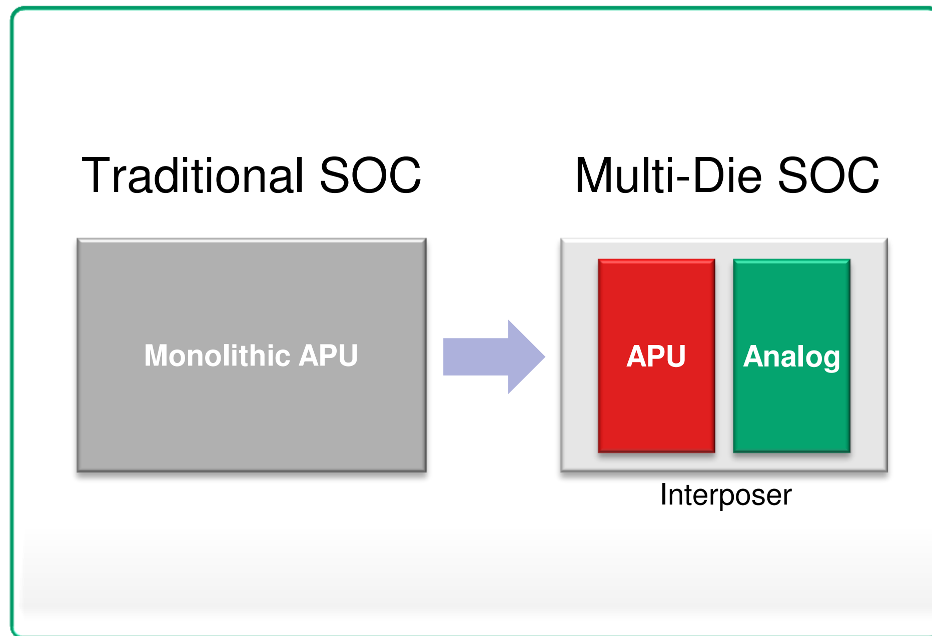




- Process complexity is increasing and yield is dropping as mask count increases
- Large die sizes will continue to have yield challenges

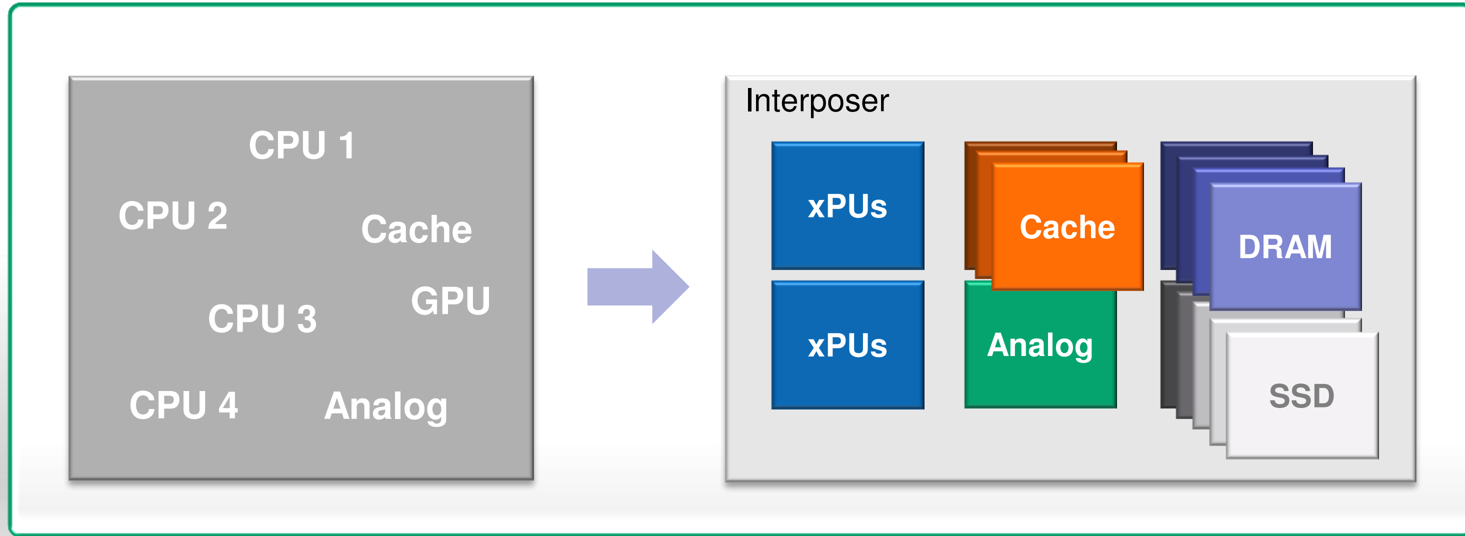
DIE STACKING MOTIVATION (PROCESS COMPLEXITY IS DRIVEN BY DIVERSITY)





- Thick oxide gates are useful for high performance high efficiency IO devices
- Separating functionalities such as Analog reduces node complexity

INTERPOSER WILL BE THE SOC WITH MULTIPLE 3D COMPONENTS



- Focus process node development on specific application functionalities
  - Reduce complexity and mask layer count
  - Reduce process node TTM
  - Reduce wafer runtime
  - Reduce wafer start cost
- Yield improves
- Functionalities scale at their own pace
- IP sharing includes test, reliability, and yield learning
- Improve performance, power, area, and cost of each functionality

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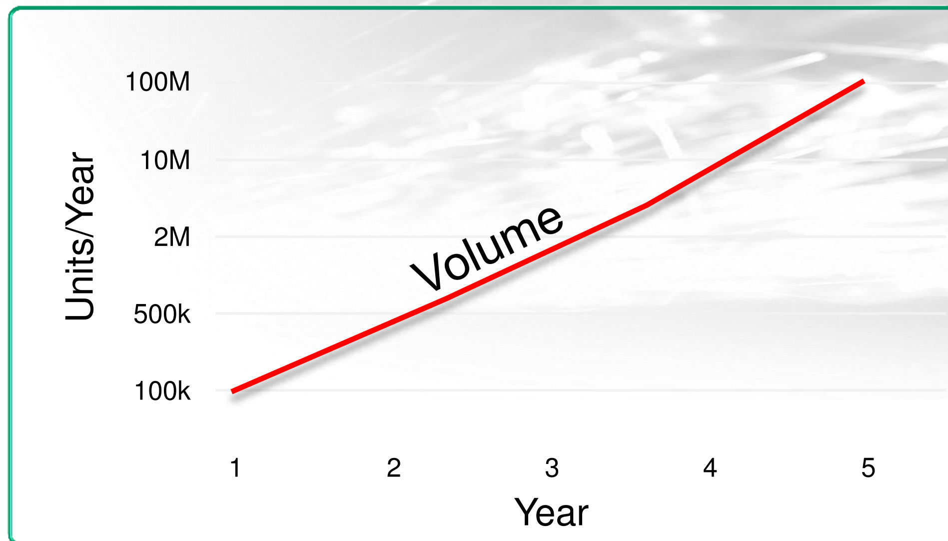
DIE STACKING IS A DEATH BY 1000 CUTS

- **Resources:** Internal and external limitations
- **Business:** New business partners, new business models, new capital investments, no history for forecasting
- **Product:** Design utilization, CAD infrastructure, Define requirements, Mitigate high risk
- **Test:** Wafer probe, KGD, Manufacturing thermal heads, Impact of gimbaling, component test & repair
- **Assembly manufacturing:** Big die challenges, Thin wafer handling, Die to die bonding thermal compression or reflow, Assembly order, New μbump technologies, EM, ESD, Underfill
- **Wafer Manufacturing:** TSVs, Carrier attach/detach, Thinning, μbump
- **Platform:** System characterization changes with integration
- **Packaging:** Large and new materials to reduce warpage
- **Thermals:** System solutions, Package solutions, Materials selection
- **Reliability:** How is reliability proven with multiple vendor components with different requirements?
- **Quality:** How is quality distributed among partners? Who does burn in?
- **Yield & Cost:** Require time for maturity

No single challenge is an issue but there are many and they are diverse

HOW TO GROW THE DIE STACKING INDUSTRY



- **Can't jump to high volume because it requires cost & yield learning**
- **Low volume, high ASP, high margin products will drive the technology**

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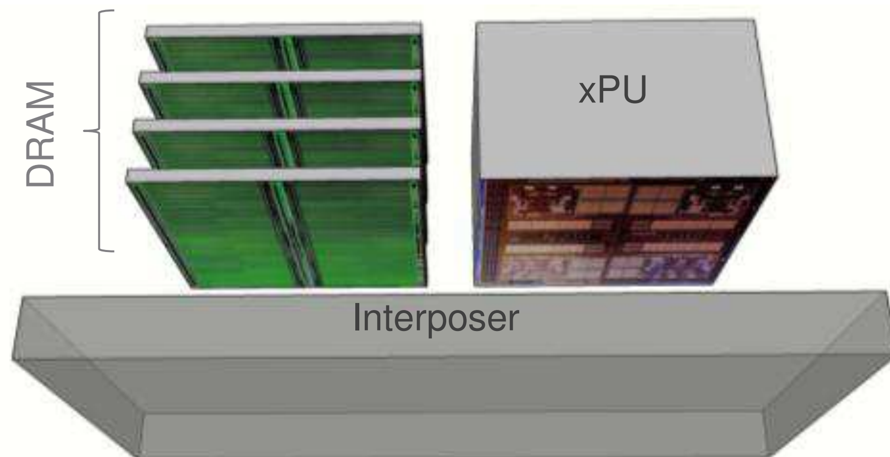
CONCLUSION



VERTICAL STACKING (3D)

INTERPOSER STACKING (2.5D)

- Die stacking will enable new levels of system integration leading to new form factors and new usage models
- Die stacking will also help reduce process node complexity and improve yield and system cost

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