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Xilinx SSI Technology
Concept to Silicon Development Overview

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Aug 27th, 2012

Agenda

- Economic Drivers and Technical Challenges
- Xilinx SSI Technology, Power, Performance
- SSI Development Overview
- Summary

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Market Dynamics

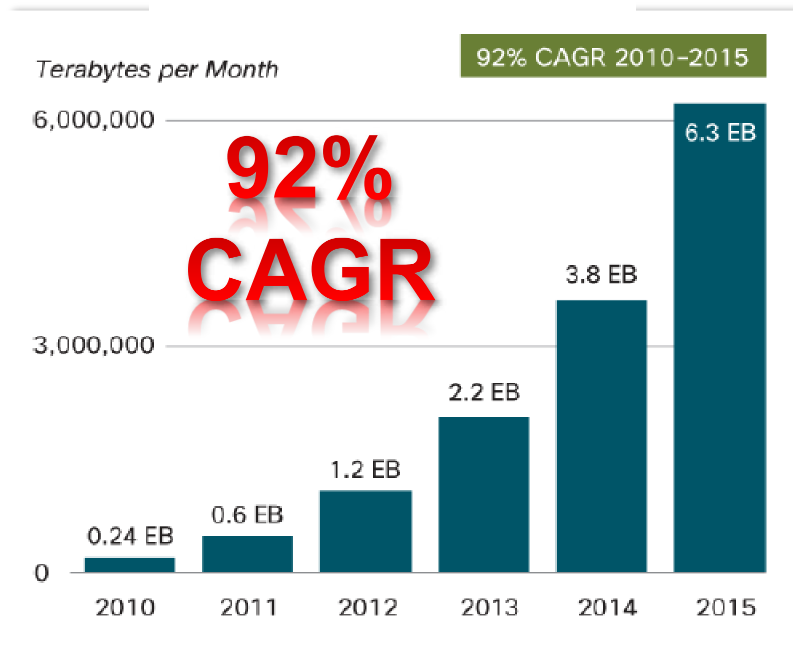
Video Driving Explosive Growth in Traffic

By 2015 2/3 of Mobile Traffic will be Video

Machine to Machine

- **Smart Meters, Security Cameras, Health Care, Telematics, etc.**

Mobile Data Traffic



2x Bandwidth growth every 3 years at the SAME POWER BUDGET

Source: Cisco Global Mobile Traffic, January 2011

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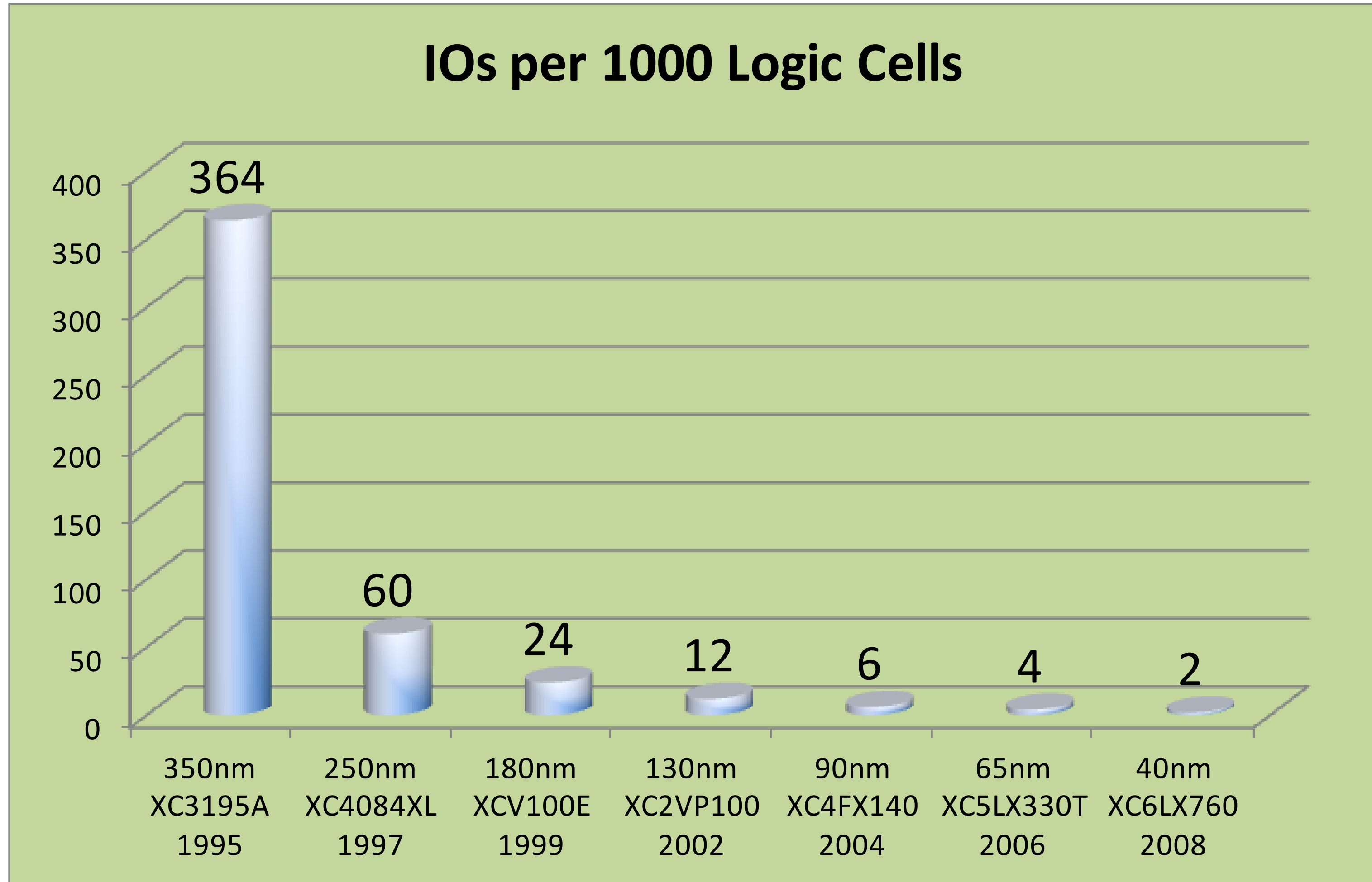
On Die IOs Not Scaling

Number of I/Os per 1000 logic cells in the largest FPGA in each family



Logic doubles with Moore's Law but I/O quantity does not

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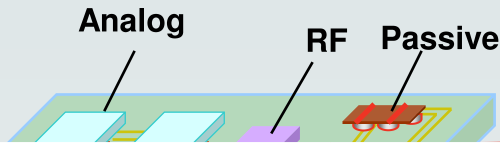
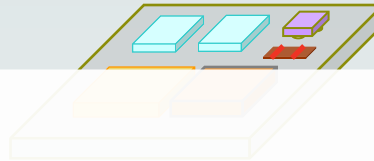
The Progression of 3D Technology

Traditional MCM/PCB	Silicon Interposer 2.5D	Full 3D





Goals for 2.5D / 3D

- Connectivity: Break die to die IO bottleneck
- Capacity: Achieve Integration beyond Moore's Law
- Power: Reduce Total Power
- Heterogeneous SOC's: Mixed Functions & Processes

Flipchip + wire bond

2.5D side-by-side integration on a silicon interposer

Vertical stacking with memory & logic

Source: TSMC

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Capacity : Beyond Moore's Law

Manufacturability

Sooner

500k LC

2M LC w/ Stacked Silicon Interconnect

Prod

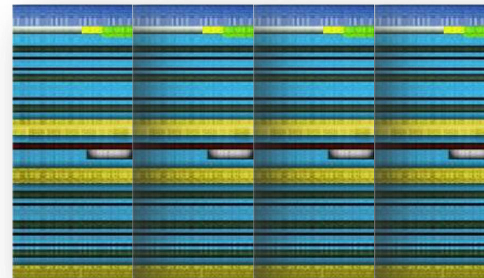
ES

1M LC

Time

2M LC

Multiple Small Die Slices



✓ **Greater capacity, faster yield ramp**

Reference:
Node N to N+1 ~ 1.5 to 2 years for Xilinx FPGAs

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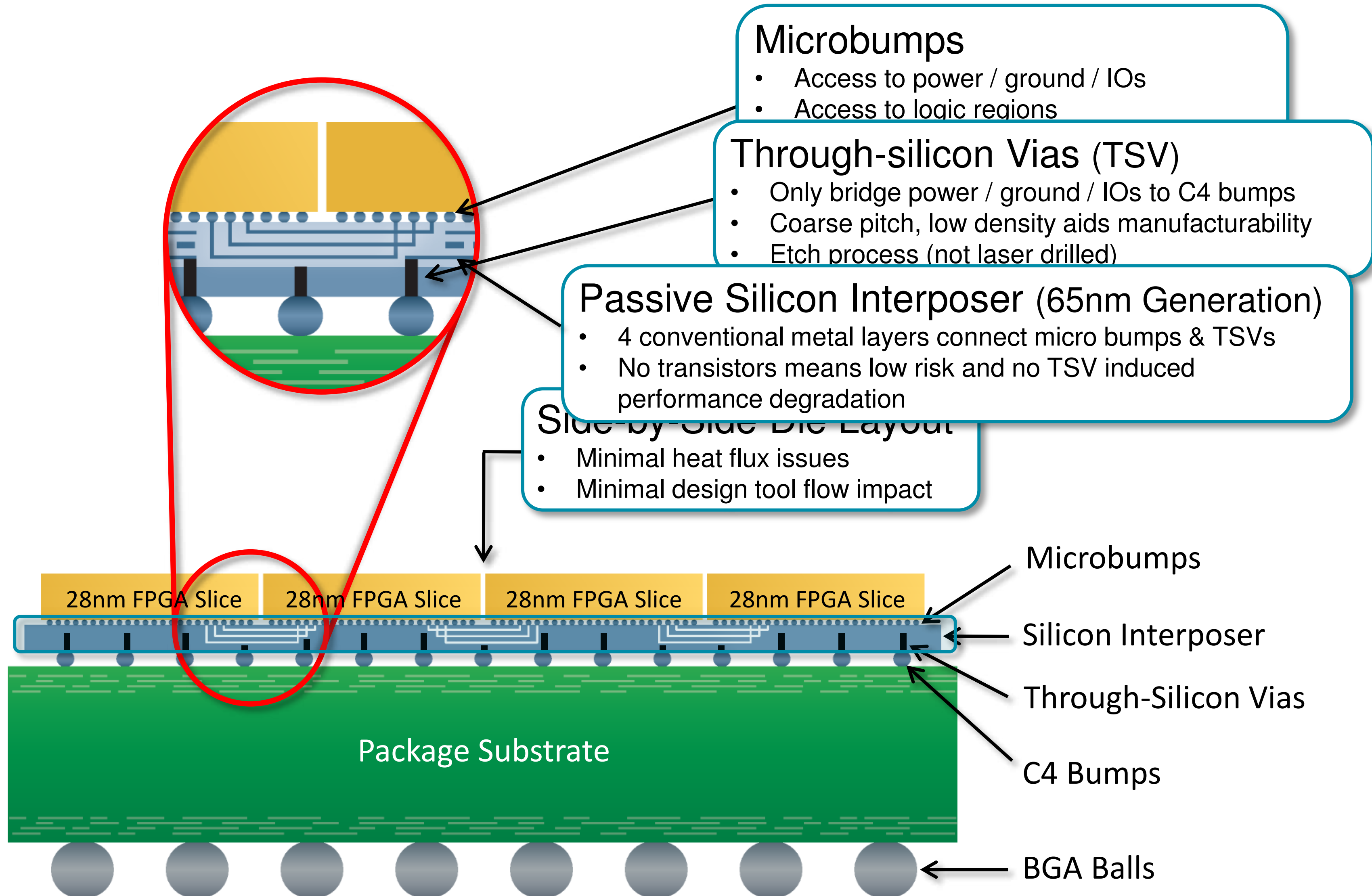
Well published technology boiler plate



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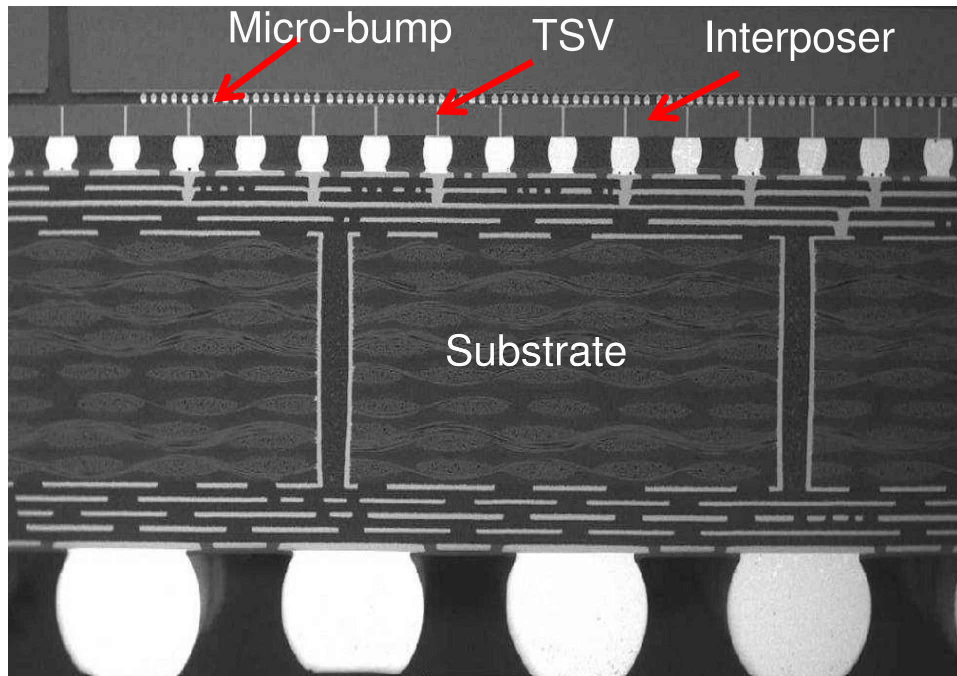
Cross-section of 28nm FPGA with SSI

Virtex-7 2000T

28nm Active Die + 65 nm Passive Interposer



Courtesy of Xilinx, TSMC, Amkor

Interposer /Package Technology

Technology	Specs
M1-M4	2um pitch 4 4X layers
TSV	12um diameter & 180um pitch
Micro-bump	45um pitch
C4	180um pitch
Package	6-2-6 Layer, 1.0 mm BGA pitch

- **Low risk approach to integrate TSV & u-bump**
- **High density micro-bump for ~50K chip-to-chip connections**
- **Better FPGA low-k stress management with silicon interposer**

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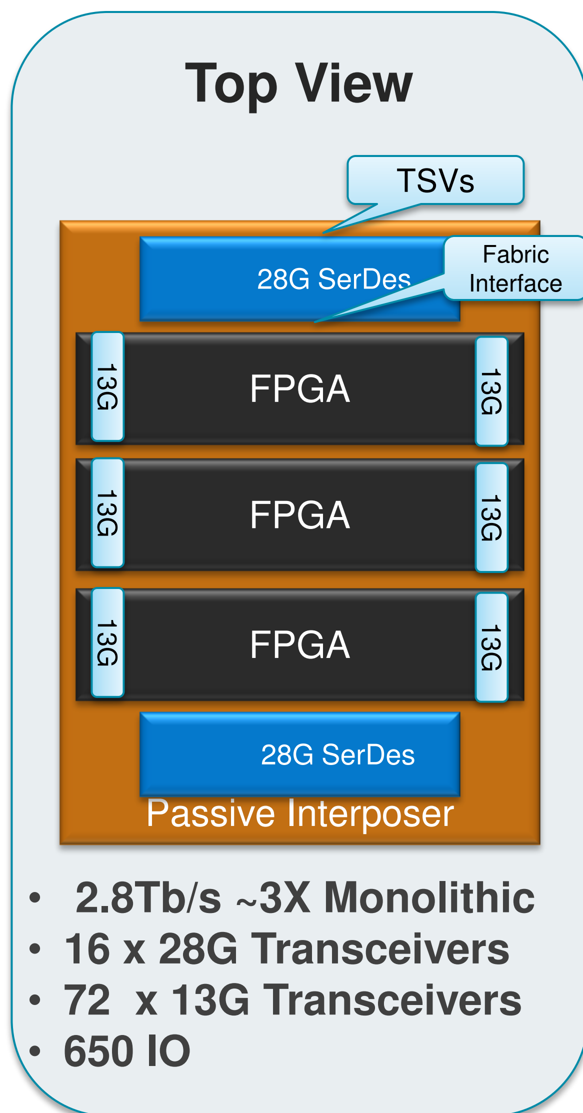
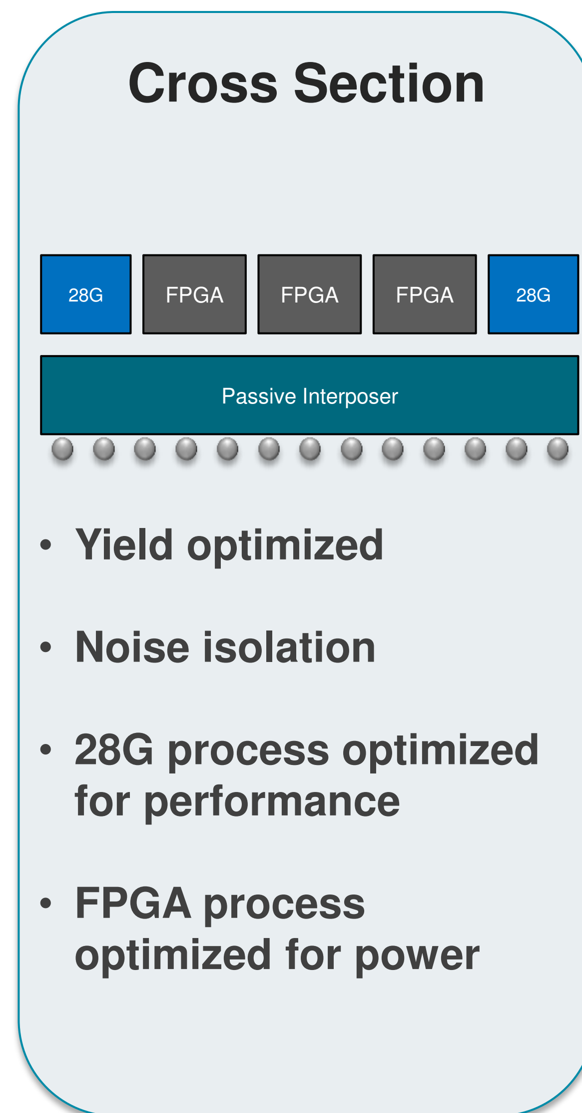
Heterogeneous FPGAs with SSI
Virtex-7 HT





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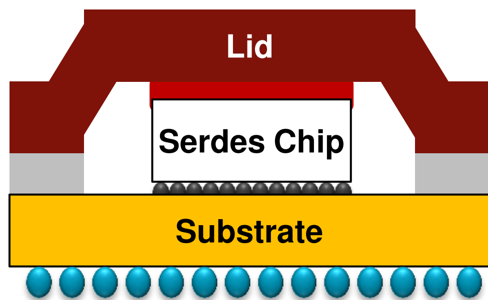
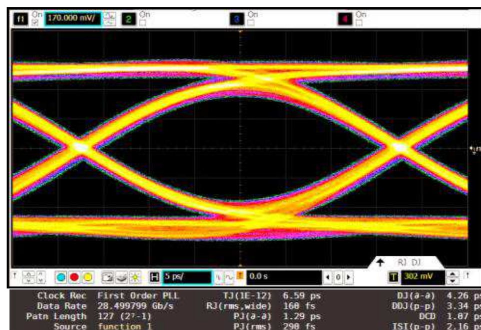
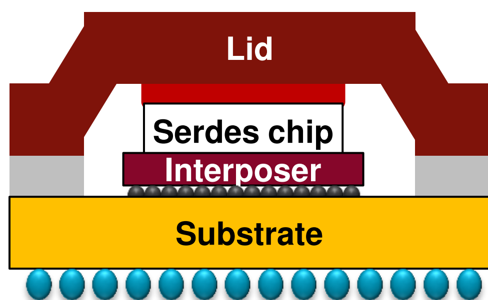
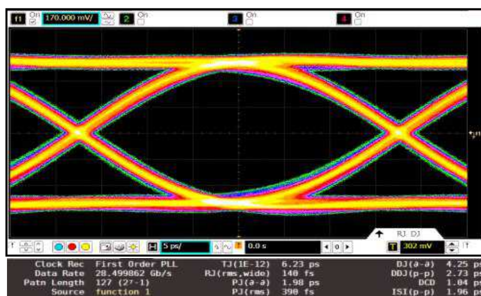
2.5D Performance vs. Monolithic





Vehicle 1 - Monolithic packaged 28Gbps Serdes





Vehicle 2 - 2.5D packaged 28Gbps Serdes

- **Measurements show 2.5D comparable performance to Monolithic die**

- Diagrams not drawn to scale

Reduced noise and better performance margin with SSI

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2.5D / SSI Takeaways

- **SSI Technology summary**
  - Capacity beyond Moore's law, Faster yield curve
  - Breaks die to die IO bottleneck
  - Heterogeneous SOCs
  - Power advantage
  - Stepping stone to true 3D

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SSI Implementation Overview

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Challenges for 3D design and validation

- **What areas of design validation and sign off are challenging for 3D and why?**
  - Circuit Design and Schematic capture
  - RTL, Physical Design of Top Die and Interposer
  - Extraction
  - Functional and Physical Verification (LVS, DRC)
  - Chip level functional verification
  - STA
  - IR/EM/SI or other Electrical analysis
  - Assembly and Yield (beyond the scope of this presentation)

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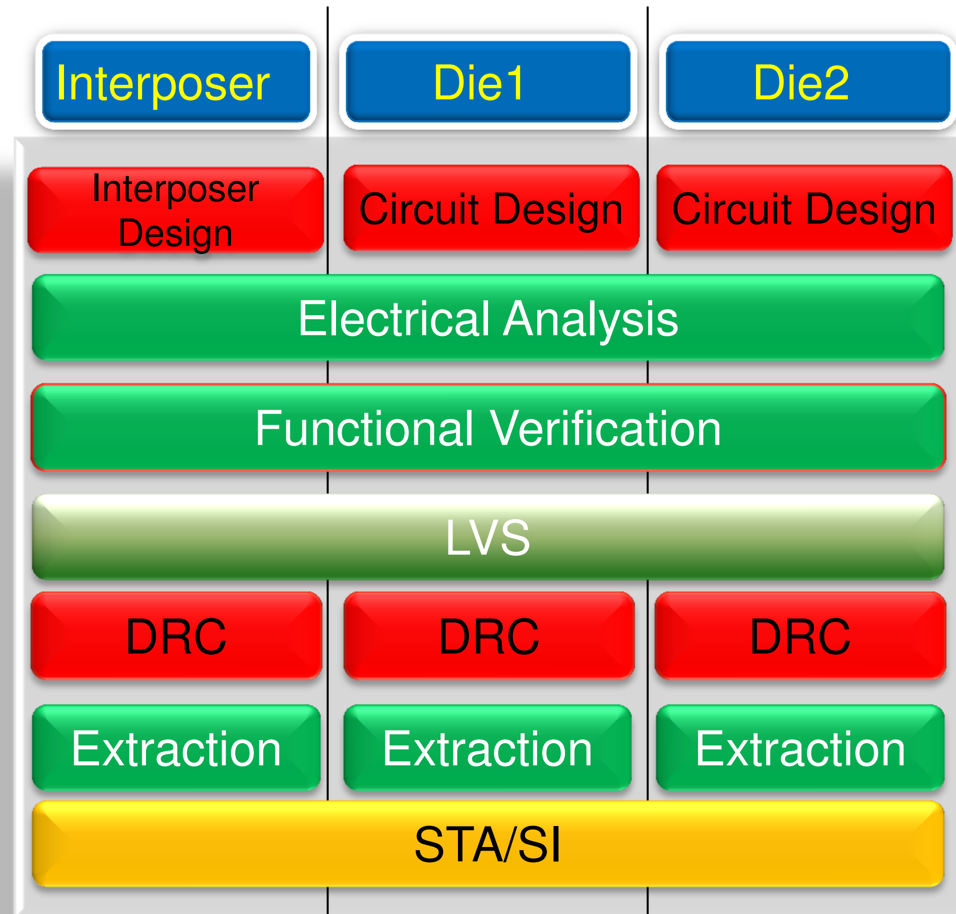
Analysis and Sign off

State of EDA tools

1. Can the analysis be split into hierarchical independent levels?
2. Can the data for analysis be split into hierarchical independent levels



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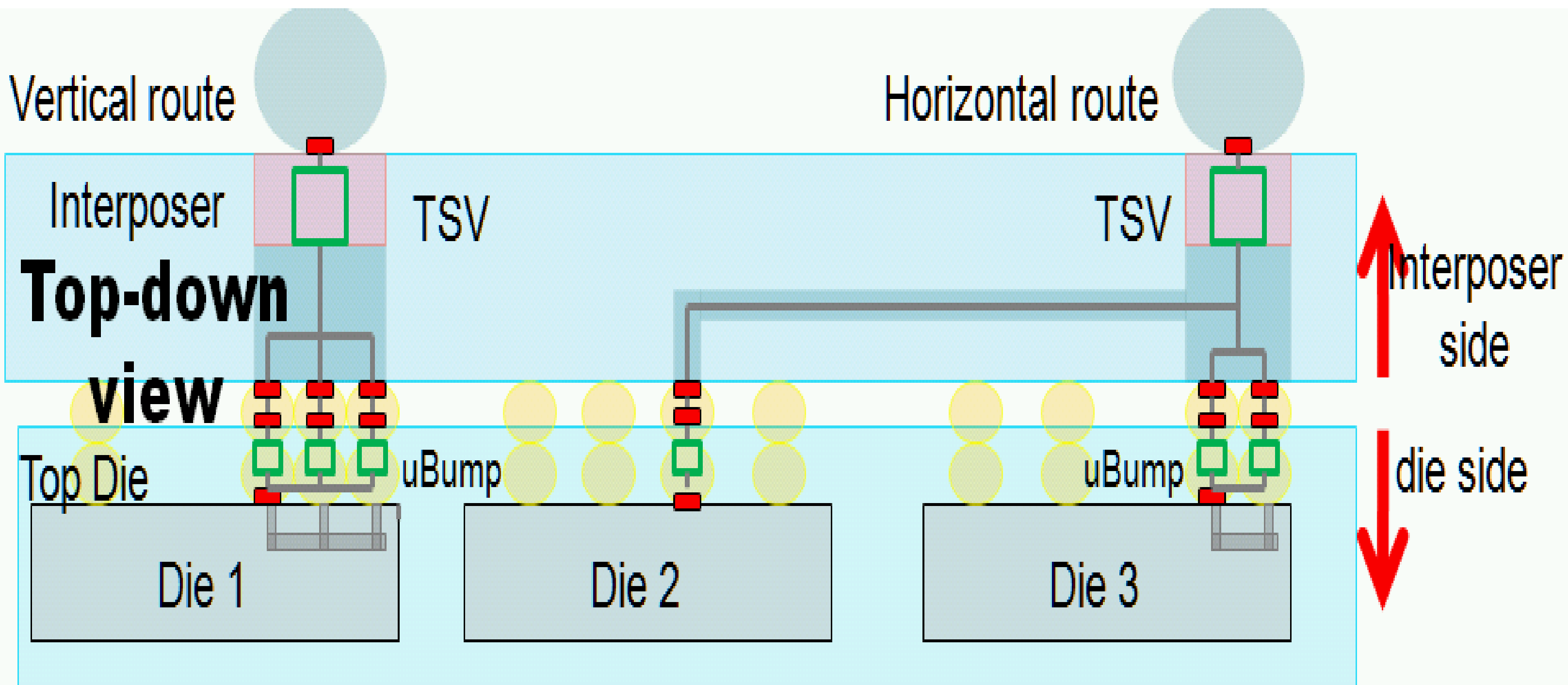
SSI Full chip



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Circuit and Physical Design

- **Circuit Design and Schematic capture**
  - Electrical modeling of Interposer
  - Design of driver and receiver
  - HSPICE Simulations with process models from multiple process nodes
  - Signal Integrity analysis
  - ESD considerations
- **Physical Design, Extraction and Verification**
  - Manual vs. Auto-routed Interposer
  - Like Top Die (e.g. all FPGAs) vs. unlike Top die (FPGAs, w/ 28G SerDes)
  - Extraction of Interposer layout
  - LVS done on each Top die and multiple die together;
  - DRC done on Interposer and Top Die separately

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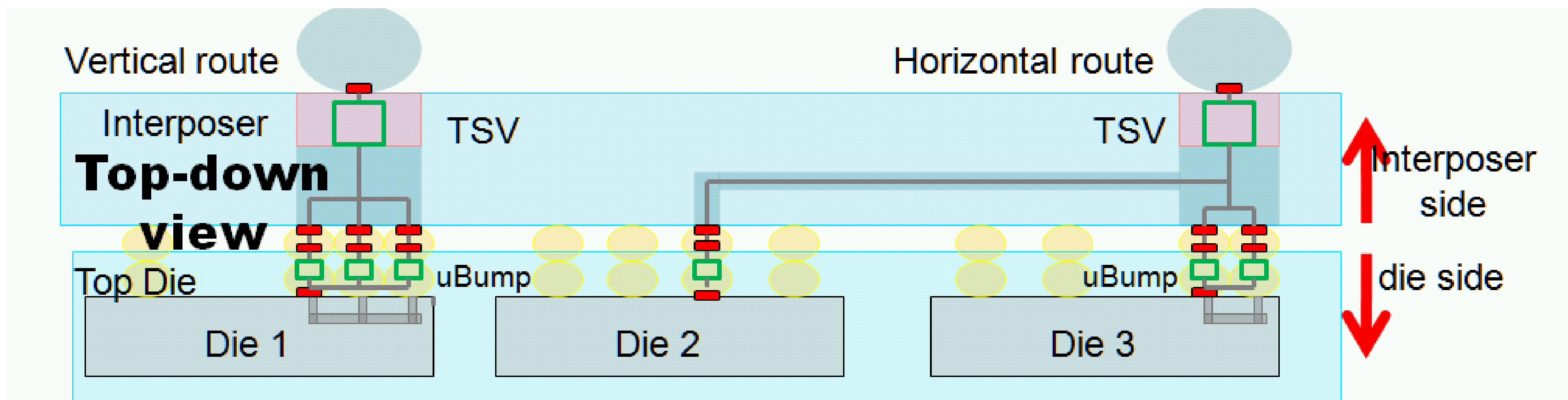
Static Timing Analysis

- **STA**
  - Black box ILM generated for each die
  - Full chip netlist (w/ extracted Interposer) generated using internal scripts
  - Special consideration given to the process distribution



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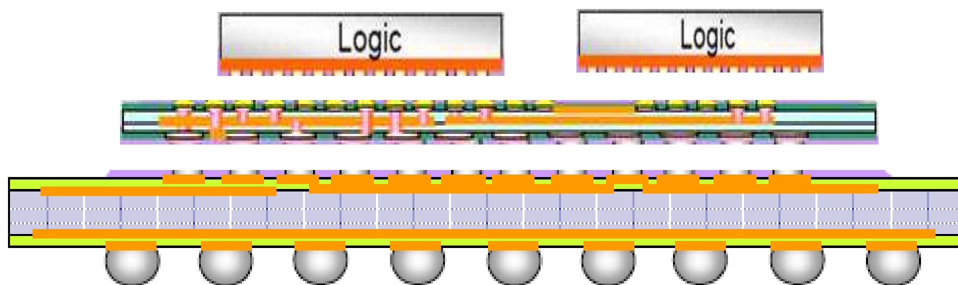
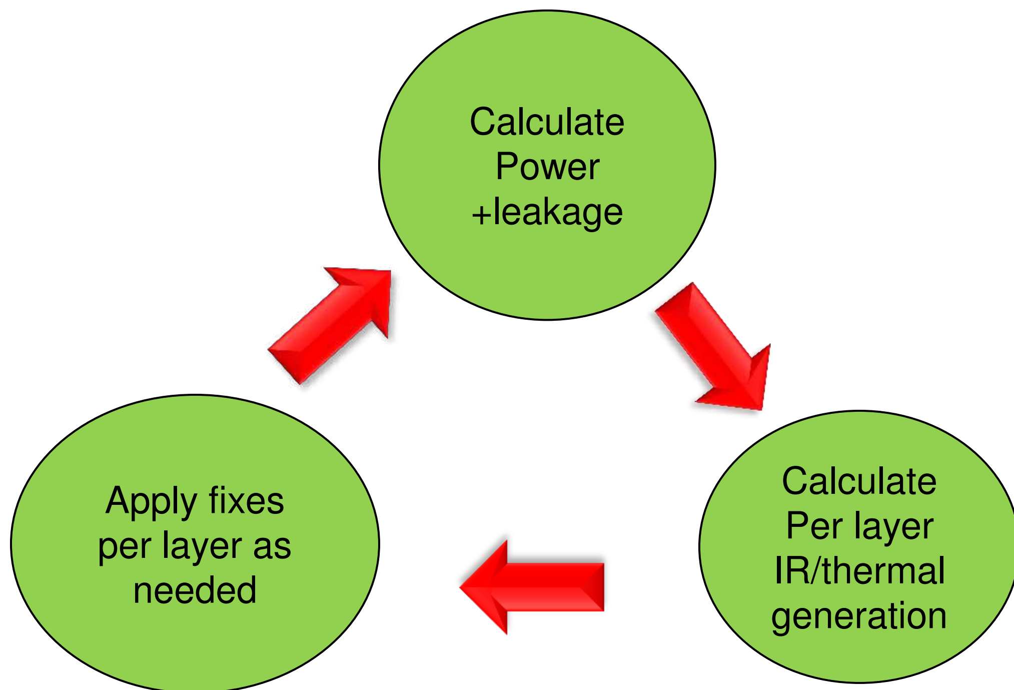
EM/IR and Thermal Analysis: Challenges





EM/IR by budgeting

Accurate EM/IR and thermal analysis is iterative in stacked Die Scenario.

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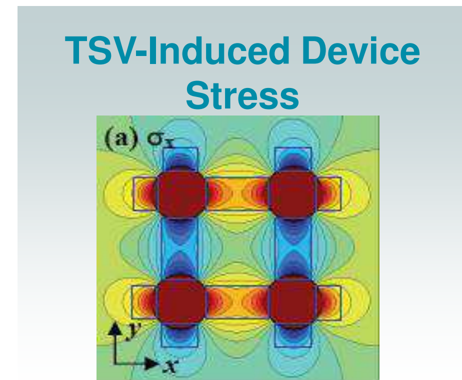
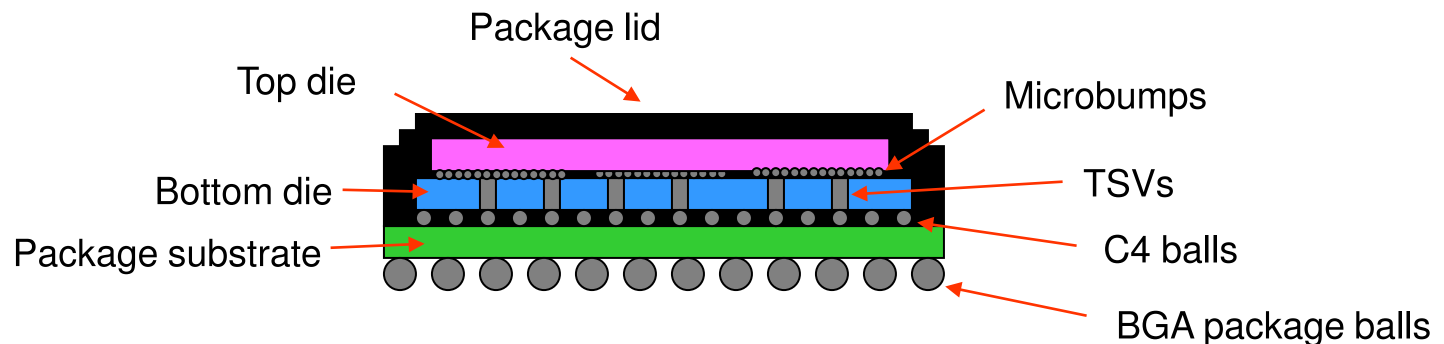
3D: The next frontier

- Higher performance chip stacked on top
  - Thermal considerations
- Bottom die includes power TSV's for top die
  - Can be in older, "TSV-friendly" technology
- Floor-planning is critical:
  - Thermal concerns (stacked thermal flux)
  - TSV keep out zones may be required in bottom die to avoid stress-induced performance impact





Assembly Technology still evolving

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Call-to-Action: Develop & Evolve 3D Standards

- **Design enablement**
  - Interposer Models
  - EDA Tools for 3D development and verification
  - Chip-to-chip interface standards
- **Manufacturing standards**
  - DFM rules for TSV, microbump
  - Materials: TSV, u-bump
  - Thermal budget
- **Test**
  - Test HW & u-bump probing
  - Known-Good-Die method
  - Self Test Required (FPGA programmability is an advantage)

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Conclusion

- **Bandwidth, power and cost demands are beginning to present significant challenges for monolithic silicon**
- **Stacked Silicon Interconnect is a breakthrough!**
  - Capacity
  - Connectivity
  - Power, Performance
  - Heterogeneous SOCs

SSI technology is the next big step in IC evolution

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Stacked Silicon Interconnect: A World of Difference

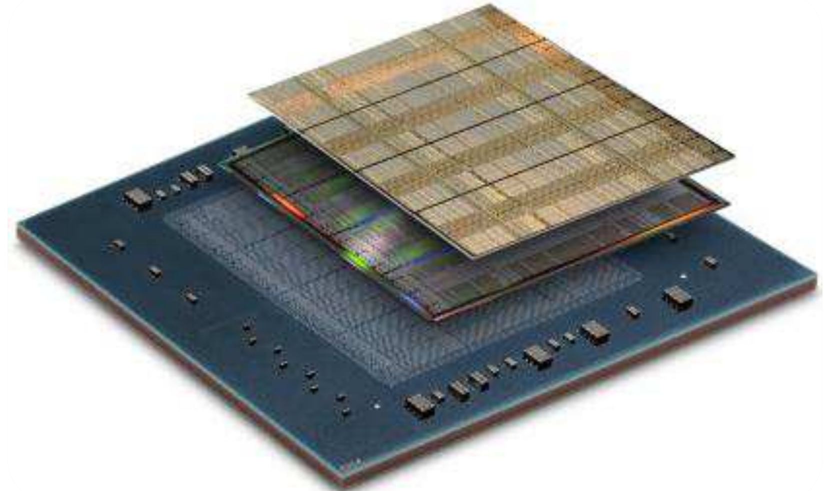
Earth

Area: ~500 Million km^2

Population: ~6.8 Billion People

Oceans: 5

Age: 5 Billion Years



Virtex-7 2000T

Interposer Area: ~775 mm^2

Population: ~6.8 Billion Transistors

Chips: 5

Age: 40 weeks

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