QUALCOMM CDMA Technologies

REDEFINING MOBILITY

Roadmap for Design and EDA Infrastructure for 3D Products

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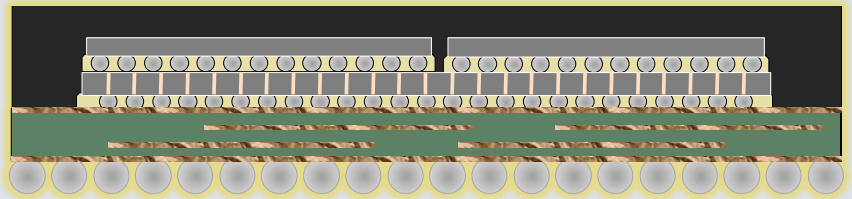
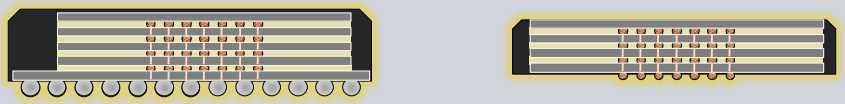
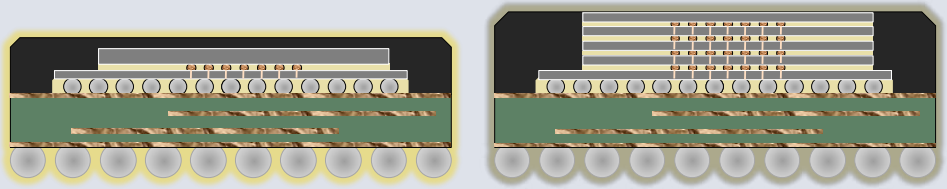
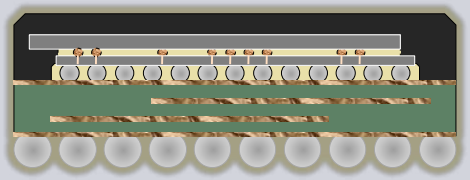
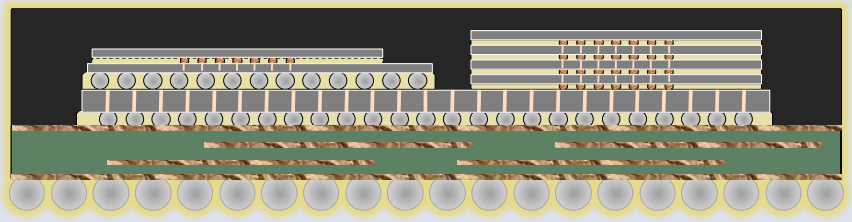
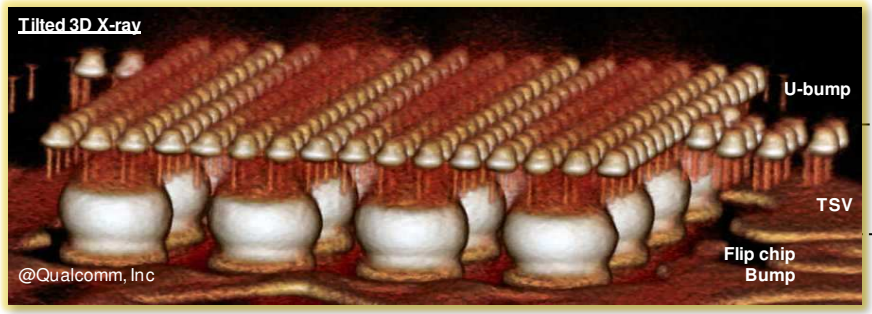
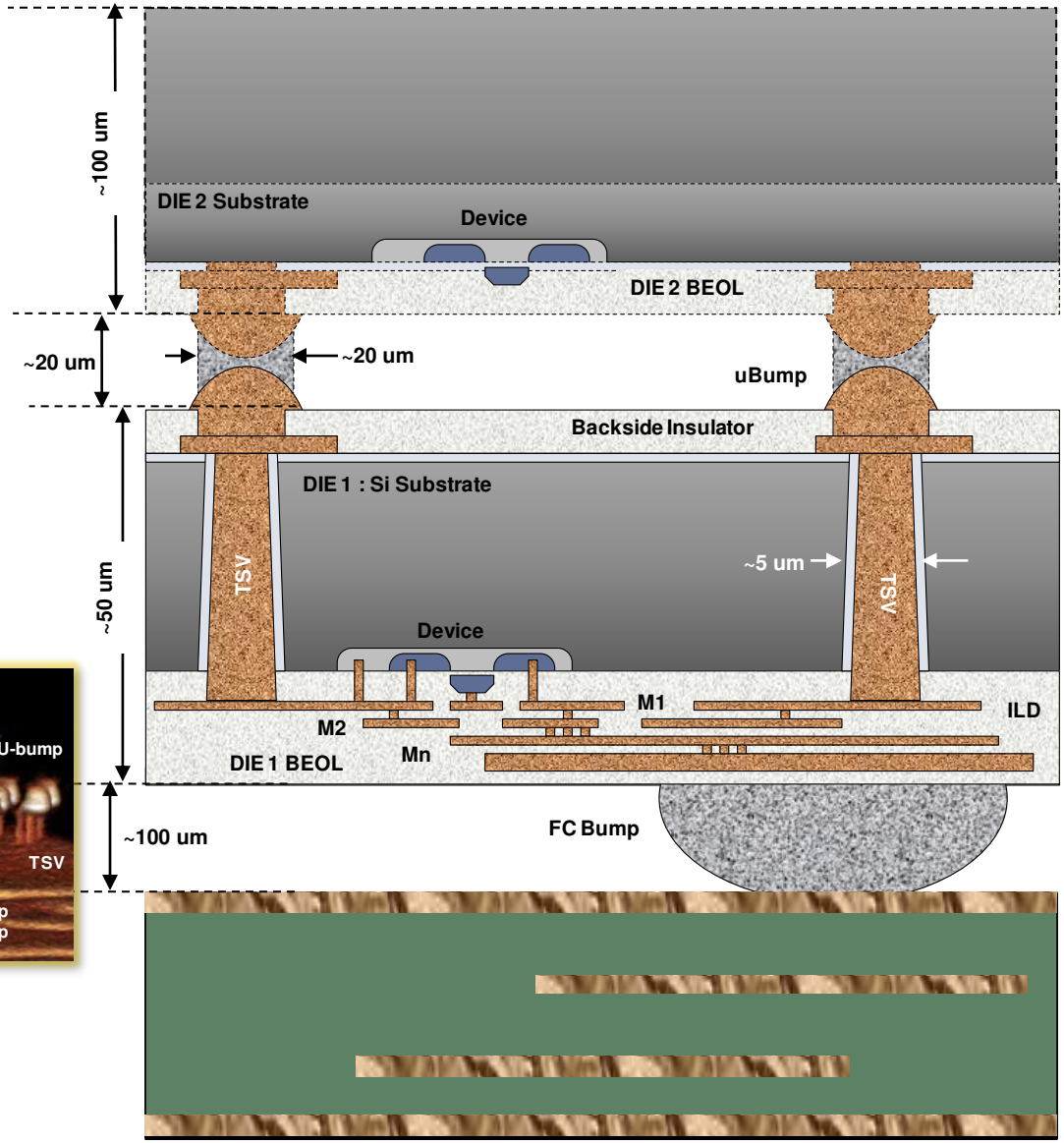
Some of the Typical 3D Options

2.5D	Side by side die stacked on a passive interposer that includes TSVs	
3D Memory	Multiple DRAM die stacked standalone or on an active interposer	
3D Memory on Logic	One or More DRAM die stacked directly on logic die (M-0-L)	
3D Logic on Logic	Multiple logic die stacked on top of each other (L-o-L)	
3D + Interposer	Mix of side by side and stacked schemes with a passive or active interpsr	

Evolving to “Mainstream” 3D Technologies

- For 3D stacking
  - e.g. Wide IO Memory on Logic
  - stacking orientation: F2B
  - TSV via diameter ~ 5u
  - wafer thickness ~ 50
  - uBump Array pitch : 40x50



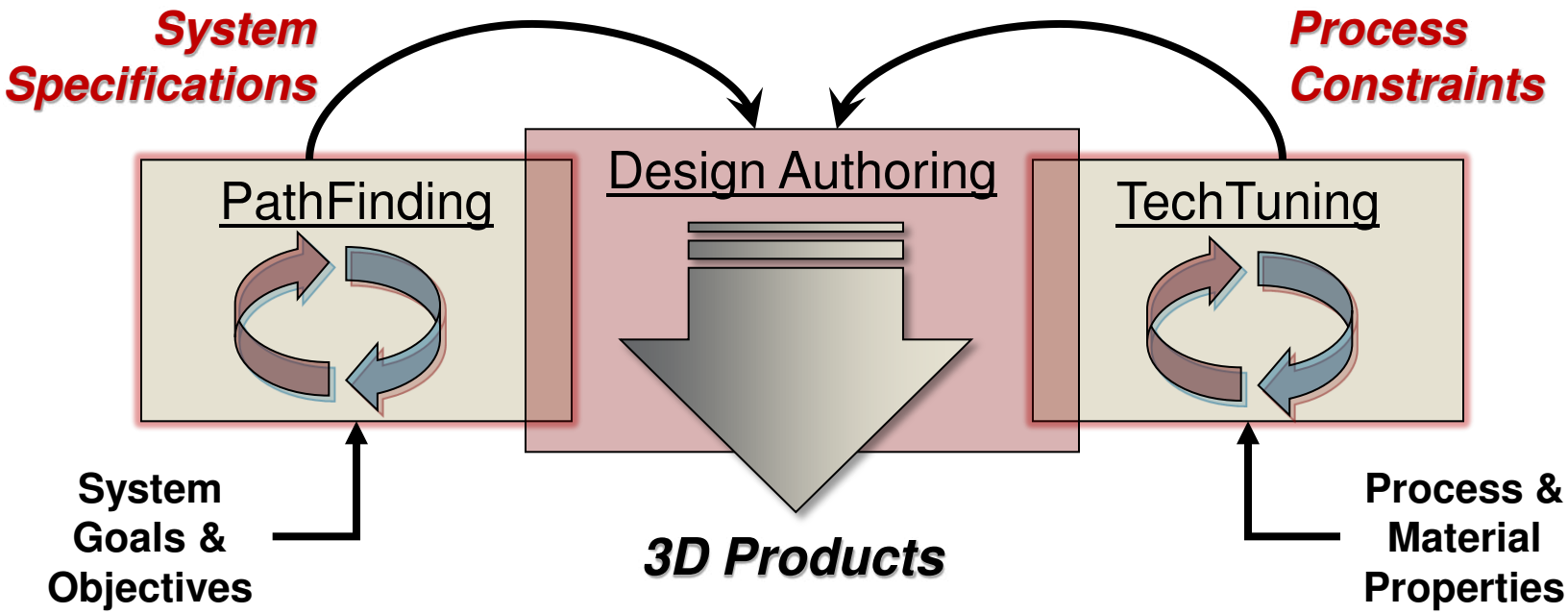


Snapshot of Intrinsic Technology Status

	Was (common concern a few years ago)	Is (our take)
Process	High aspect ratio (10:1) 5/50 TSV process	✓
	Thinning & Backside wafer processing	✓
	Microbump and Joining	✓
	Integration & Stacking	✓
	Intrinsic Reliability Assessment	☛ in flight
	Standards (JEDEC, SEMI, Sematech, 3D EC, …)	☛ in flight
Design (M-o-L)	EDA tools (for "2D-like" Memory-on-Logic design)	☛ mostly
	Design Enablement (for "2D-like" Memory-on-Logic design)	✓
	Testability (for "2D-like" Memory-on-Logic design)	✓
	Variability (Corner for "2D-like" Memory-on-Logic design)	✓
	Standards (JEDEC, Si2, IEEE …)	☛ in flight
Product	System Level Value Proposition	✓
	Thermal Modeling & Design for Thermal	☛ in flight
	Stress Modeling & Design for Stress	✓
	SI modeling & Design for Parametric Yield	✓ in flight
	Cost Structure & Business Models	TBD
	Yield and Yield Learning	TBD
	Volume Manufacturing Ramp	TBD

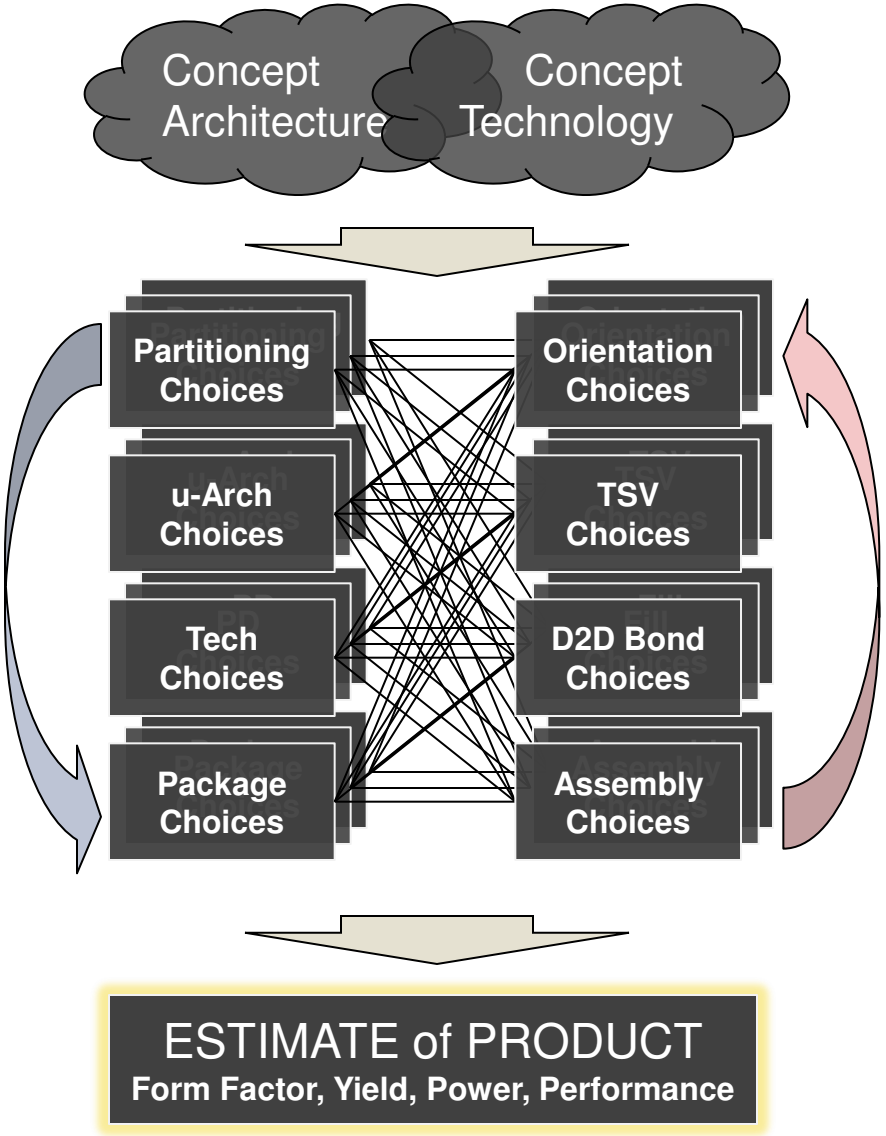
Eco-System for 3D Design

- **Segment Design Eco-System into 3 Buckets to Address 3 Key Challenges**
- ***Design Authoring* – actual chip design**
  - Implement Design via (mostly) Traditional 2D Chip Design Flow (RTL2GDS))
  - Output GDS
- ***PathFinding* – design/technology concept exploration**
  - *Manage Choices* via Cheap, Quick & Dirty Concept Design
  - Output Clean Specs
- ***TechTuning* – physical space exploration**
  - *Manage Interactions* via Cheap, Electrical, Thermal & Mechanical Chip Simulation
  - Output Clean Constraints



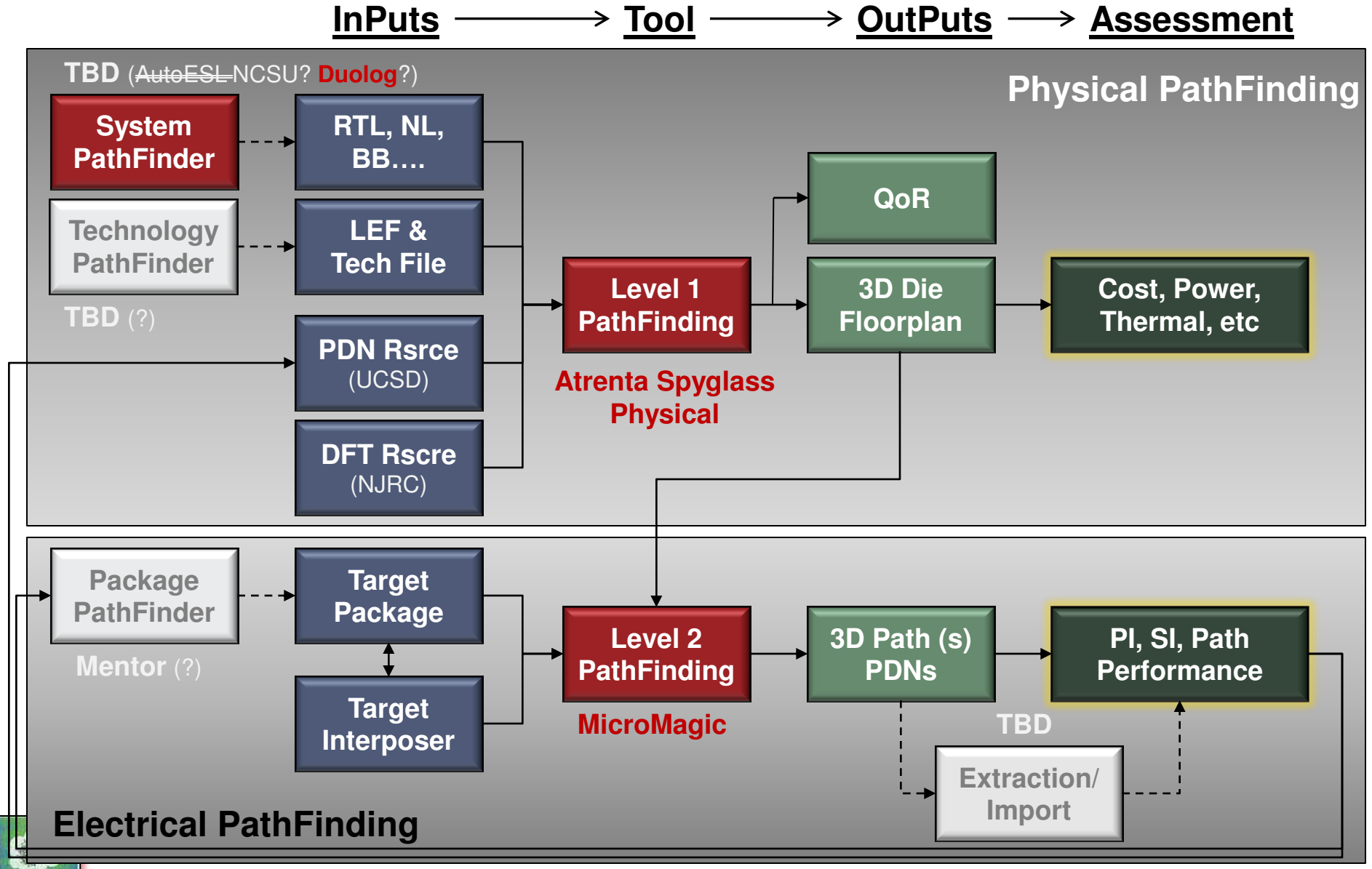
PathFinding: Why & What ?

- Managing Choices ….
  - Want to optimize product attributes
  - Cost, power, performance, engineering …
- Need to Co-Optimize Process & Design
  - Winning 3D Product will Be Architected specifically to Leverage 3D Technology
  - Selection of choices is Product Specific
- In General: Need Spatial Awareness
  - Quick and flexible
  - Hi fidelity vis-a-vis accuracy
- For 3D : Also Need Heterogeneity
  - Multiple stacking styles & orientations
  - Multiple tech files
  - Multiple levels of hierarchy
  - Multiple resource constraints
- Structured Methodology.
  - Past experience not applicable
  - Opportunity for paradigm shifts
  - Not tied to Legacy design
  - Process-Design-Package co-optimization



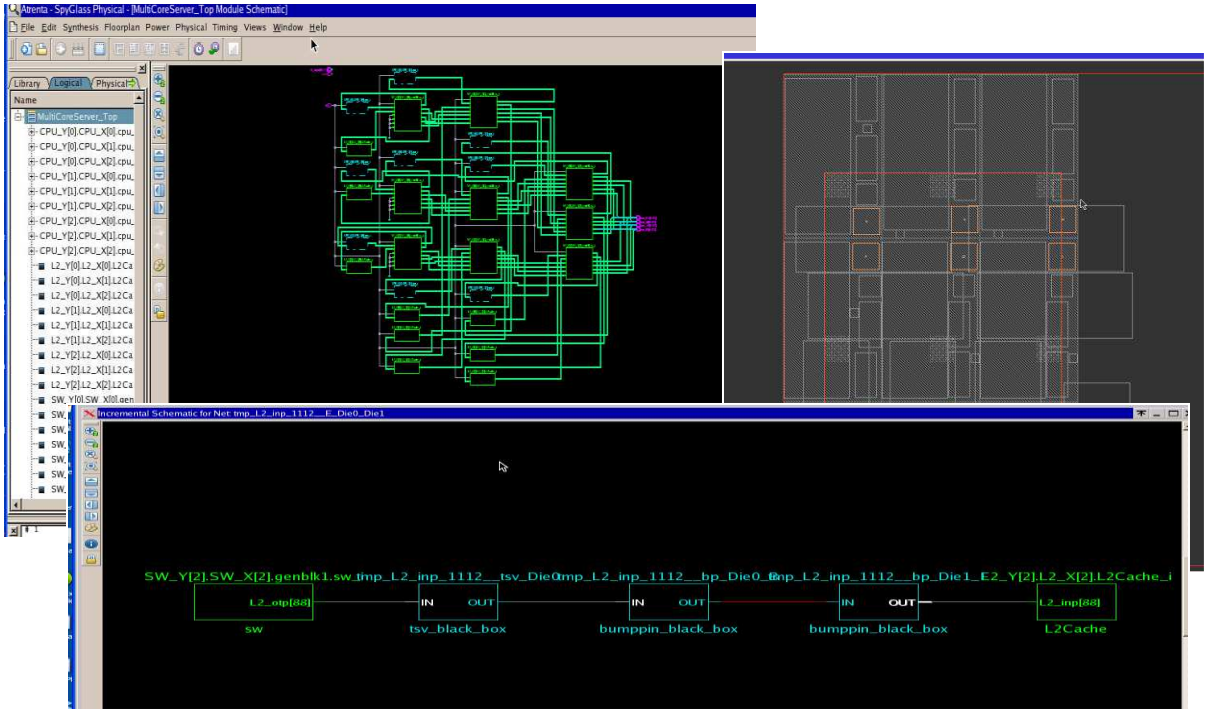
Details :3D System Integration, Springer 2011

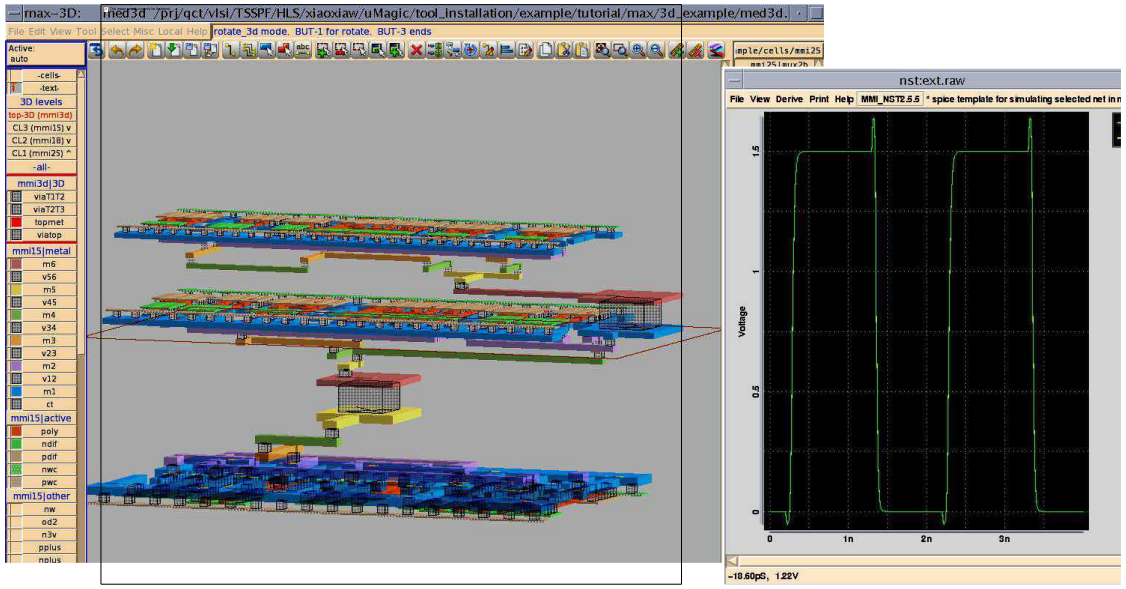
3D PathFinding : Current View



PathFinding

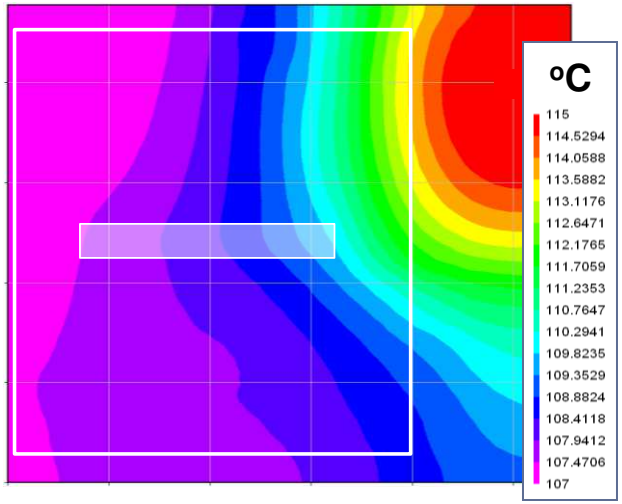
- Level 1 (Atrenta): think
  - RTL & Netlists
  - Block Level Schematics
  - Partitions
  - Block assignments
  - T2T connectivity
  - Global Routing
  - Floorplans
- Level 2 (MicroMagic): think
  - Transistor Level Schematics
  - T2T layout
  - SPICE Netlist
  - Waveforms
  - Polygons
  - GDS

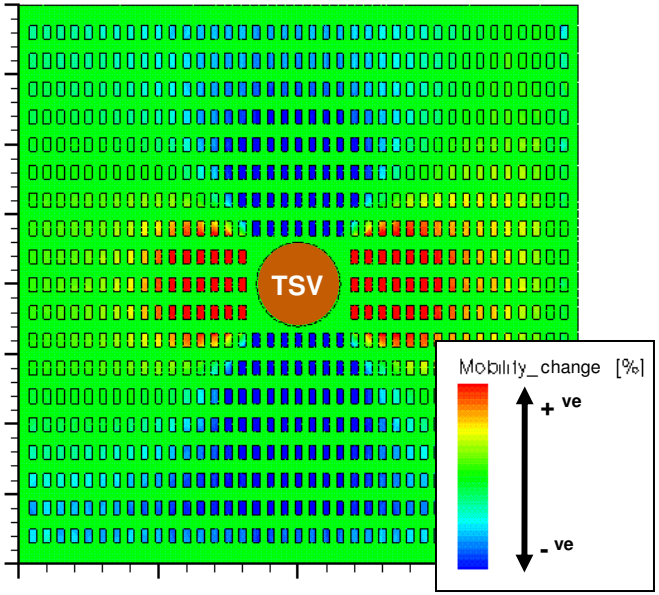




TechTuning: Why & What ?

- Managing Interactions
  - Intimate Proximity and Coupling Between Die
  - In Electrical, Thermal & Mechanical Domains
- Electrical Domain Interactions
  - Within Die Interactions with New Features
    - Substrate noise, Coupling etc..
  - Die to Die interactions (SI, PDN, PI…)
- Thermal Domain Interactions
  - Within a Die & Die to Die
  - Need Thermal Rules & Guidelines
    - Design Specific & Technology Specific
    - Need a methodology to plug into std design flow
- Stress Domain Interactions
  - Within a Die & Die to Die
  - Need Thermal Rules & Guidelines
    - Design Specific & Technology Specific
    - Need a methodology to plug into std design flow

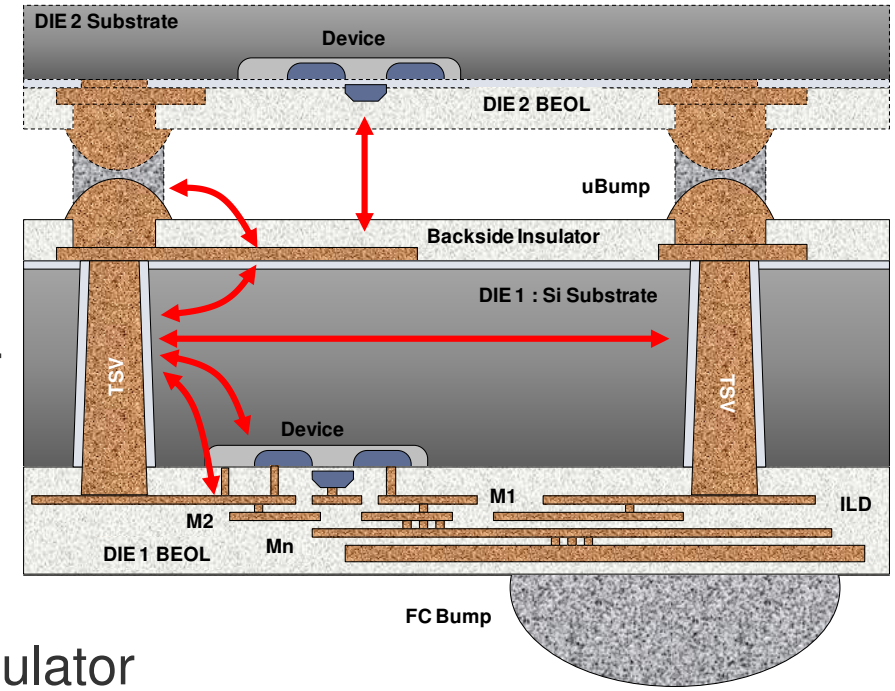




Details :3D IC Stacking Technology, McGraw Hill 2011

3D Electrical Interactions

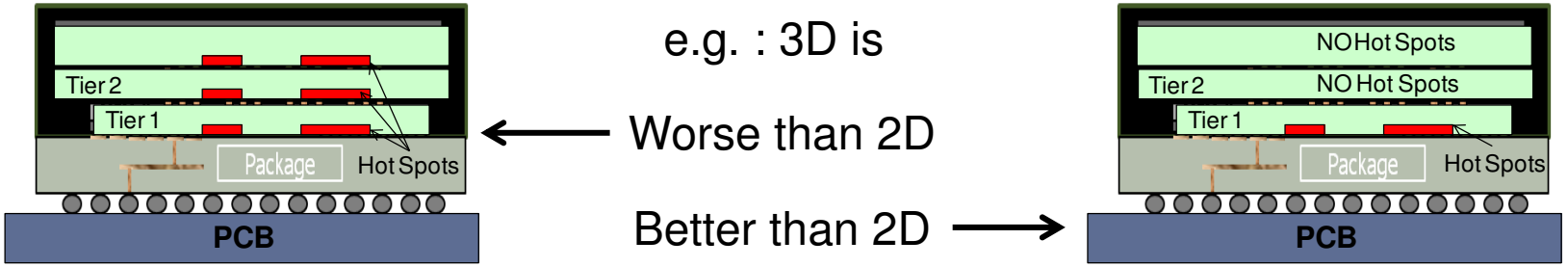
- Many Possible Interactions
  - Die to Die – close proximity
  - Within a Die – new features



- New Geometries: not just simply planar
  - uBump to BRDL
  - TSV to BRDL
  - TSV to TSV
  - TSV to M1
- New Features: not just conductor or insulator
  - MOS nature of TSV & Semiconductor nature of Si
  - e.g. Substrate Noise Coupling: TSV to Device
    - vs. substrate thickness
    - vs. Doping Profile in the Si substrate
    - vs. TSV to Device Separation
    - vs. Substrate Tap & Guard Ring Configuration
    - etc…
- Need true 3D Chip Level Extraction & Coupling Analyses
  - Or a restricted layout with pre-characterized macro model

Thermal Challenges => a Fundamental Constraint

- Thermal: a Global (=System Level) & Local (=Component Level) Challenge
  - Global Concern : must manage skin temperature and overall system power
  - Local Concern : must manage hot spots, junction temperature, and power density
  - Compounding Factor: all advanced systems use some form of Thermal Mitigation
- Thermal is not a 3D-only Challenge
  - A Problem that has to be addressed with 2D Components as well…
  - At Architecture, Design, Floorplanning, Packaging, Application, Software …
  - Could be a 3D Opportunity ?



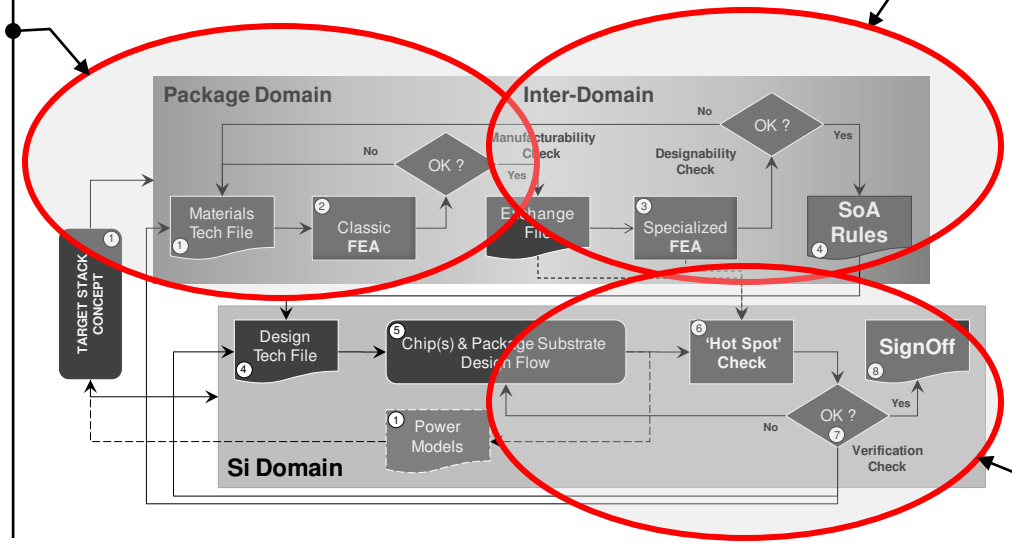
- Need a System-Chip Co-Design Methodology & Tools
  - Faster and More Flexible than the traditional CFD / FEA methodologies
  - Compatible with cross – company handshake (a la TDP practice in PC domain)
  - Compatible with fuzzy PathFinding-like forward looking inputs
  - Compatible with different system level 'knobs'
  - Compatible with different chip level 'knobs'

Implementation of a TechTuning Flow for Stress

- Interface to actual Design Authoring : **Rules now**
  - maybe in-flow model based simulation later..
  - Based on 'off-line' simulations using specialized tools
  - Define a 'Safe Operating Area' => a set of rules
  - Supplement with a smart 'hot spot' checker to close the loop

Traditional Simulation

✓FEA methodology
✓~1 to 0.01mm range
✓Hosted Model from AMKOR
✓Working on similar deliverable from ASE



Specialized Simulation

✓Submodeling & specialized FEA methodology
✓ μm to nm range
✓SNPS FAMMOS tool

"Hot Spot" Checker

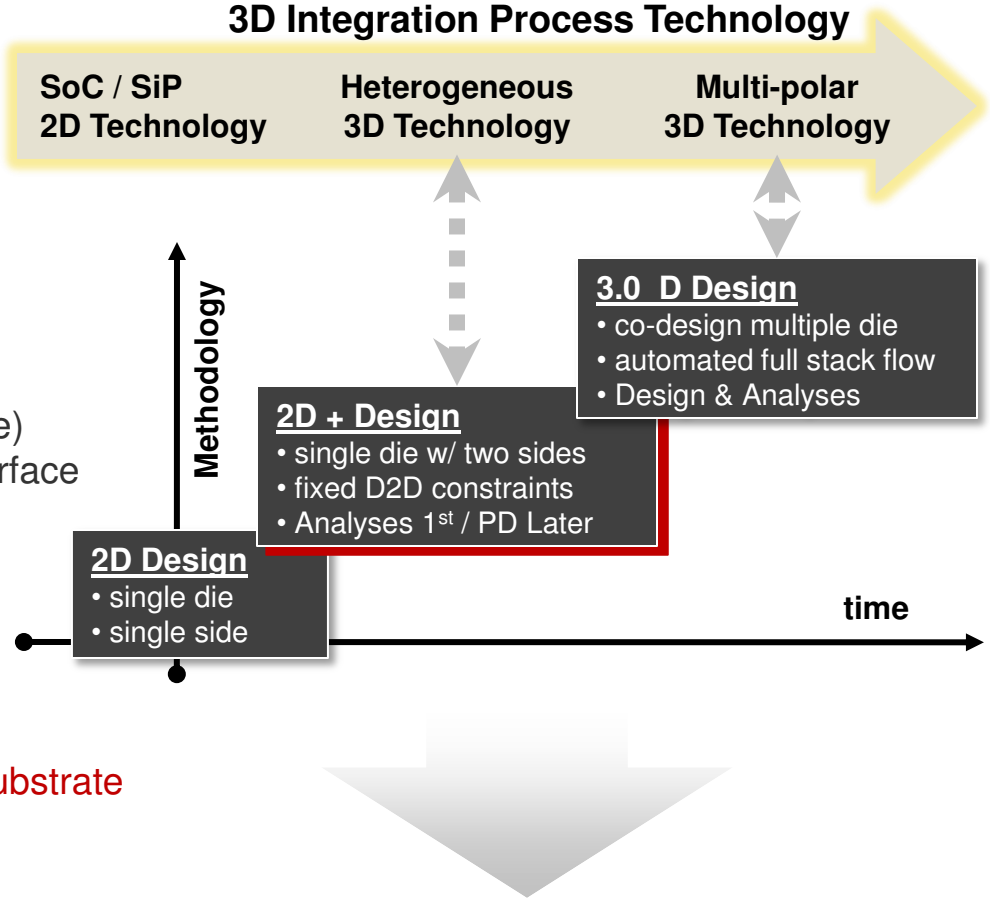
- Validation that bits and pieces fit & SIGN OFF the design
- Must interface to design environment : I/P : GDS2 , LEF, DEF …
- May have to be COMPACT MODEL Based (read the whole design and include all effects)
- Working with MENT

Managing Costs : What Does It Mean for TSS Design?

- Expect Gradual and Graceful Evolution
  - Process and Design – together / in synch
  - Significant investment in the existing flow
  - Will be Applications Driven

- Now : Heterogeneous Stacking
  - e.g. Memory (or Std Analog) on logic
  - Design Methodology Requirements
    - Partitioning : by die types w/ spec interface
    - Syntheses 1-die-at-a-time
    - Floorplanning : constraint from the other die
    - Physical Design : partial 2-sided die (maybe)
    - Physical Verification: 1-die-at-a-time + interface
    - Analyses : whole stack (eg PDN)

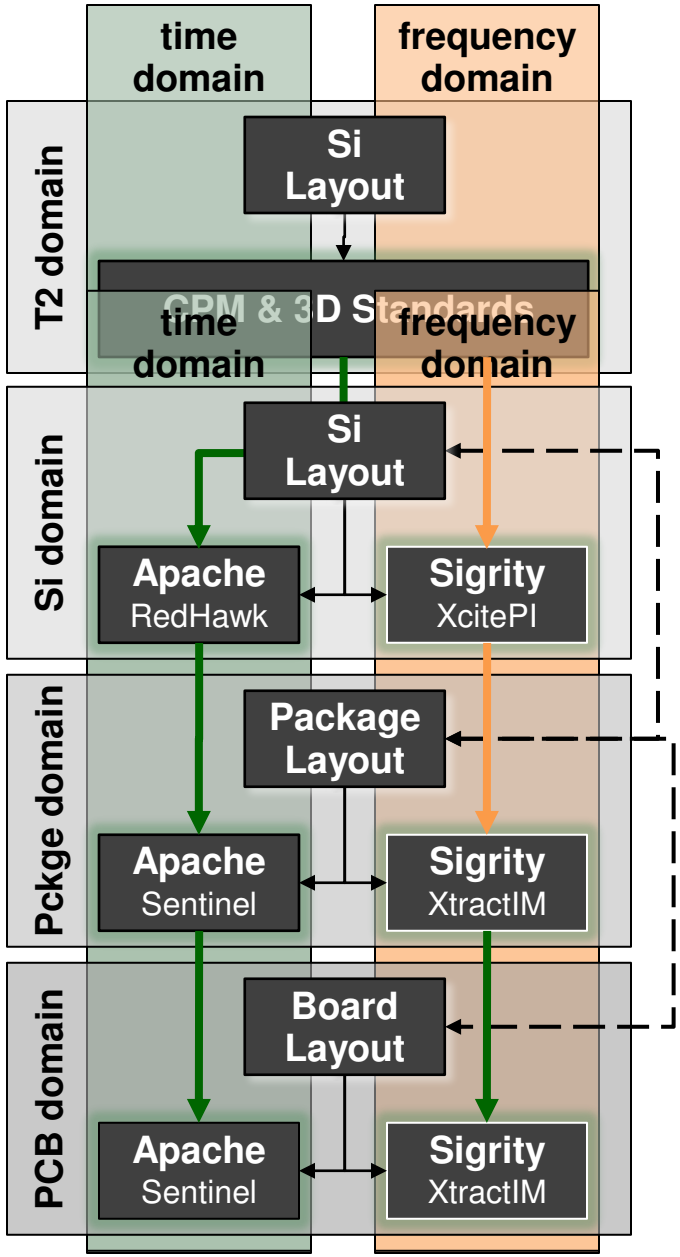
- Next : Integrated Stack Designs
  - e.g. Logic-on-Logic or Interposers
  - Design Methodology Requirements
    - Integrated PD Co-Design w Interposer & Substrate
    - Design Constraint Methodology
    - Design Authoring – including the Package
    - Manufacturability (aka TechTuning)



Evolving from 2D Design

3D PDN Design Flow

- 2D Ref Flow
  - Sign off in time domain (Apache)
  - Analyses in frequency domain (Sigrity)
- 3D PDN Flow Approach
  - ✓ Take as much as possible from ref flow
  - ✓ Similar approach as Si-Package-PCB Analyses
    - – Extract each tier separately
    - – Model as an integrated stack
  - ✓ Upgraded tools to understand new features
    - – TSV, uBump, BRDL, Tier n …
- Current Status
  - Demonstrated Tools & Flow
  - Supporting development of standard Compact PDN Models and associated 3D Design Exchange Format Standards



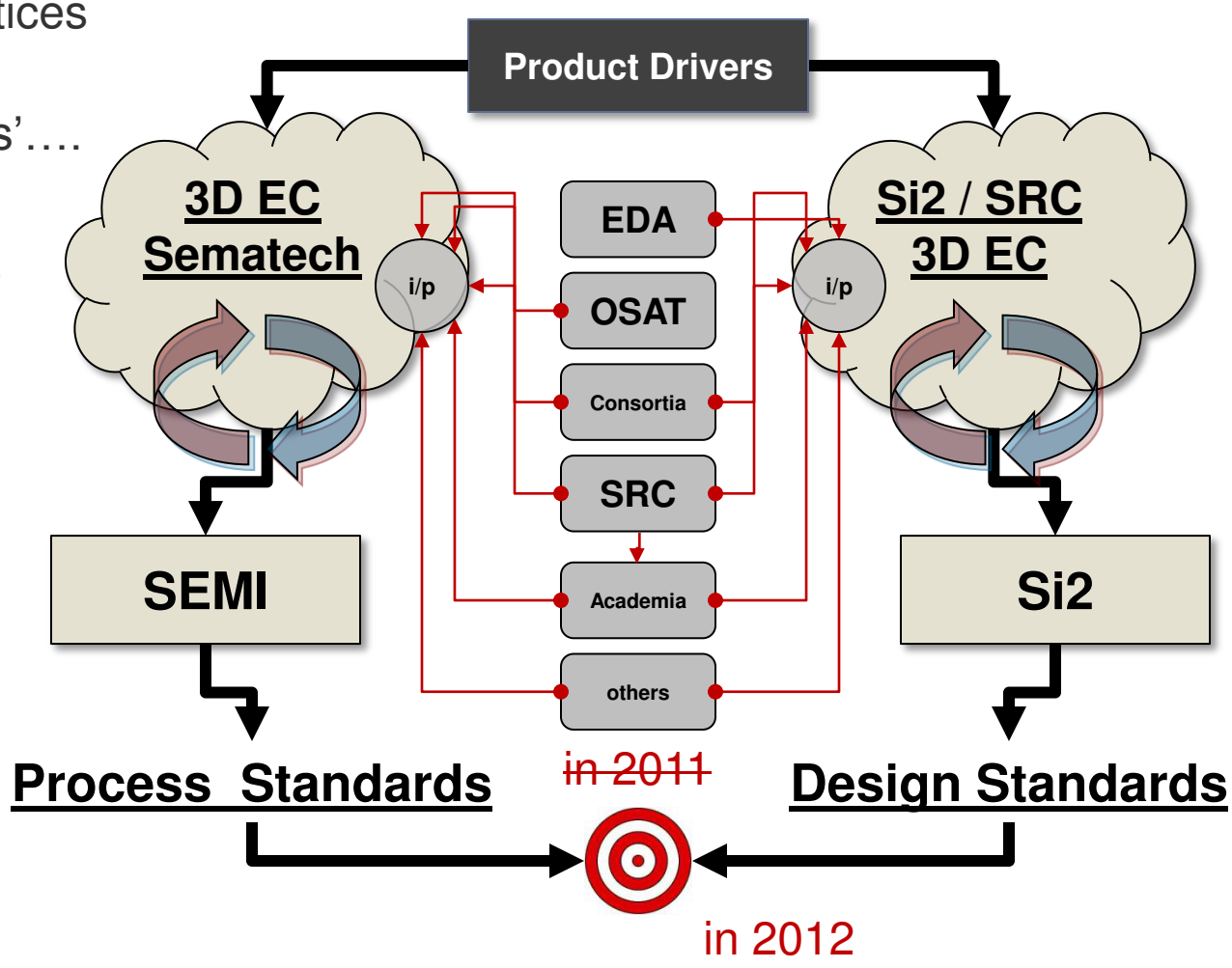
Inventory of Current Core Design Technologies

	PathFinding	TechTuning	Design Authoring
Things We Do Have	✓ 3D Floorplanner ✓ 3D Net generator ✓ PDN resource estimator	✓Package Stress simulator ✓Feature Stress simulator ✓Reference Thermal sim.	✓2D design flow & tools ✓Timing with a fixed TSV/uBump layout ✓ 3D aware PI / SI analyses
Things We are Working On	• Package PathFinder • System PathFinder • Standard 3D design exchange formats	• Chip Level Stress Sim • Chip thermal floorplanner • Standard 3D design exchange format & PDK	• M-o-L product design • 3D Variability Flow • Standard 3D design exchange formats
Things we do NOT Have (and wish we did)	Technology PathFinder	3D in flow substrate coupling analyse Fully supported TechTuning "PDK' System component thermal co-design	TBD Logic on Logic TBD Interposer TBD 3D Extraction TBD 3D ++ (see below)

- We don't have Everything – but we do have much more than Nothing ☺ !!

Standards : a Lubricant for the Supply Chain

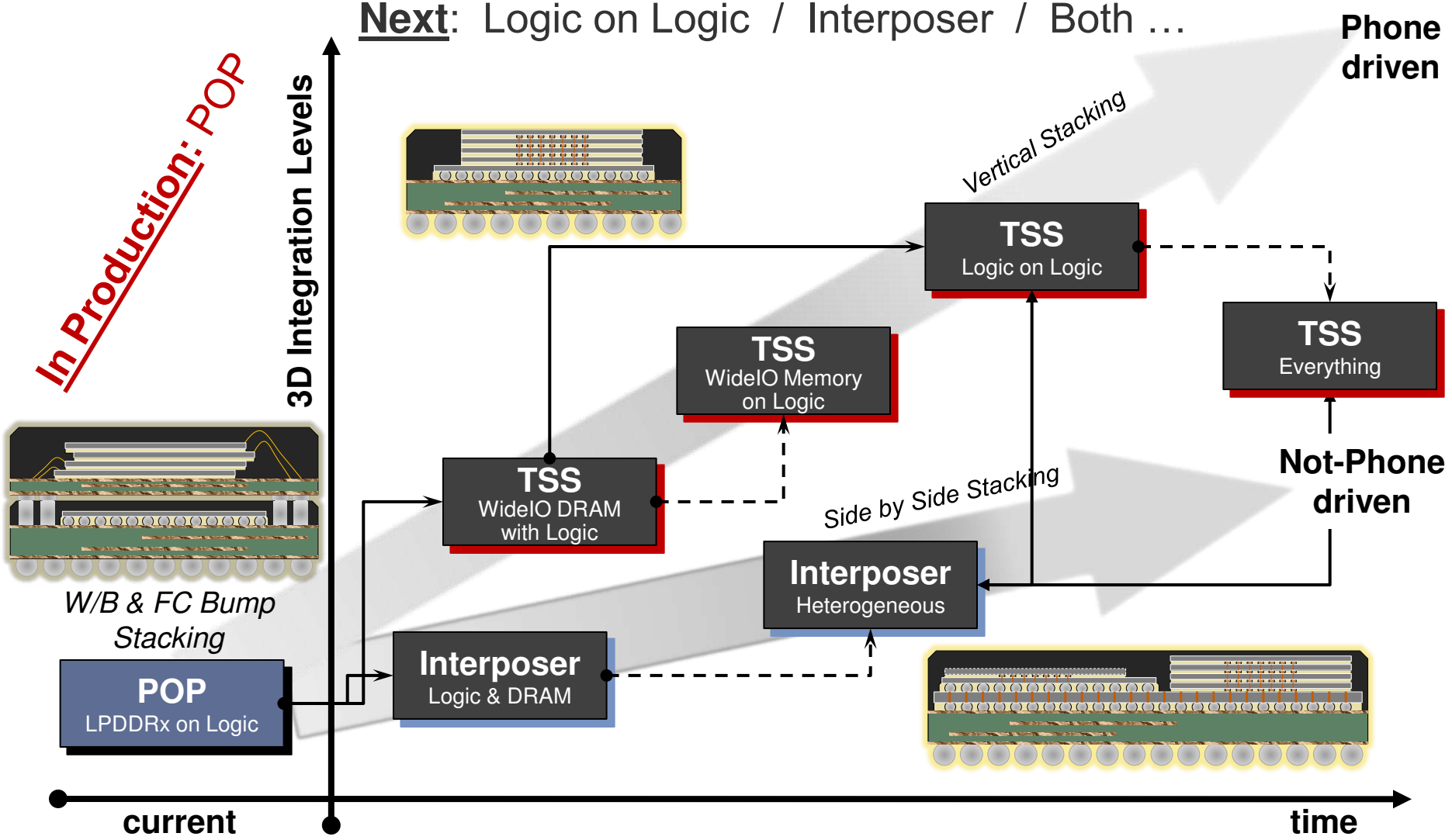
- **Leverage Existing Standards Bodies**
  - Established balloting, adoption and management practices
  - But formal and hence need 'mature proposals'….
- **Process Standards**
  - 3D Enablement Center
  - Sematech
  - SEMI …
- **Design Standards**
  - Si2
  - 3D EC / SRC
  - IEEE
  - JEDEC…
- **Encourage Participation by the Industry – esp EDA**



2.5D / 3D Stacking Roadmap

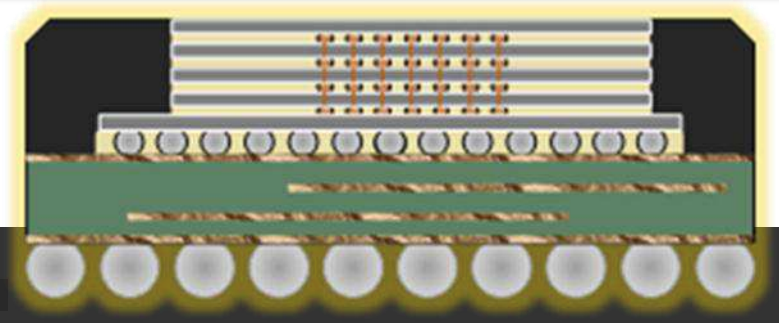
Our Current Focus: Wide IO DRAM on Logic = TSS

Next: Logic on Logic / Interposer / Both …



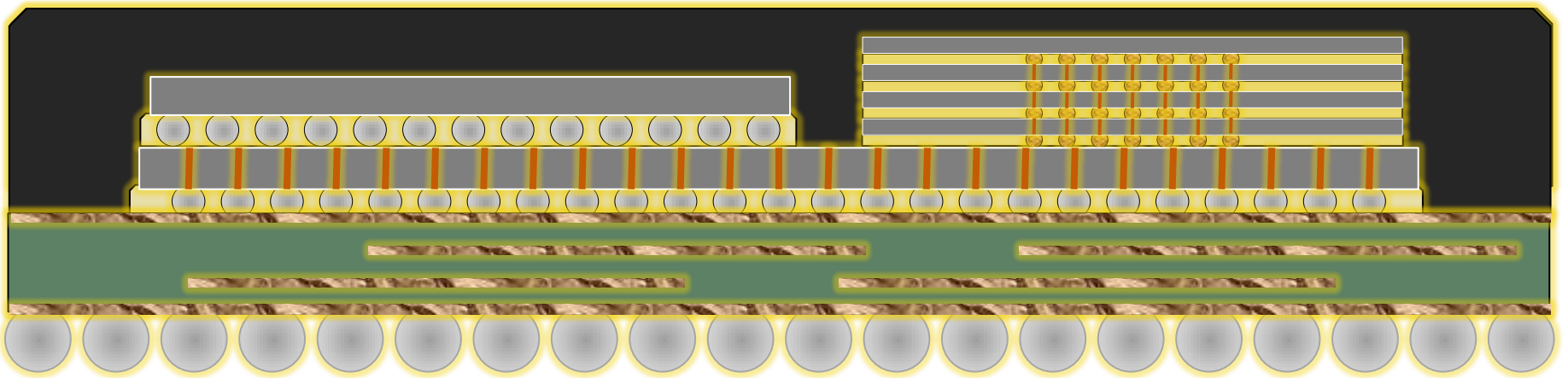
Design Environment for Memory-on-Logic

Status	Arena	Item
Have	**Design**	✓ 2D design flow & tools + quasi-manual placement of T2T / TSV array + custom T2T buffer design & incremental rules to manage interactions
	Timing	✓ 2.5D analyses flow & tools + compound 'lumped' TSV delay model
	PI	✓ 2D analyses flow and tools + extended hierarchy + recognition of new features
	SI & Variability	✓ 'Off Line' analyses to produce set of 'keep out' rules
In Flight	**'In Line' Rule Checkers**	✓ Chip Level Stress Simulator – for 'stress Hot Spots' ✓ Chip Level Thermal Floorplanner ✓ Chip Level SI Simulator
	Integration w/ Commercial Die	✓3D Design Exchange Formats
Like to Have	**SI Analyses**	In Flow SI analyses – on line and in product flow
	TechTuning & PathFinding	Fully supported TechTuning "PDK' System-Component thermal co-design



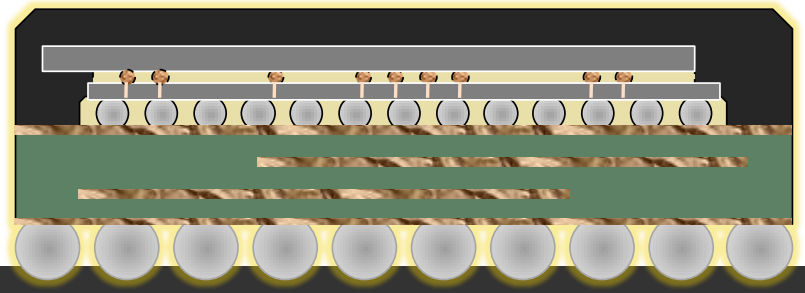
Design Environment for Interposers

Status	Arena	Item
Have	Design	✓ 2D Layout tools ✓ 2D Extraction Tools
Need to Have	Extraction	Integrated 3D Extraction inc. TSV , routing and FRDL/BRDL
	Signal Integrity	Integrated SI tools inc floating substrate and 3D features
	Power Integrity	Integrated PI analyses tools & flow
	DFT / Test	Integrated Double Sided Passive Floating Substrate
	PathFinding	Architectural Trade Off Analyses for Value Proposition



Design Environment for Logic on Logic

Status	Arena	Item
Have	Design	✓ 2D Flow for One Single Sided Die & Technology at a time
	PathFinding	✓ 3D Physical PathFinding Flow for finding Value Propostion
Must Have	Floorplan	3D with optimization across multiple tiers (technologies)
	Utility Insertion	3D tools for global utilities – eg NoC, Clock, DFT….
	Extraction	3D Extraction inc. TSV , routing and FRDL/BRDL
	Timing	across multiple tiers, technologies, libraries….
	Power Integrity	Integrated PI analyses tools & flow
	Signal Integrity	in flow SI analyses tools inc 3D features
	DFT / Test	Optimized DFT overhead for pre-stack test
	Verification	3D Physical Verification, LVS, etc across multiple tiers
	etc..	dependent on the actual stack partition



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