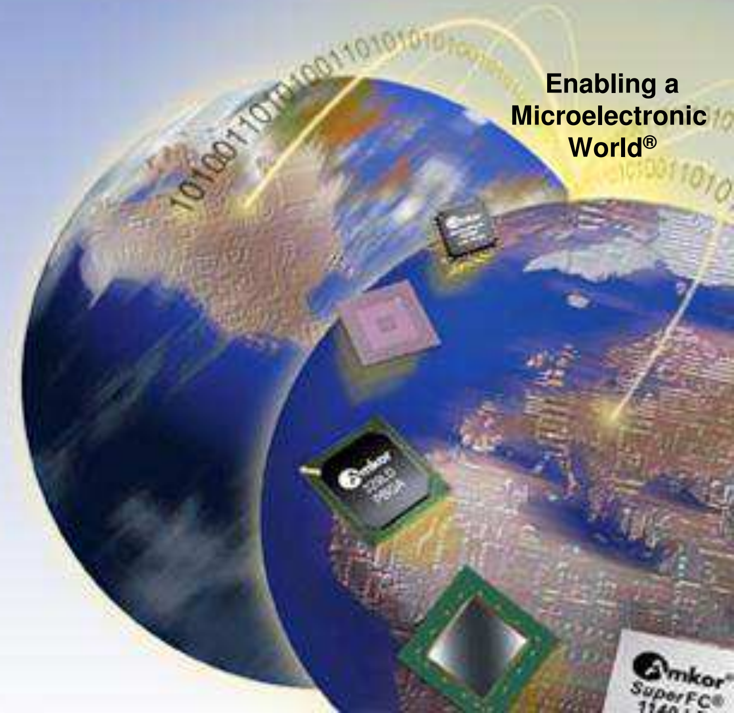
Hot Chips: Stacking Tutorial

Choon Lee
Technology HQ, Amkor

Reliability & Trust

信義



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Mobile Phone Technology Change

theguardian

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Smartphones take lead in European mobile phone market

Simple 'feature phones' now make up less than 50% of sales as quarterly smartphone shipments exceed those of more basic devices for the first time

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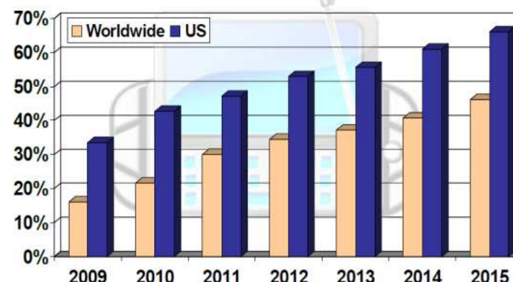
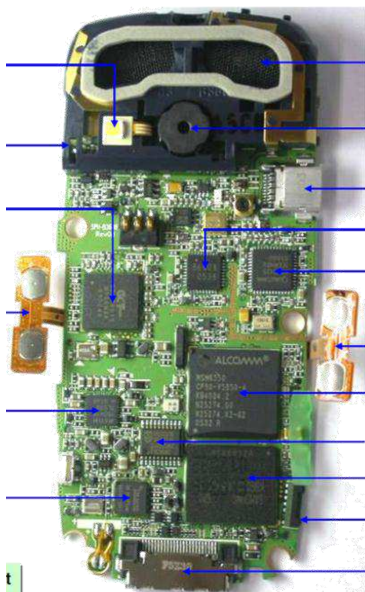
Source : The Guardian, 2011

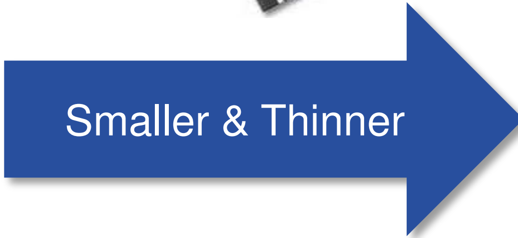
Smartphones as a Percentage of All Phones



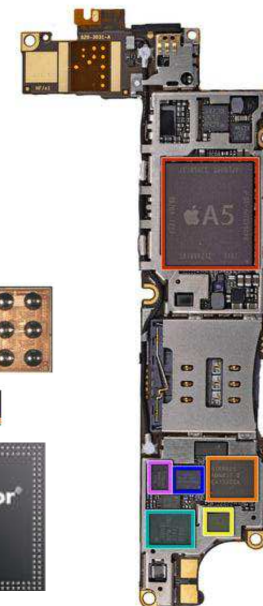
Source : in-stat, 2011



FBGA
QFN
SSOP



FBGA
QFN
WLCSP
PoP
MEMS



Samsung SPH-B3650

Apple iPhone4S

Source : www.ifixit.com

PC Technology Change

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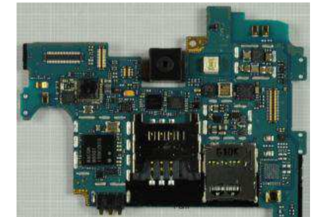


QFP

PBGA

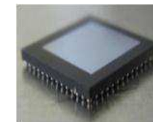
SOIC

QFP

PBGA

CABGA

FCBGA



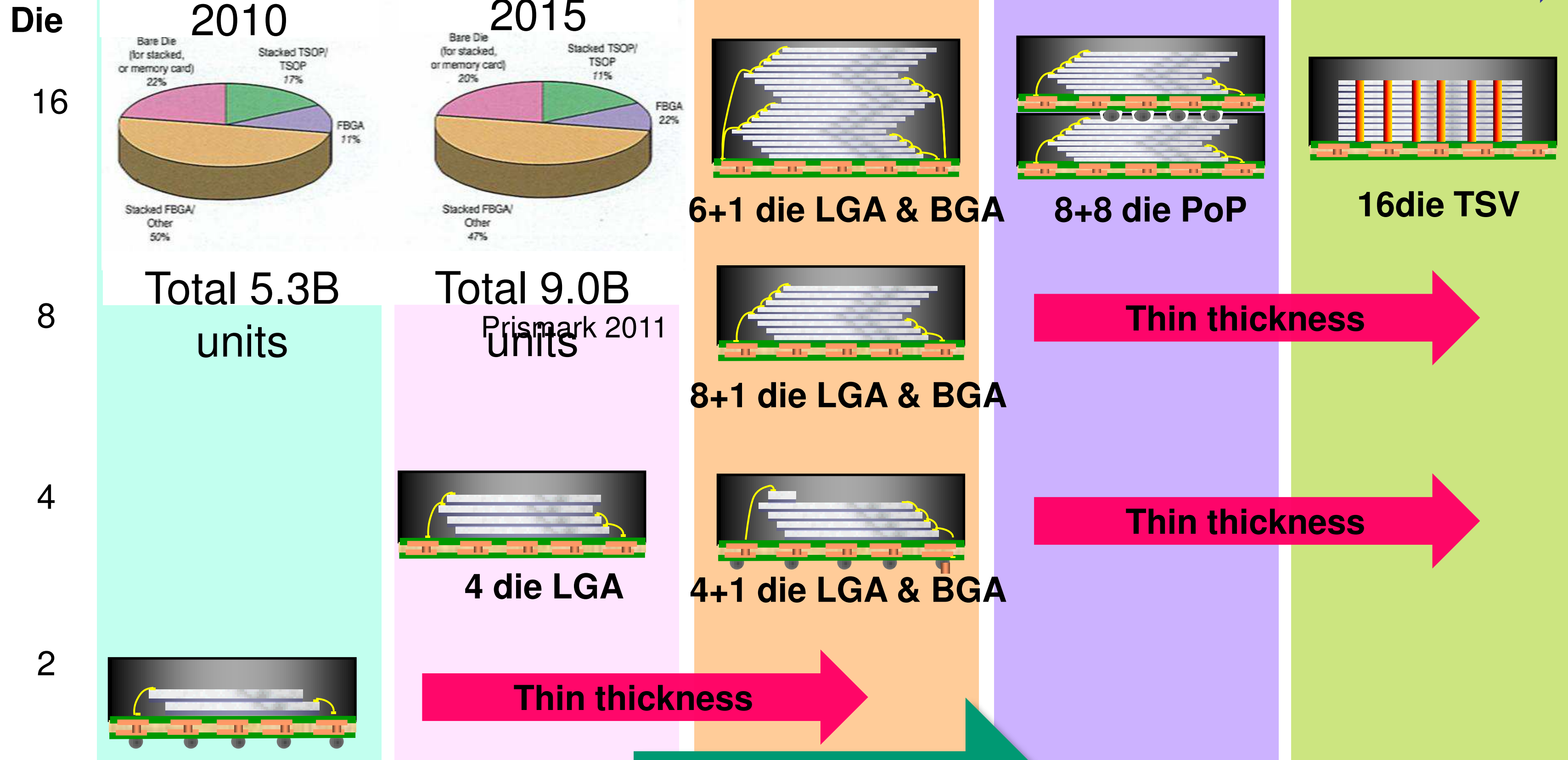
WLFO

MLF

WLCSP

POP

Memory Technology Change



AP+Memory Stack Technology Movement

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Storage Option

TSV Wide I/O

High Density Pin

Memory controller

Baseband

Memory controller

AP

Storage Option

Flip Chip Wide I/O

High Density Pin

Memory controller

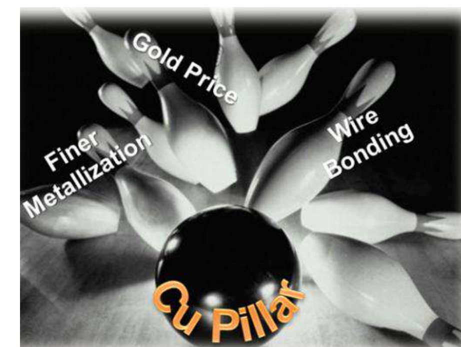
Baseband

Memory controller

AP

External LPDRAM

LPDDR, 2, 3



PoP

TMV

Hybrid TSV + Flip Chip

TSV-Wide IO

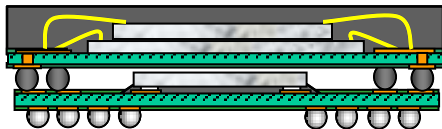
3D Packaging Paradigm Shift

Package Stacking

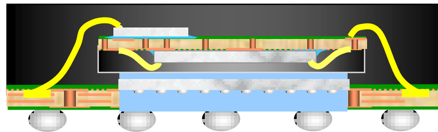
3D Stacking

3D IC

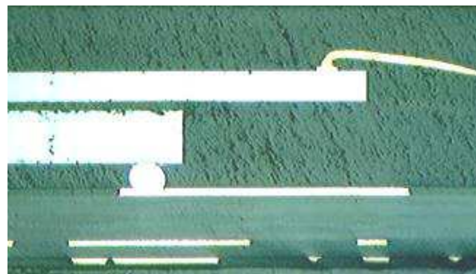
Package-on-Package



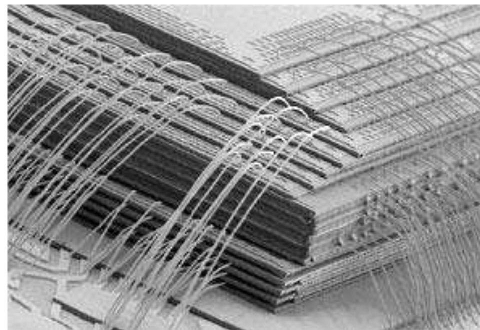
Package-in-Package



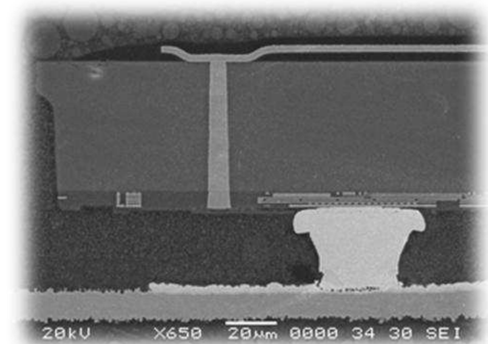
Flip chip + Wire bonding

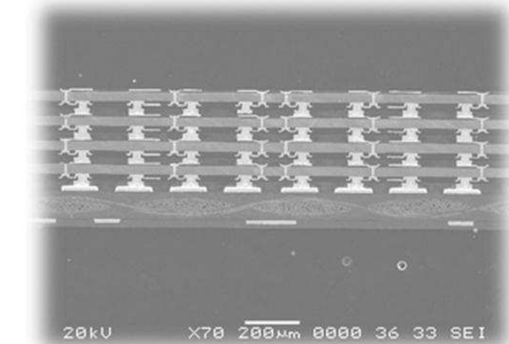


Wire bonding
+ Wire bonding



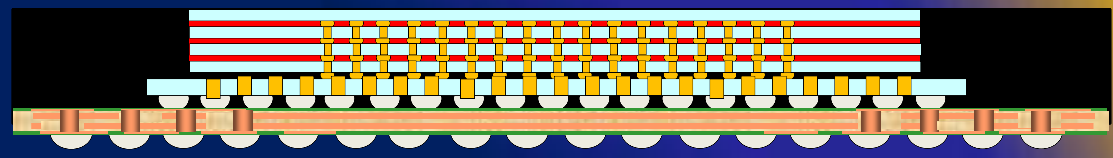
TSV

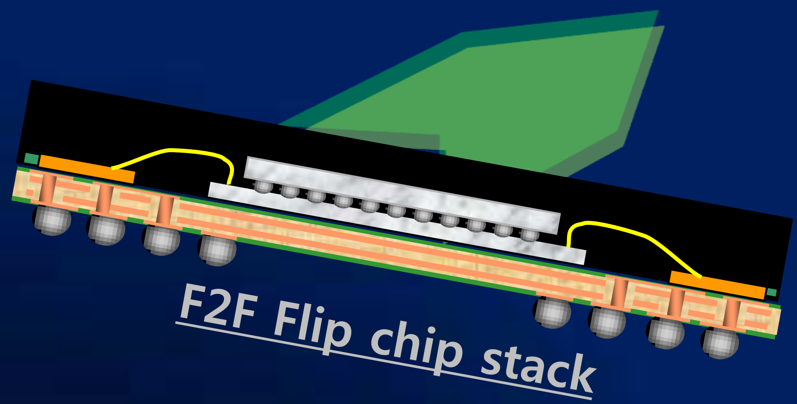




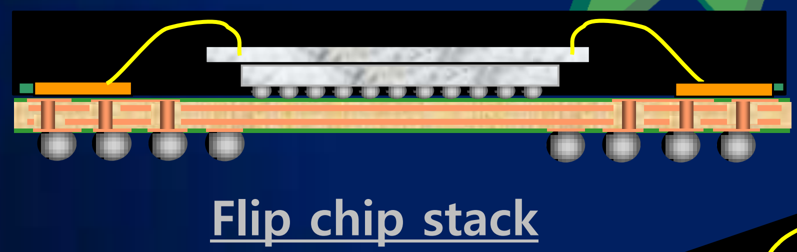
Flip Chip / Wire bonding stack

...Evolves into 3D TSV

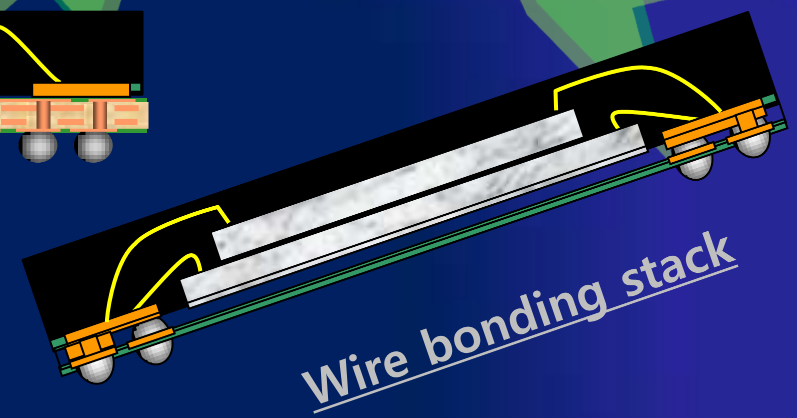




F2F Flip chip stack



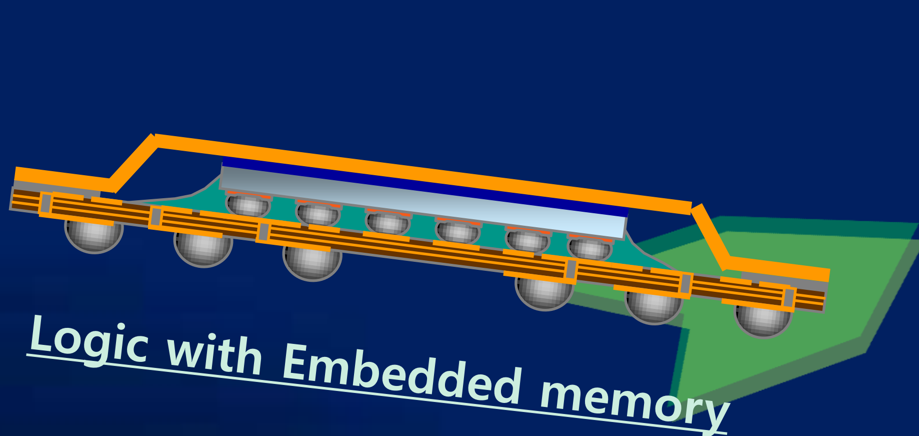
Flip chip stack

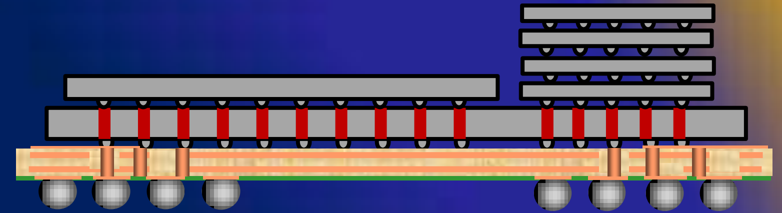


Wire bonding stack

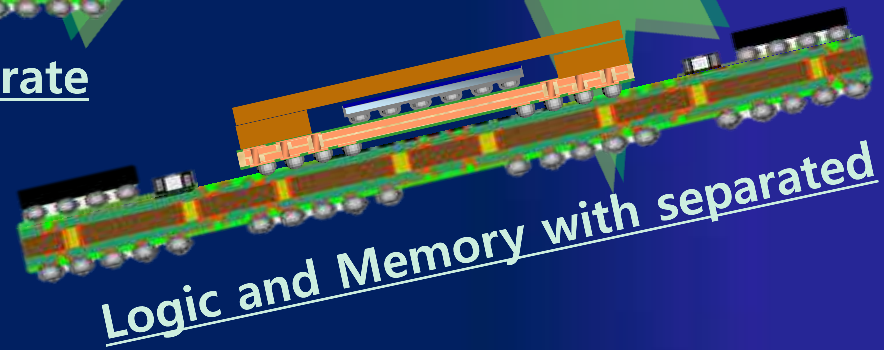
High End fcBGA

...Evolves into 2.5D TSV





Logic and Memory in same Substrate



3D TSV Key Process

Front Micro Bump Pad (Ni/Au)

Temporary bond

Carrier

Wafer thinning Flat reveal

Silicon Recess

Bumping

Secondary reveal

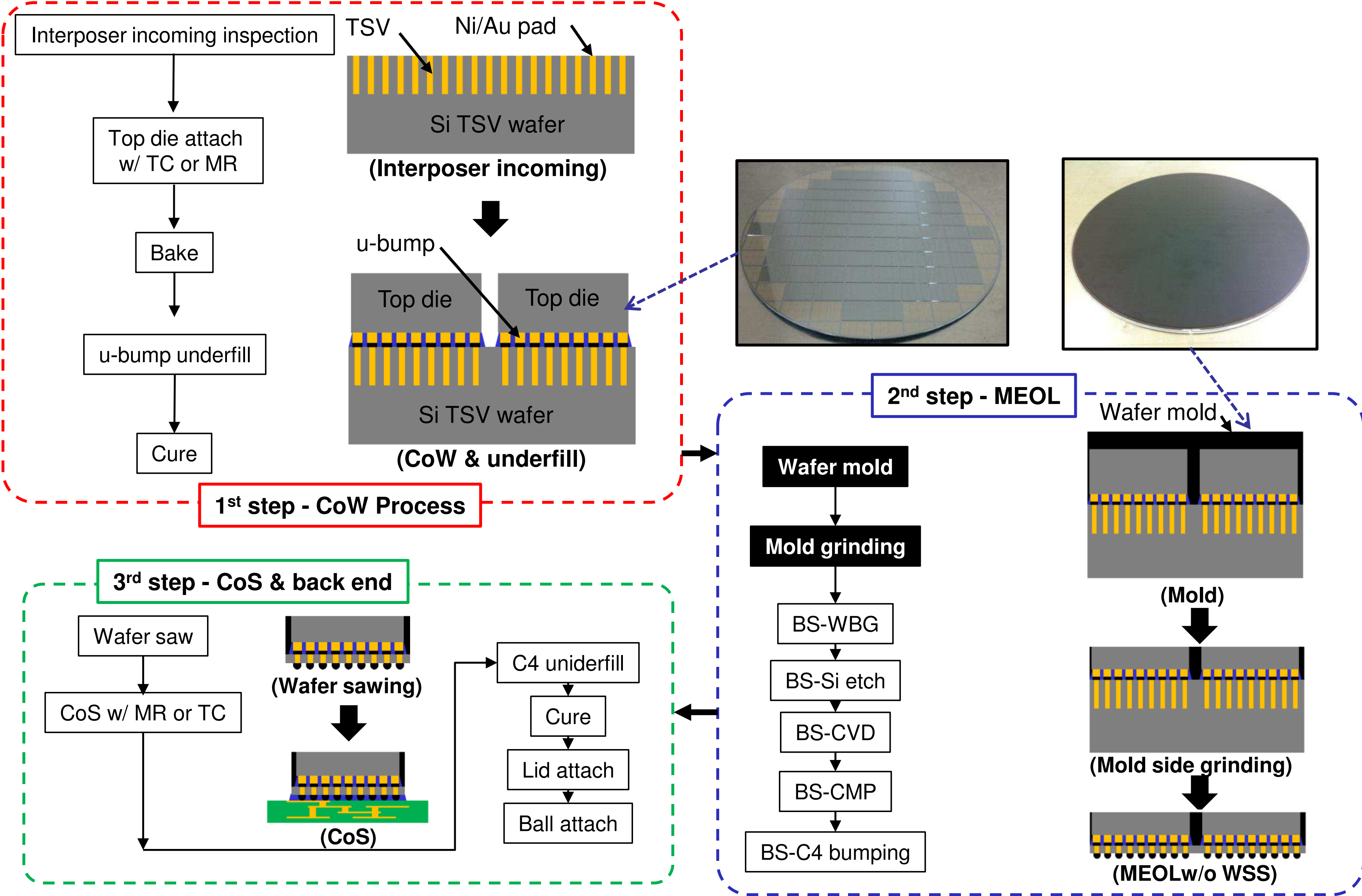
Backside passivation

Organic Version

Inorganic Version

Substrate

Chip on Interposer First Process



Chip on Interposer First Process

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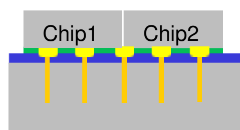
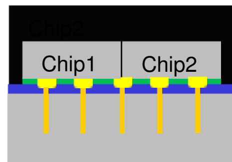
1 Front Micro Bump Pad (Ni/Au)

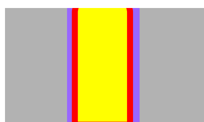
2 Chip Attach & CUF



3 Wafer Mold

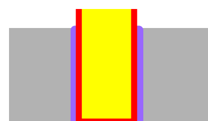


4 Wafer thinning Flat reveal



Cu reveal By WBG+CMP

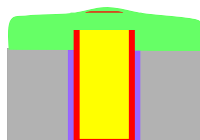
5 Silicon Recess



Dry etch : CF4

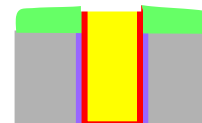
Organic Version

6-1 Backside passivation



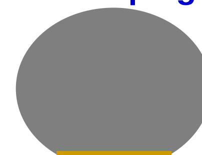
Pass. coat

7-1 Secondary reveal



Pass. exposure, Develop and cure

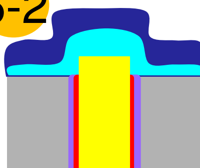
8 C4 Bumping



UBM +C4 plating

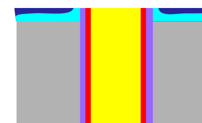
Inorganic Version

6-2

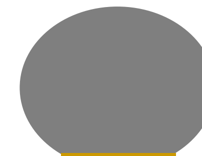


Inorganic passivation PECVD SiN + SiO2

7-2

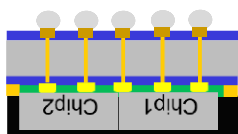


SiO2 CMP

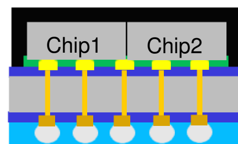


UBM +C4 plating

9 Mold thinning



10 Dicing



Chip Attach to Substrate

Chip on Interposer First Process – High Level Risk

① **Front Micro Bump Pad**
- Ni/Au Pad : Shape, Thickness, IMC embrittlement

② **Chip Attach & CUF : Chip Attach alignment, Flux cleaning, Underfill dispensing**

③ **Wafer Mold : Warpage, Void**

④ **Flat Reveal Wafer Thinning + CMP**
- Wafer Cracking, Cu smearing, Cleaning

⑤ **Silicon Recess – Dry Etch (CF4)**
- Cu corrosion, Etch rate variance, Slow Etch, Contaminate

⑥ **Passivation – organic pass. coating, PECVD**
- Wafer Cracking, Edge Arcing, Thickness/Stress control

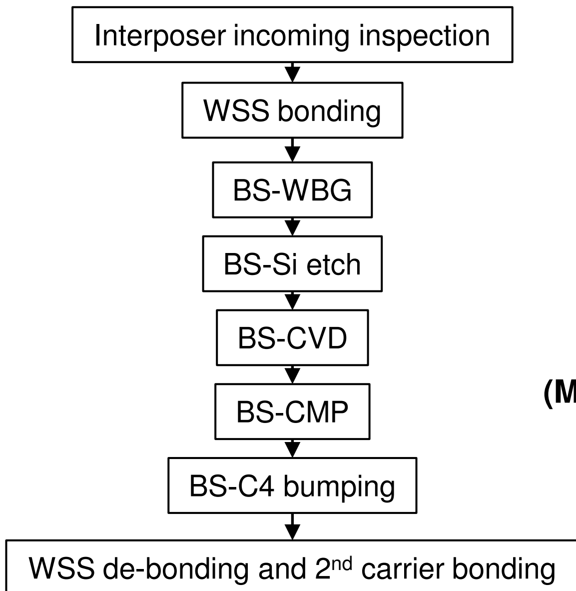
⑦ **Secondary Reveal –CMP : Wafer Cracking**

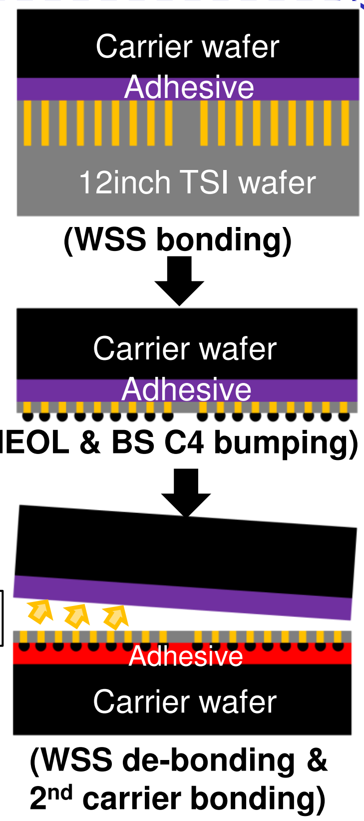
⑧ **C4 Bumping**

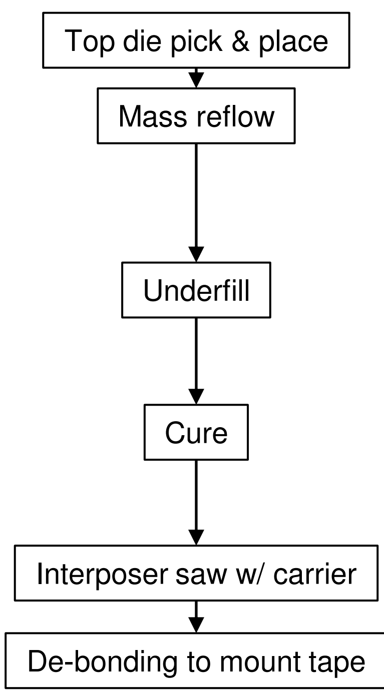
⑨ **Mold Thinning (optional)**

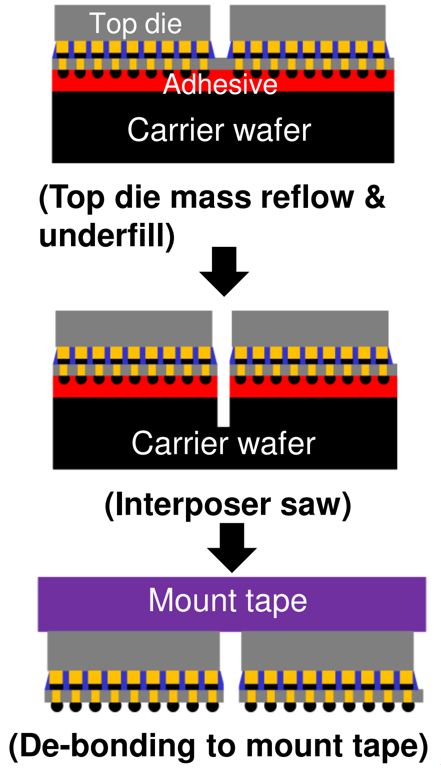
⑩ **Dicing – Saw street cracking**

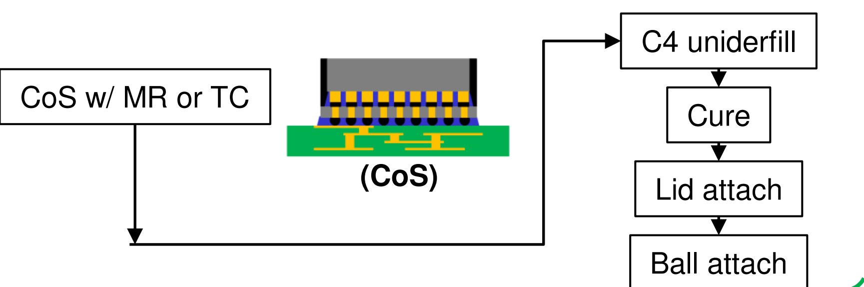
Chip on Interposer Last Process



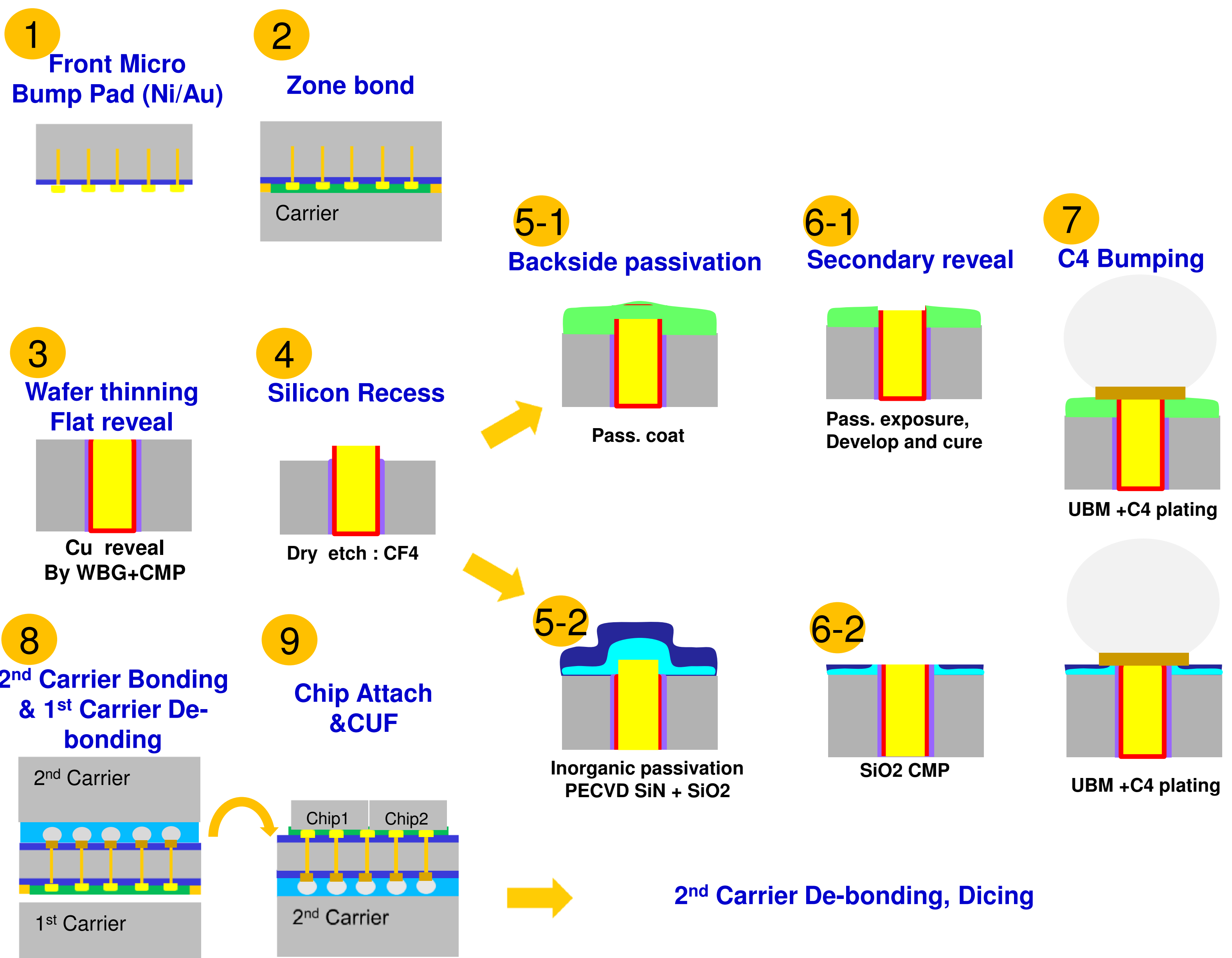








Chip on Interposer Last Process



Chip on Interposer Last Process – High Level Risk

① **Front Micro Bump Pad**
  – Ni/Au Pad : Shape, Thickness, IMC embrittlement

② **Zone Bond : TTV Control**

③ **Flat Reveal Wafer Thinning + CMP**
  – Wafer Cracking, Cu smearing, Cleaning

④ **Silicon Recess – Dry Etch (CF4)**
  – Cu corrosion, Etch rate variance, Slow Etch, Contaminate

⑤ **Passivation – Organic pass. coating, PECVD**
  – Wafer Cracking, Edge Arcing, Thickness/Stress control

⑥ **Secondary Reveal**
  – Wafer Cracking

⑦ **C4 Bumping**

⑧ **2nd Carrier Bonding & 1st Carrier De-bondding**

⑨ **Chip Attach on Interposer**

⑩ **2nd Carrier de-bonding**

FS NiAu – CoC Evaluation

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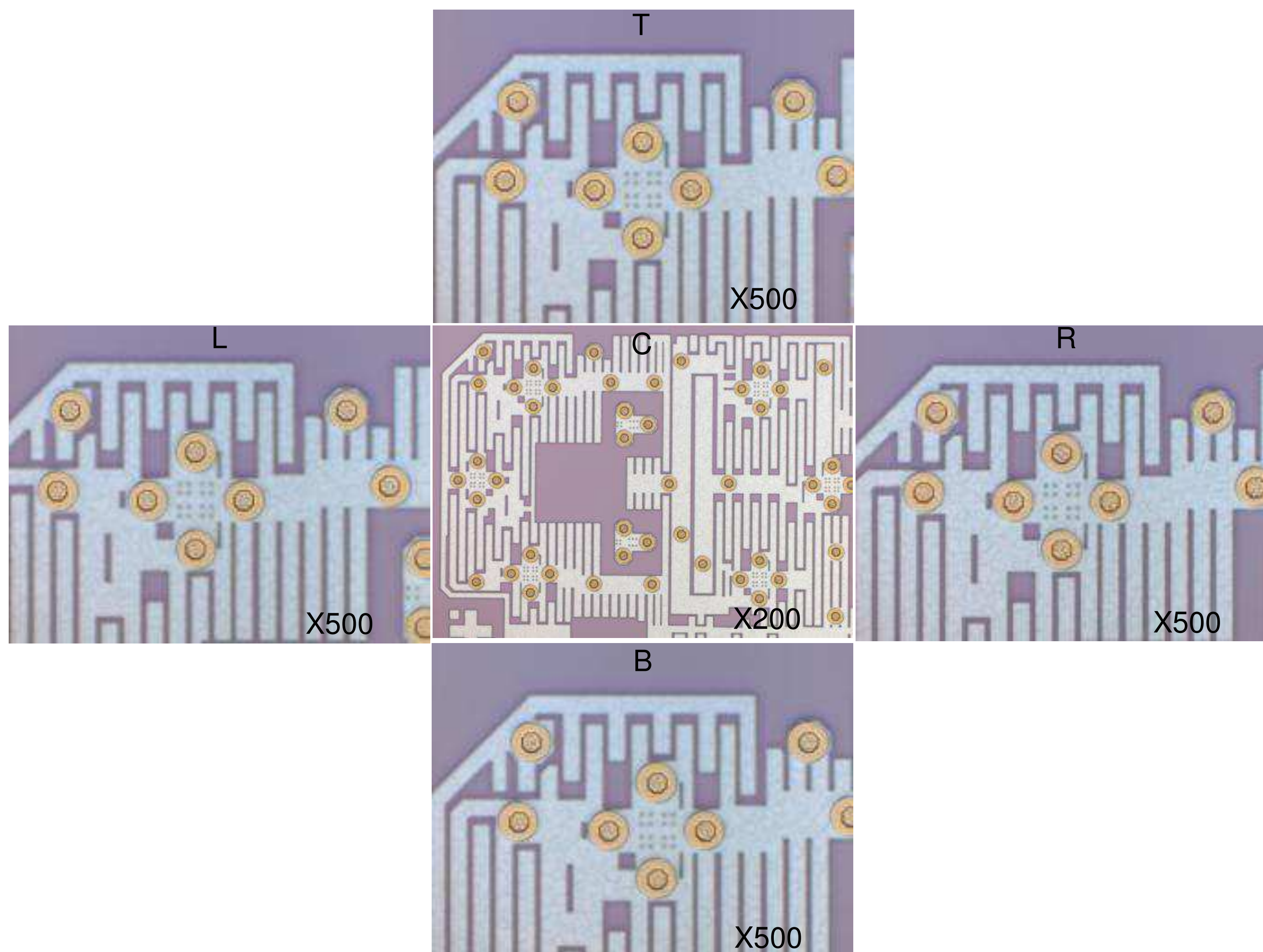
- **CoC Evaluation on E-lytic Ni/Au**
  - AOI inspection
  - Ni/Au thickness measurements
  - Auger analysis for surface condition
  - Wafer bonding
  - Simulated backside thermal processes
  - Debond
  - AOI Pad inspection for FM
  - Singulate
  - Mass Reflow
  - TC Bond
  - "FA - X-section, EDX line scan, EDX area mapping"
  - TC CoC
  - FA

FS NiAu Plating Evaluation

- **Images - Post UBM Etch Process**
  - There are no abnormalities

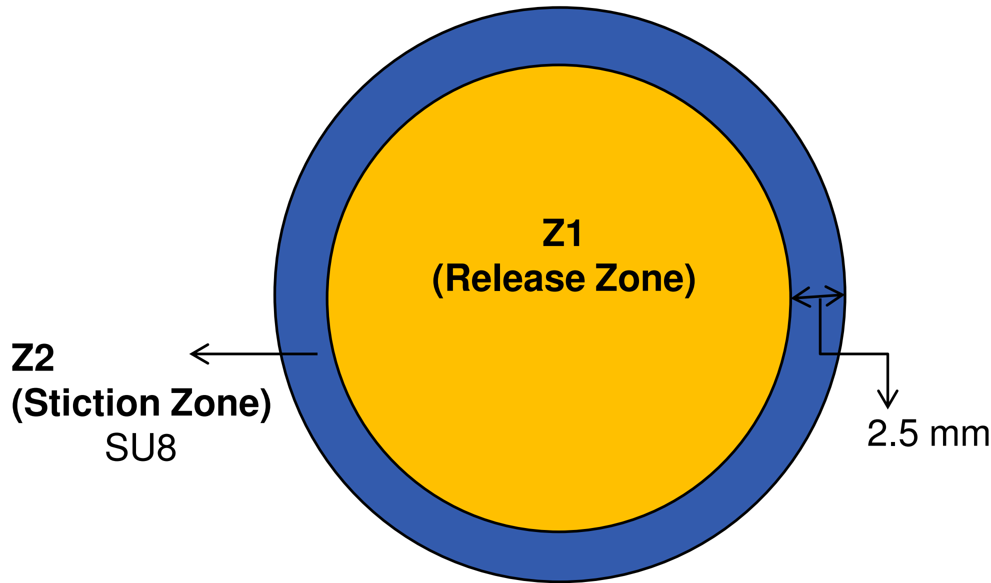


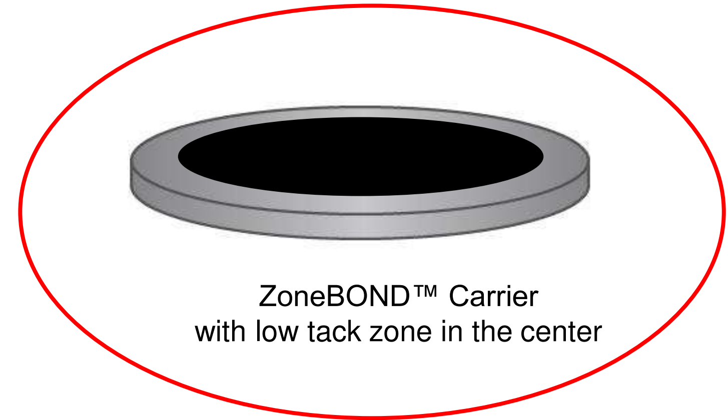
Edge trim & WSS

- **Process validation**
  - For edge trimming to reduce chipping.
  - Optimization of wafer bonding to minimize thickness variance of temporary bonding adhesive.
  - Minimizing wafer crack on debonding process.
  - EAR(Etchng Adhesive Removal) optimization

Overview of ZoneBOND carrier wafer

Amkor Technology®





- **Silane+FC40 (Z1, release zone)**
  - This is anti-sticky zone.
- **Edge zone (Z2, stiction zone)**
  - Edge zone width is approximately 2.5mm.
  - Minimum edge zone width is 1.5 mm.
  - SU8 is used as the edge zone mask.

Zone treated Carrier Preparation (3)

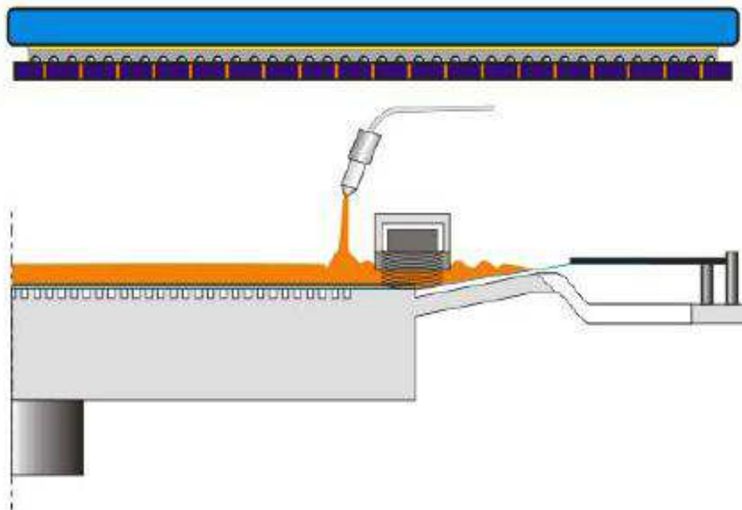
Amkor Technology®

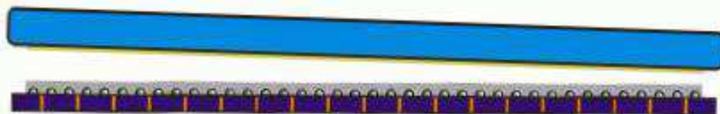
- **Drop test to Acetone**

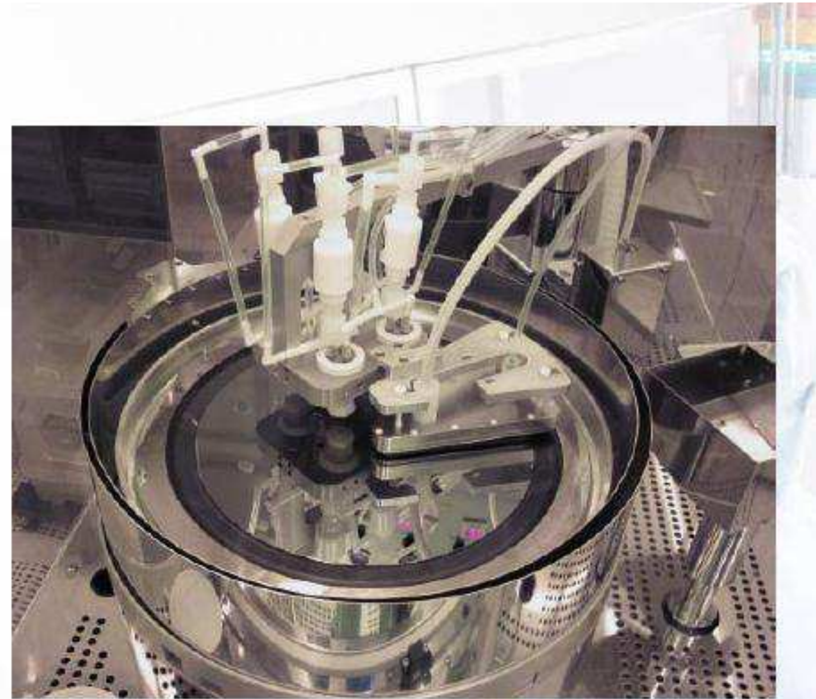
  - We can confirm that Zone treated carrier wafer(Z1) to acetone.
  - Z1 is non stick. The reaction of the material to the wafer is just to make the material chemically bond to the wafer that as a "Silanol condensation reaction". Once it reacts with the surface, the single molecule layer that's permanently attached to the carrier acts as a poly tetrafluoroethylene(PTFE) or " Teflon like" coating on the wafer.

ZoneBOND De-bonding

- **Edge Zone Release with EZR & EZD module**

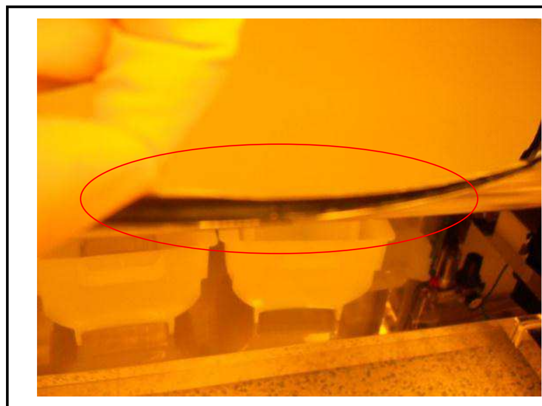






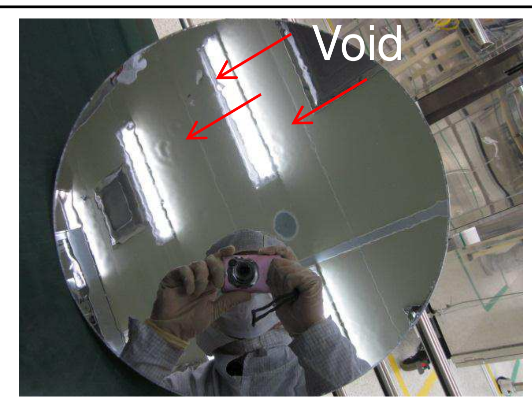
EZR Module: 300mm wafer mounted on film frame

Failures & Problems Related with ZoneBOND De-Bonding

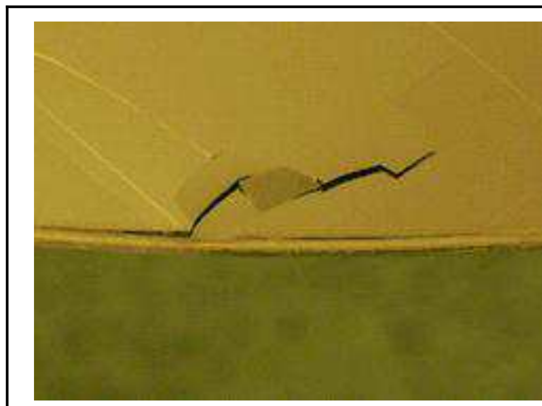


→Delamination

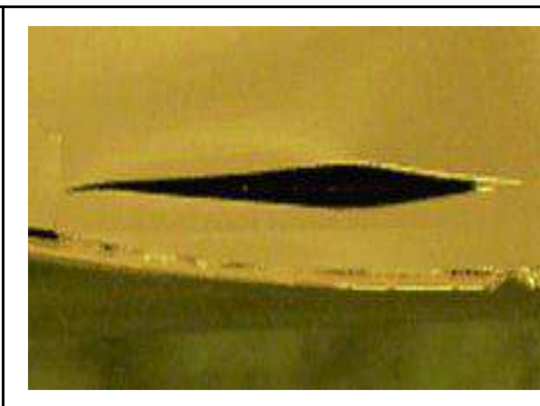
→Adhesive squeeze out



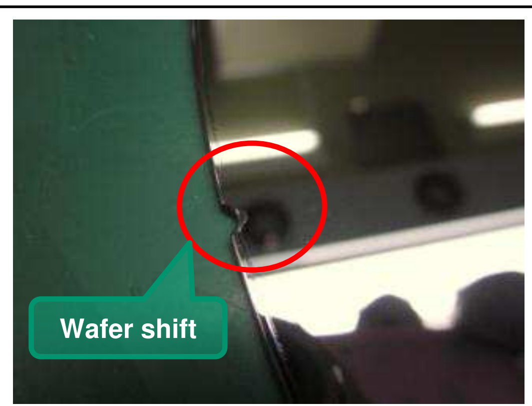
→Blisters



→Crack at edge zone



→Crack



→Wafer shift

World Wide Temporary Bonding Methods

Amkor Technology®

	Thermal	Zone	Laser	Chemical	Wedge
Machine	EVG, TEL, SUSS	EVG, SUSS	TAZMO, Yushin, SUSS	TOK	SUSS
Material	BSI, ShinEtsu, Sumitomo	BSI, ShinEtsu, Sumitomo	3M	TOK	TMAT, Dow
Machine price	Middle	High	Middle	Middle	High
Material price	High	High	Middle	High	Middle
TTV	Good	Normal	Good	Normal	Normal
UPH	Middle	Low	High	Low	High

Advantage & Disadvantage of Various Methods

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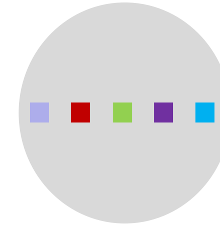
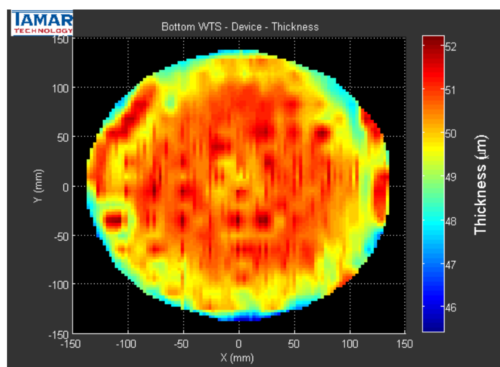
System		Thermal	Zone	Laser	Chemical	Wedge
Bond	Advantage	- Using the Si carrier	- Using the Si carrier	- Using the UV cure - Low out gassing - Double side bond	- 1 layer adhesive coat - Short bonding time - Good to adhesive generality	- Using the Si carrier - Development of an active adhesive
	Dis advantage	- Long Bonding time	- Application of Zone carrier - Bad to adhesive stability - High machine price	- Using the Glass carrier - Bad to adhesive generality	- Using the hole Glass carrier - Coating the top device - High carrier price	- 2 layer coat - Difficult to control adhesion - High machine price
Bump process	Advantage	- Applicable issue to the Si carrier	- Applicable issue to the Si carrier	- High stability (thermal, chemical)	- Advantage of out gassing - High chemical stability	- Applicable issue to the Si carrier
	Dis advantage	- Bad thermal stability - High adhesive contamination	- Bad thermal stability - Change the adhesive - Weak to void	- Glass chucking - Weak to void	- Glass chucking - Bad thermal stability - Process failure by high warp	- Low adhesion - Concern to Si del. - Weak to void - High adhesion contamination
Debond	Advantage	- No mount tape damage	- Room temperature debond - High thermal stability	- Room temperature debond	- High thermal stability	- Room temperature debond -Carrier remove to short time -High thermal stability
	Dis advantage	- Need to high temperature process - Bump damage - Thin wafer handling	- Long remove time to edge adhesion - Worry about new process - High machine price	- Possibility to laser damage - Difficult to rework - Adhesion change at surface	- Long time of adhesion removal - After removing the adhesion, possibility of damage	- Wafer edge damage - High machine price

WBG and Cleaning

- **Process validation**
  - Soft reveal
    - Minimizing TTV with accurate control.
    - Cleaning improvement after wet polish.
  - Flat process
    - Only grinding of Si layer at WBG tool not to expose Cu.
    - Using CMP tool to expose Cu and post CMP cleaning

Wafer Thinning & Cleaning
Example of Flat process





<Device>

Mean : 50.1 um
Max : 52.7 um
Min : 46.8 um
TTV : 5.9 um

Dry Etch

- **Process validation**
  - Soft reveal
    - Acceptable etch rate
    - Optimizing etch rate and uniformity with TSV bonded pairs.
    - Finding via height for ISR process sequence.
  - Flat process
    - Very slow etch rate
    - Optimizing etch rate and uniformity with TSV bonded pairs
    - Etch gas mixing evaluation to improve etch rate without Cu corrosion.

Si recess etching : Dry etch

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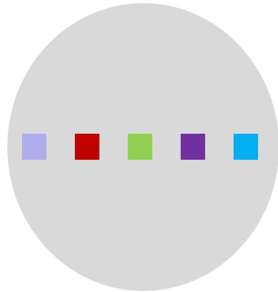

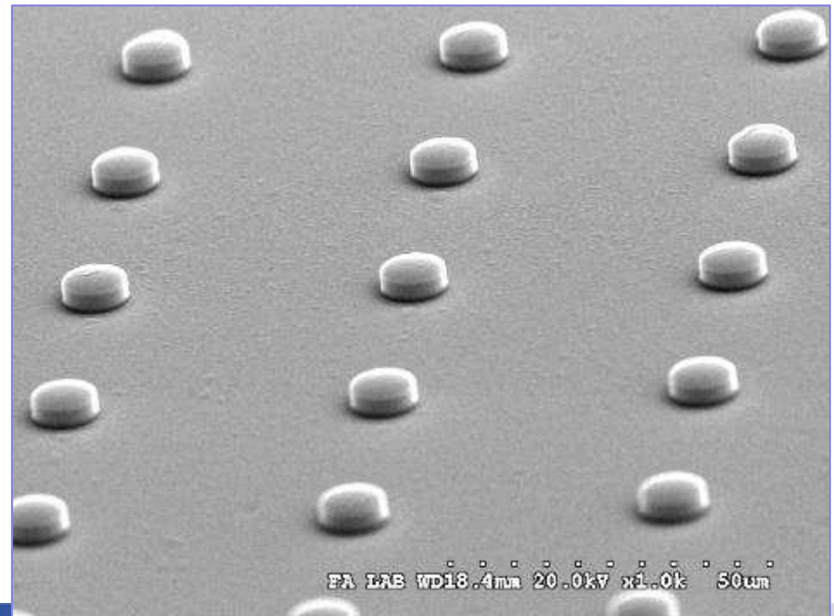

Si recess etching : Dry etch

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➢ **Flat process**

➢ **Soft reveal process**

PECVD

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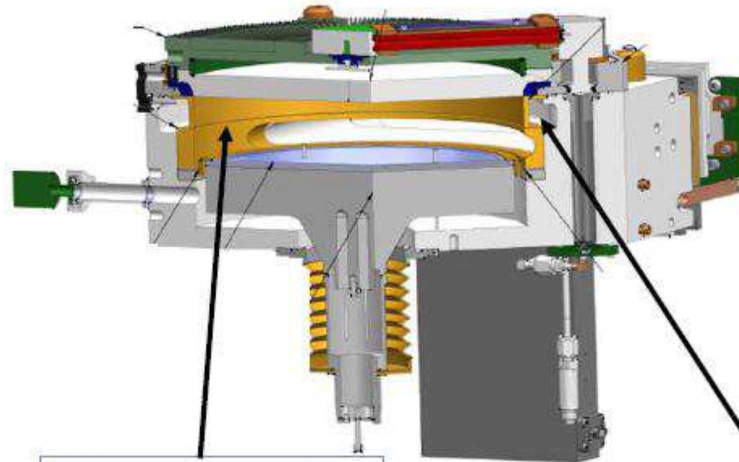
- **Process validation**
  - Deposition of SiN and SiO2
  - Confirming deposition rate, uniformity, stress and RI.
  - Setting up measurement method using elipsometer to check single layer, multi layer.

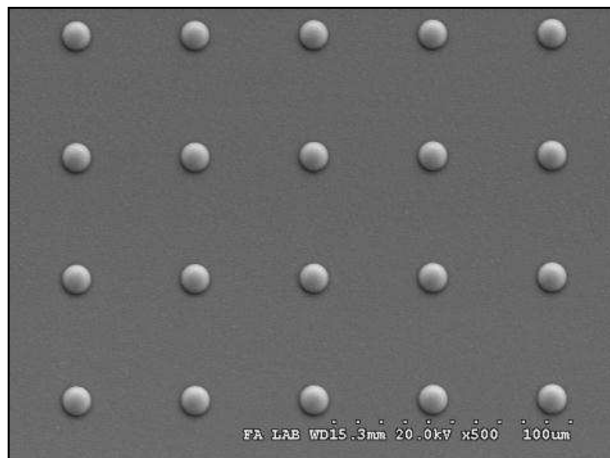
Dielectric deposition : PECVD

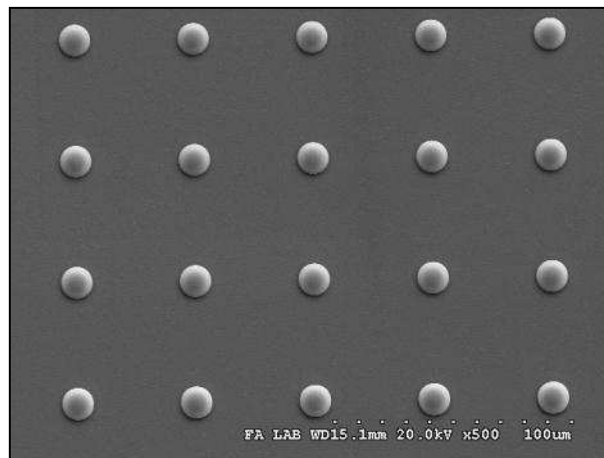


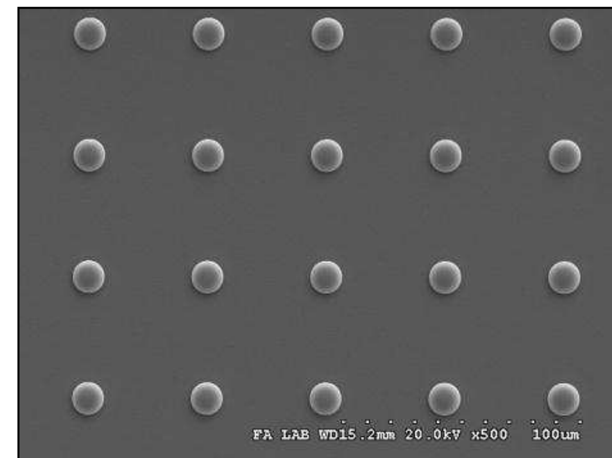
- Pumping gap limits conductance
- Extends 360°
- Radially symmetrical pumping
- Large volume pumping gallery
- Uniformity unaffected by pump

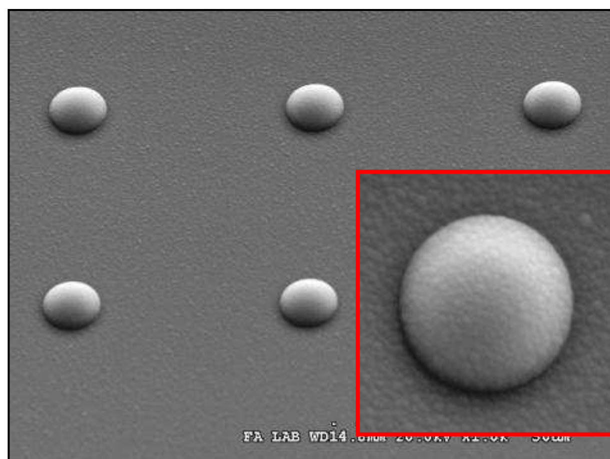
- Silicon Nitride
  - $SiH_4(g) + NH_3(g) + N_2(g) \rightarrow Si_xN_yH_z(s) + H_2(g)$
- Silicon Oxide [Silane-based process]
  - $SiH_4(g) + 4N_2O(g) + N_2(g) \rightarrow SiO_2(s) + 4N_2(g) + H_2(g) + O_2(g)$
- Silicon Oxide [TEOS-based process]
  - $Si(OC_2H_5)_4(g) + O_2(g) \rightarrow SiO_2(s)$ + byproducts

Dielectric deposition : PECVD

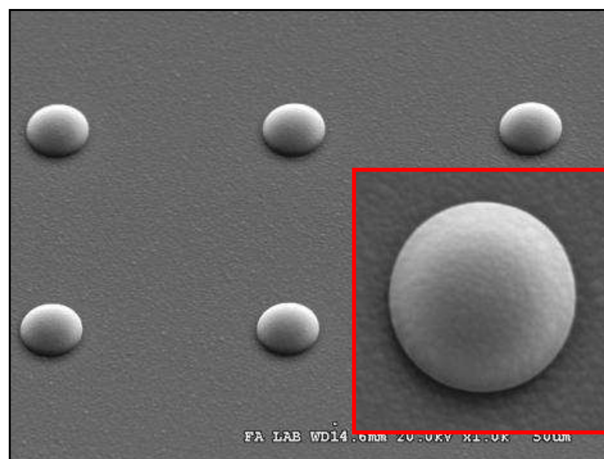




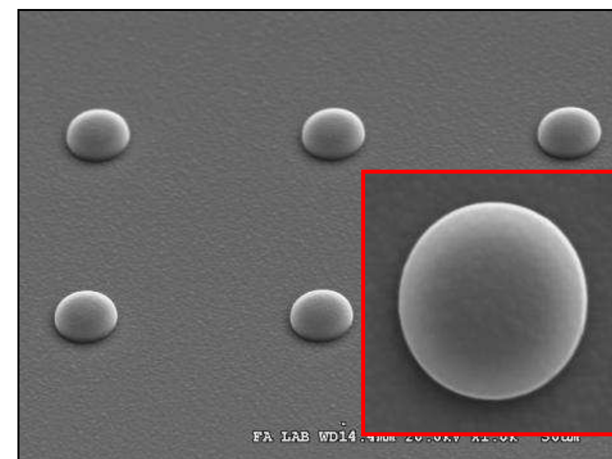




Center



Middle

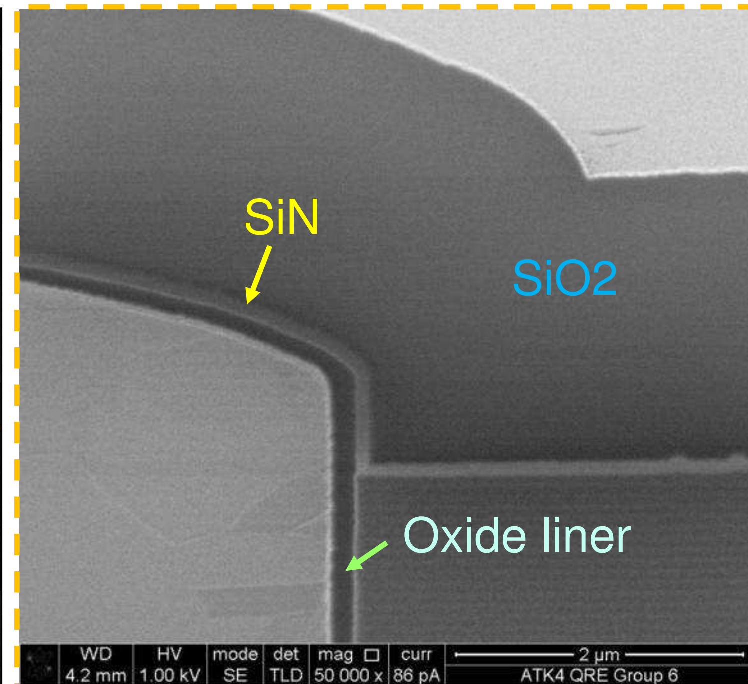


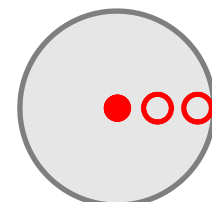
Edge

Note

- Found no abnormality.

Dielectric deposition : PECVD





Note
- Found no damage.

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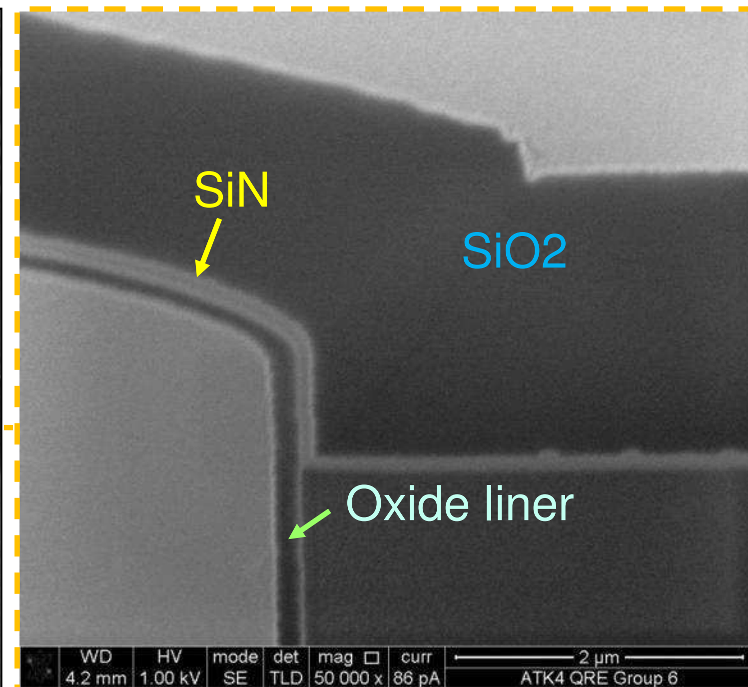
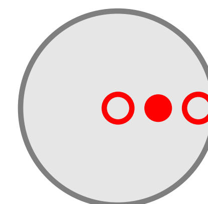
Dielectric deposition : PECVD

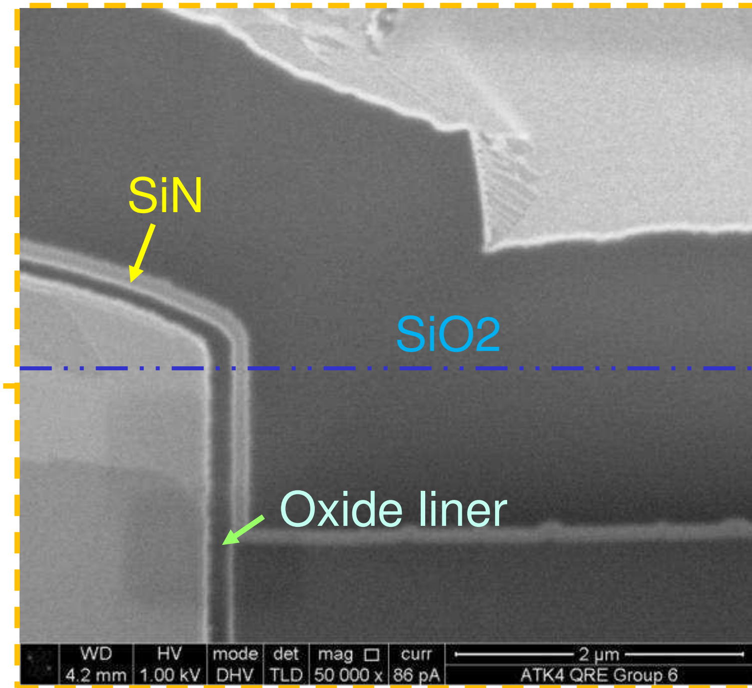


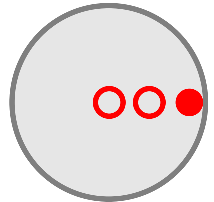


Note

- Found no damage.

Dielectric deposition : PECVD





Note

- Found no damage.

CMP

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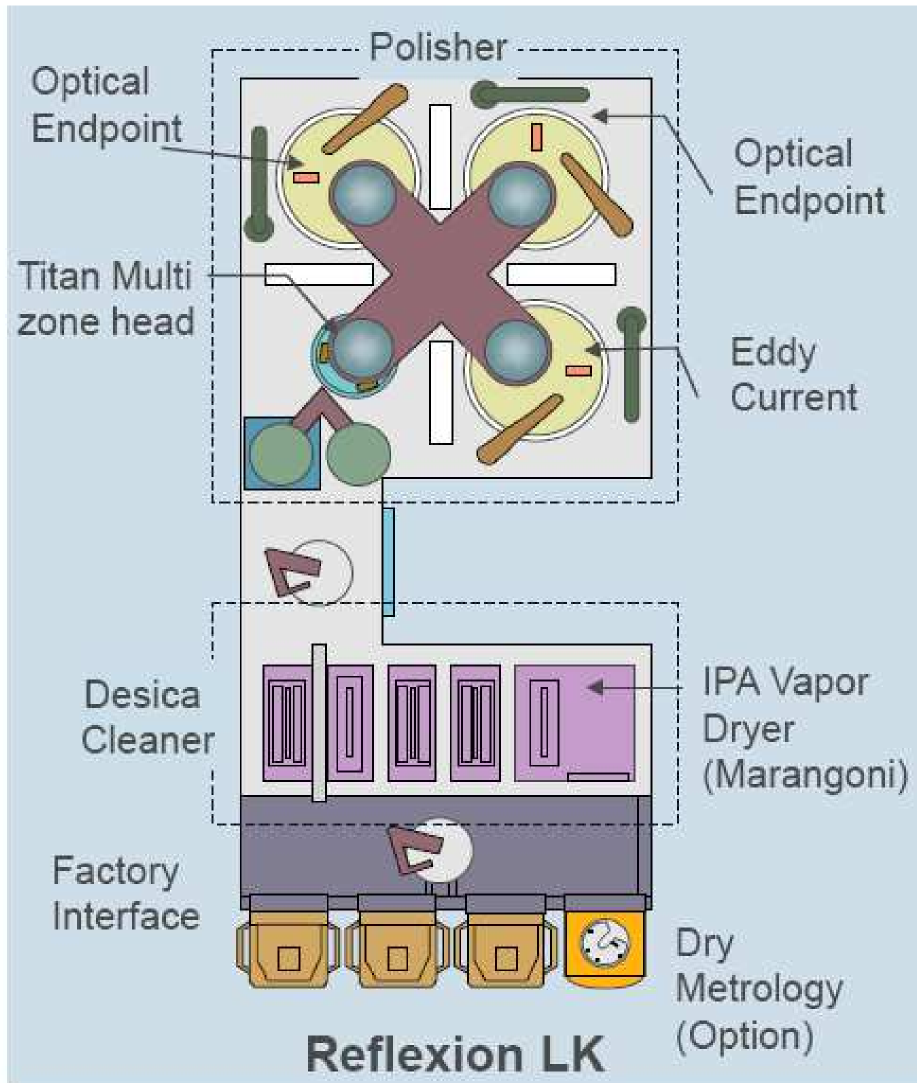
- **Process validation**
  - Process optimization to find BKM
    - Oxide/Cu polish process for ISR (Inorganic soft reveal)
    - Si/Cu polish process for flat reveal process
    - Slurry evaluation
    - Post CMP cleaning evaluation

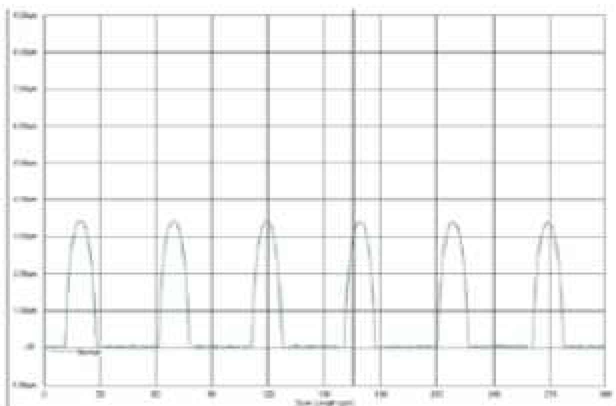
Secondary reveal : CMP



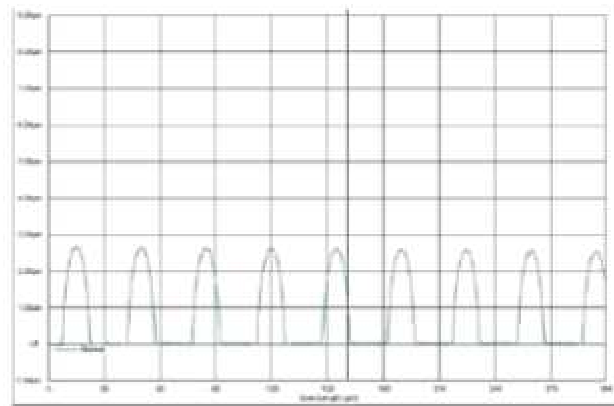
Proven product and industry benchmark CMP tool
>1500 Reflexion/Refelxion LK shipped by 2011

- **Product Features**
  - 3 platen – 4 head polisher
  - Multi zone polishing head
  - In-situ process control optimizes productivity and performance
  - High performance Desica Cleaner
- **Process Controls**
  - Real-Time Profile Control (RTPC™)
    - High-resolution eddy-current endpoint for bulk metal polish step
  - FullScan™ Endpoint
    - Laser endpoint for metal film clearing
  - FullVision™ MX Endpoint
    - Broad-band optical endpoint control for remaining dielectric thickness
  - Si EP/ISPC under development
- **Process BKMs**
  - TSV CMP know-how
  - Low cost/high performance process BKMs for various TSV CMP applications

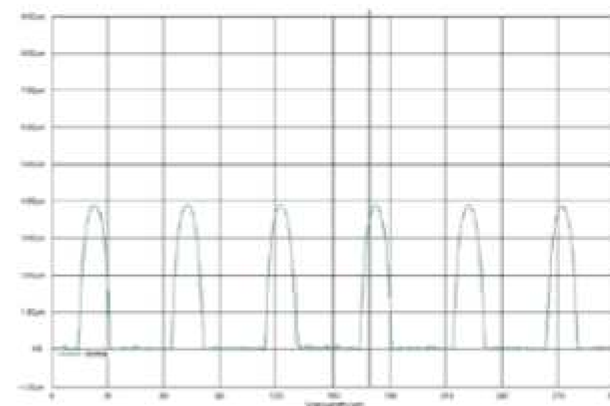
Secondary reveal : CMP



Wafer Center
~3.3um



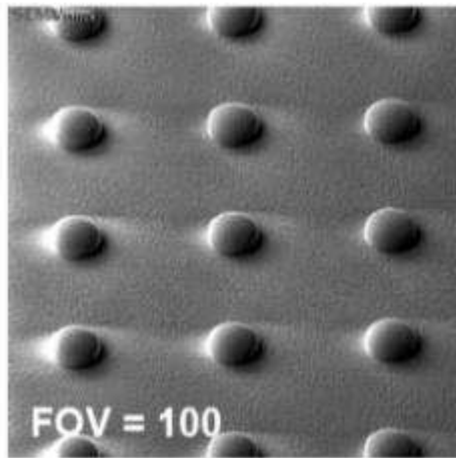
Wafer Middle
~2.6um

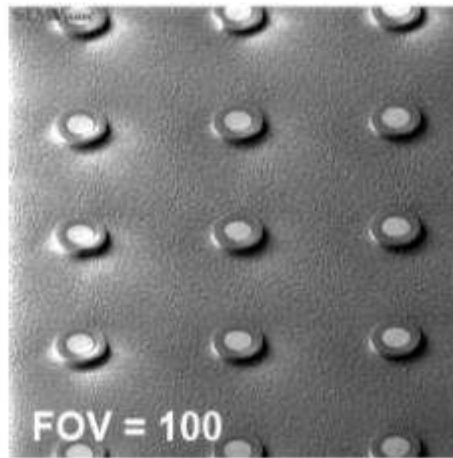


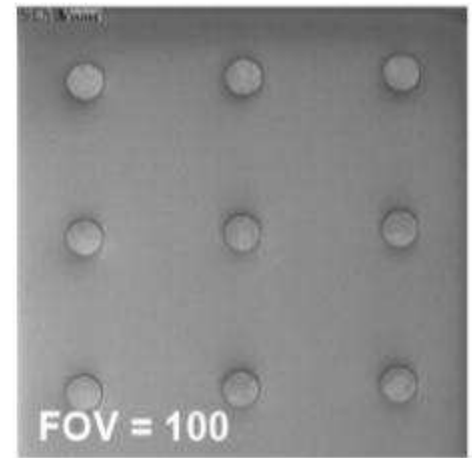
Wafer Edge
~4um

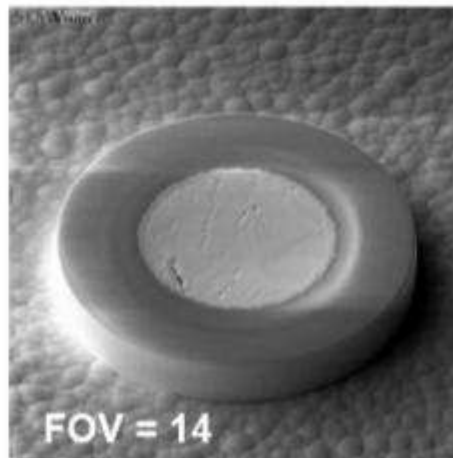
- 1k nitride and 2.8um oxide were deposited on these wafers, pillar height at wafer center and edge post etch are not high enough for CMP to fully exposed copper after pillar planarization and OP with 5k oxide removal on the field.

Secondary reveal : CMP









Pre-CMP (tilted)

Post 30s Polish Time (tilted)

Post 90s Polish Time (top-down)

- **Fast and good pillar planarization achieved**
- **Minimum field oxide loss during pillar planaraization**

Secondary reveal : CMP

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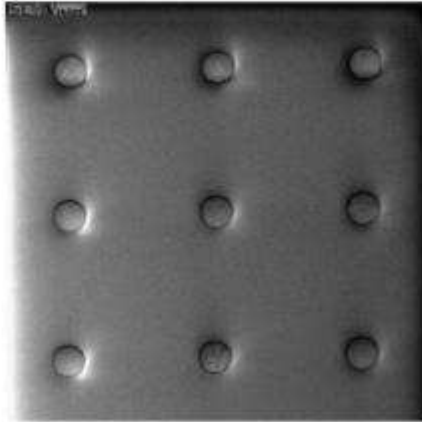
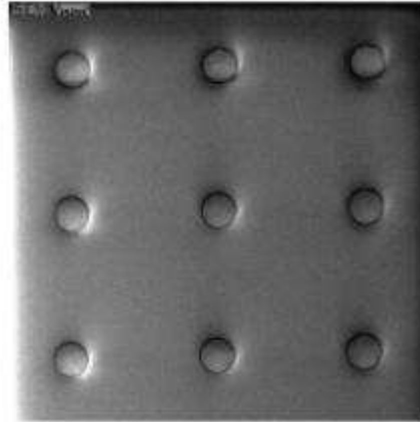
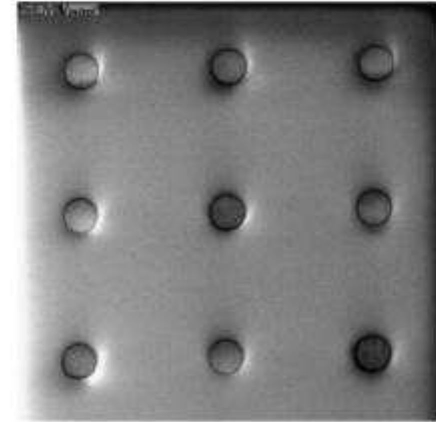
center

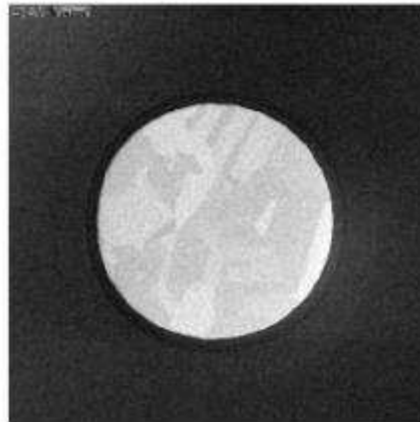
middle

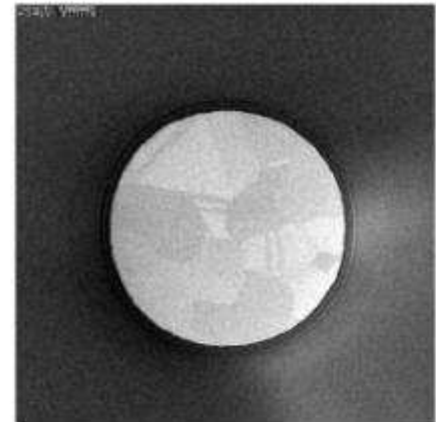
edge











Secondary reveal : CMP

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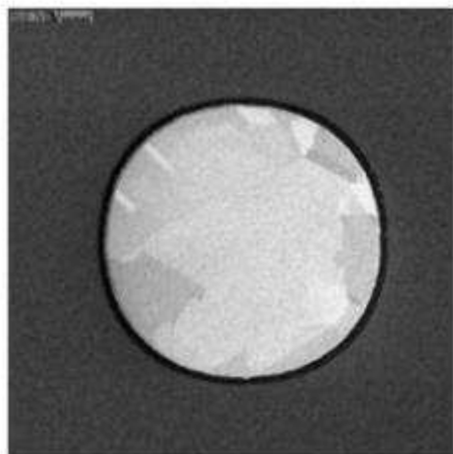
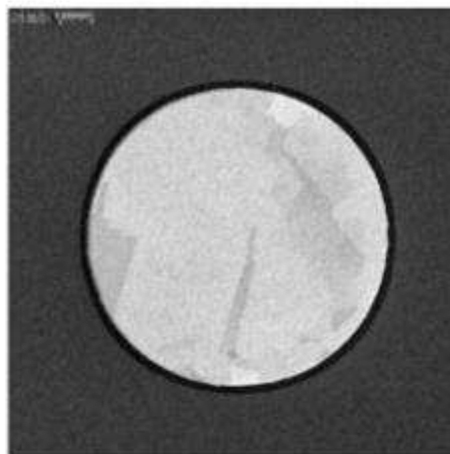
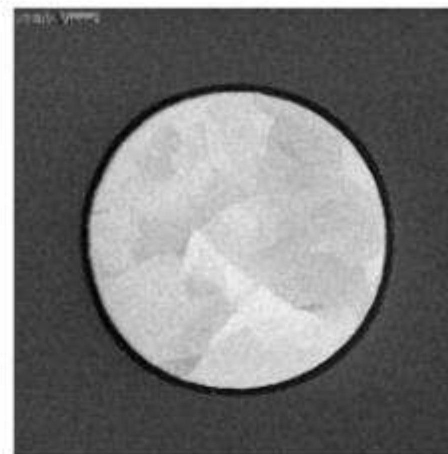
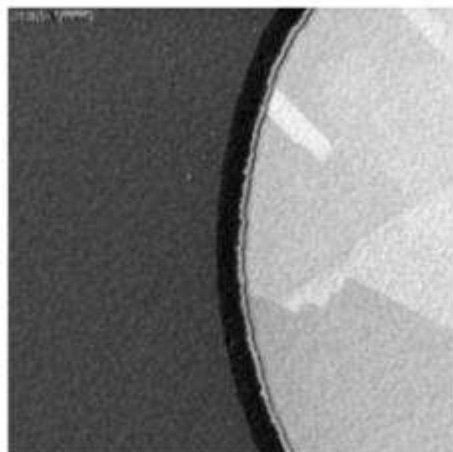
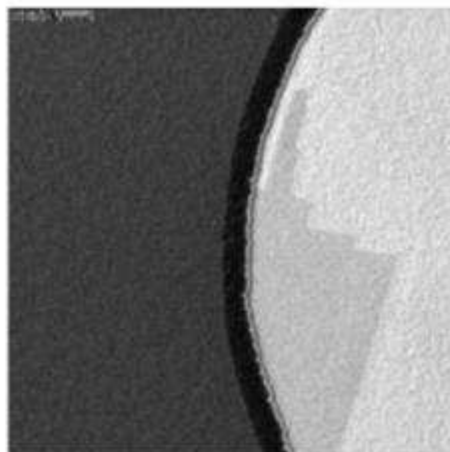
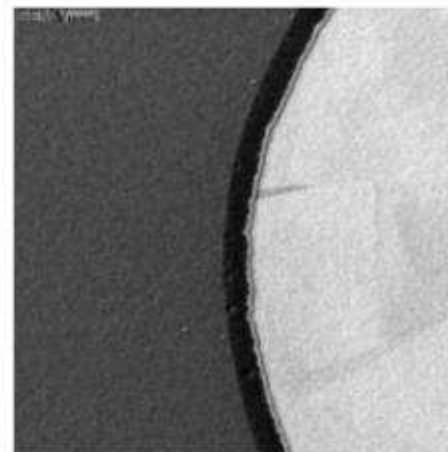
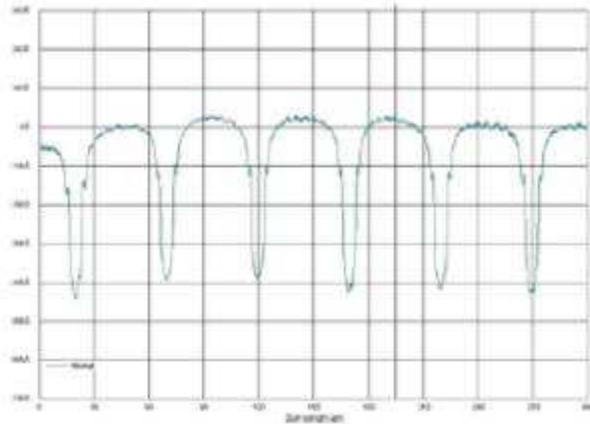
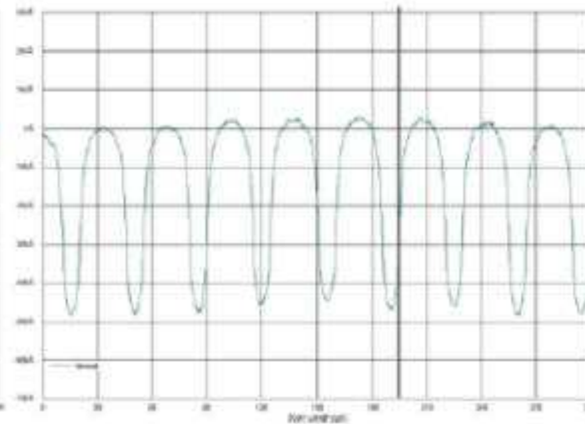







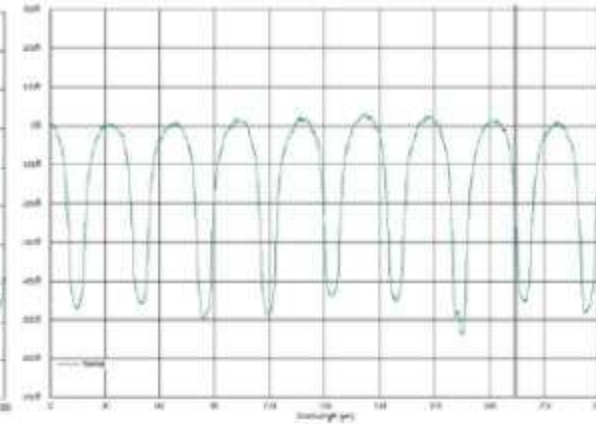
center middle edge

Secondary reveal : CMP
Post CMP Topography

W15

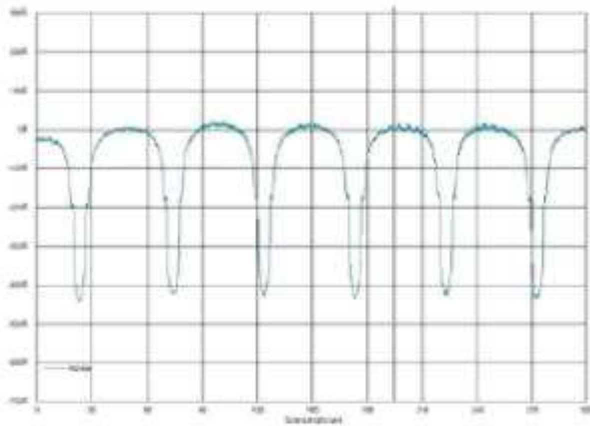


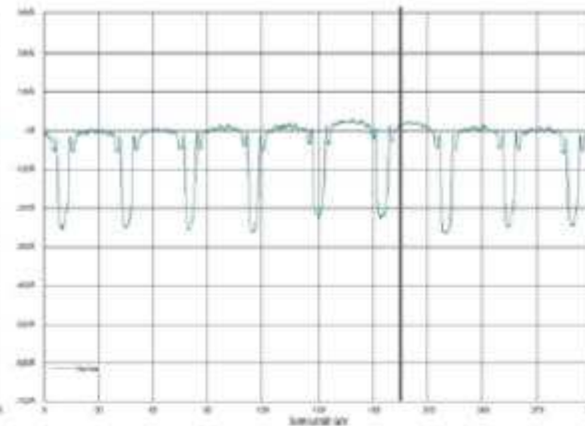


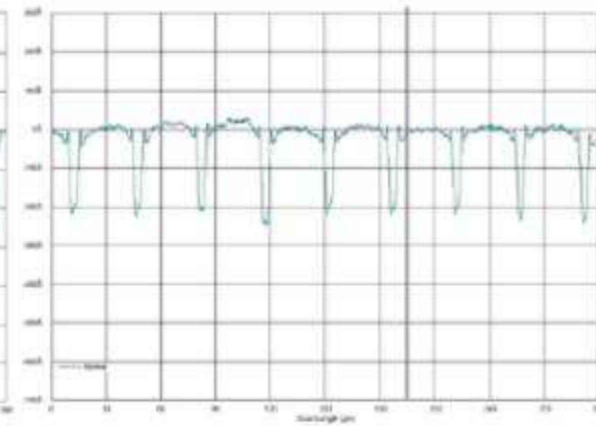


Wafer Center | Wafer Middle | Wafer Edge

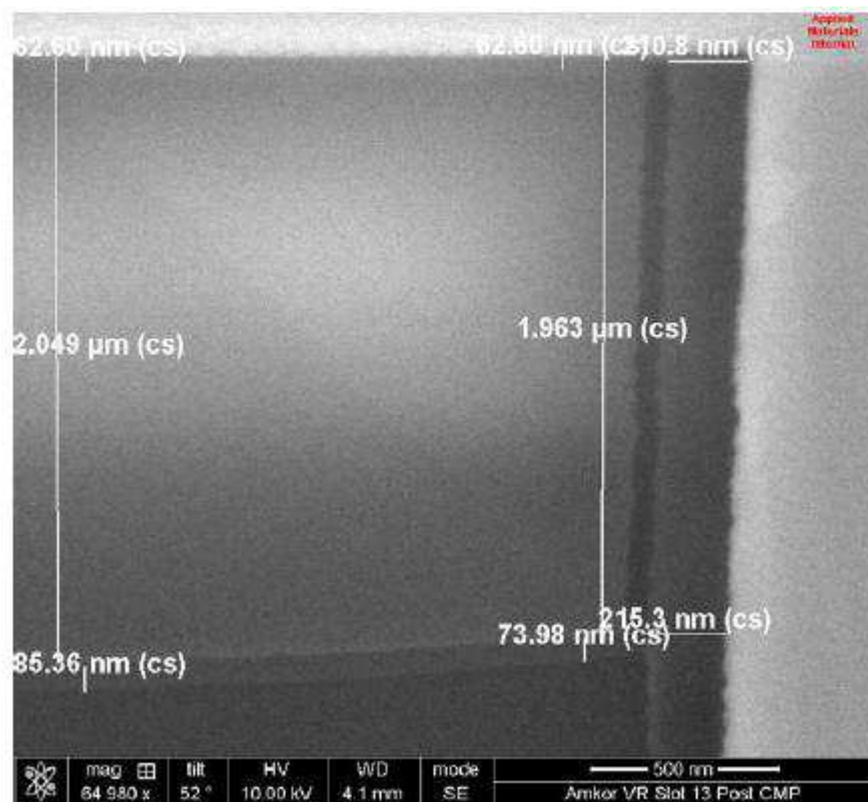
W25



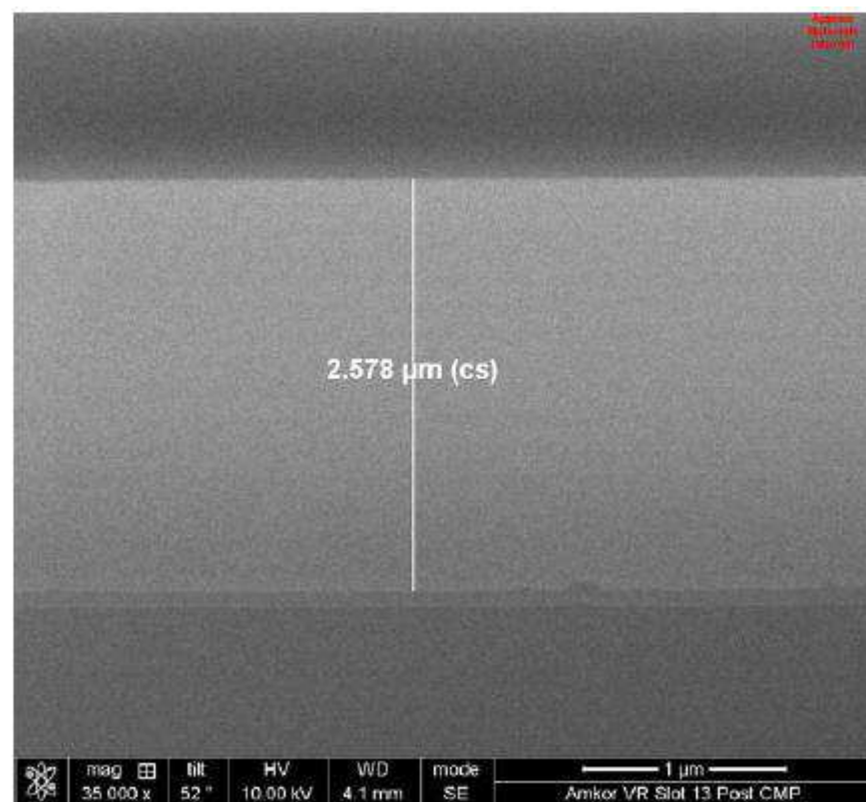




Secondary reveal : CMP
Layer Thickness confirmation after CMP



Patterned Area Next to Via



Open Field Area

Stealth Dicing

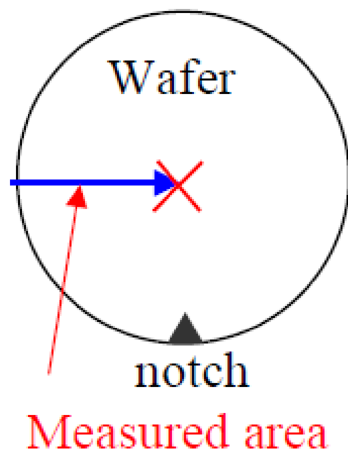
- **Process validation**
  - Performing SD with wafer frame handling.
  - Evaluation of laser transparent tape.
  - Parameter DOE of laser process
  - Study for auto focus through inorganic passivation

Stealth Dicing

Amkor Technology®

● Wafer surface flatness comparison

✓Observed wafer BG tape laminated by manual process



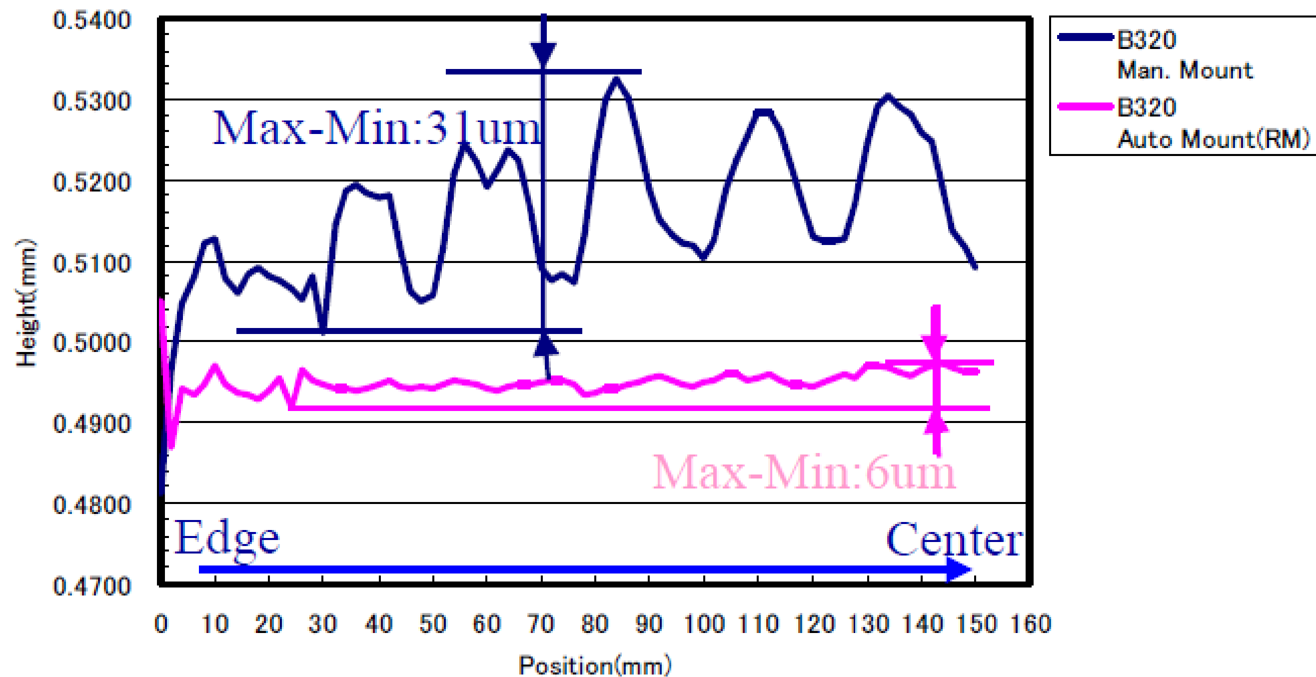


Fig.2 Wafer flatness comparison

Result

Wafer flatness was much improved after optimize tape laminate condition.

With improved condition, can expect stable Auto Focus result

= stable cutting quality.

Stealth Dicing

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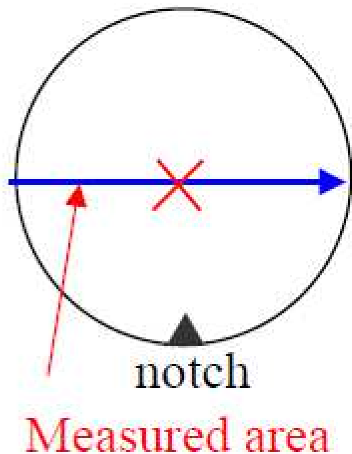
● Investigation for too low SFV on SiN layered wafer

✓Measured SFV on dicer



SFV(V)

2.6
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0

0 50 100 150 200 250 300

X position

Mirror wafer:2.4V

ACCT recommendable Min SFV:1.0V

Estimated functional lower limit:0.5V

Fig.3 SFV check result

Result

SFV was very low at all the point on wafer.

It was around “0.1V” at the lowest case.

*SFV is same as quantity of reflected AF laser from wafer surface.

*Enough high SFV (=enough reflectivity) is required to keep good Z-accuracy

Stealth Dicing

Amkor Technology®

● Influence of SiN layer on wafer surface

✓ Simulation result f reflectivity and suspected root cause of too low SFV

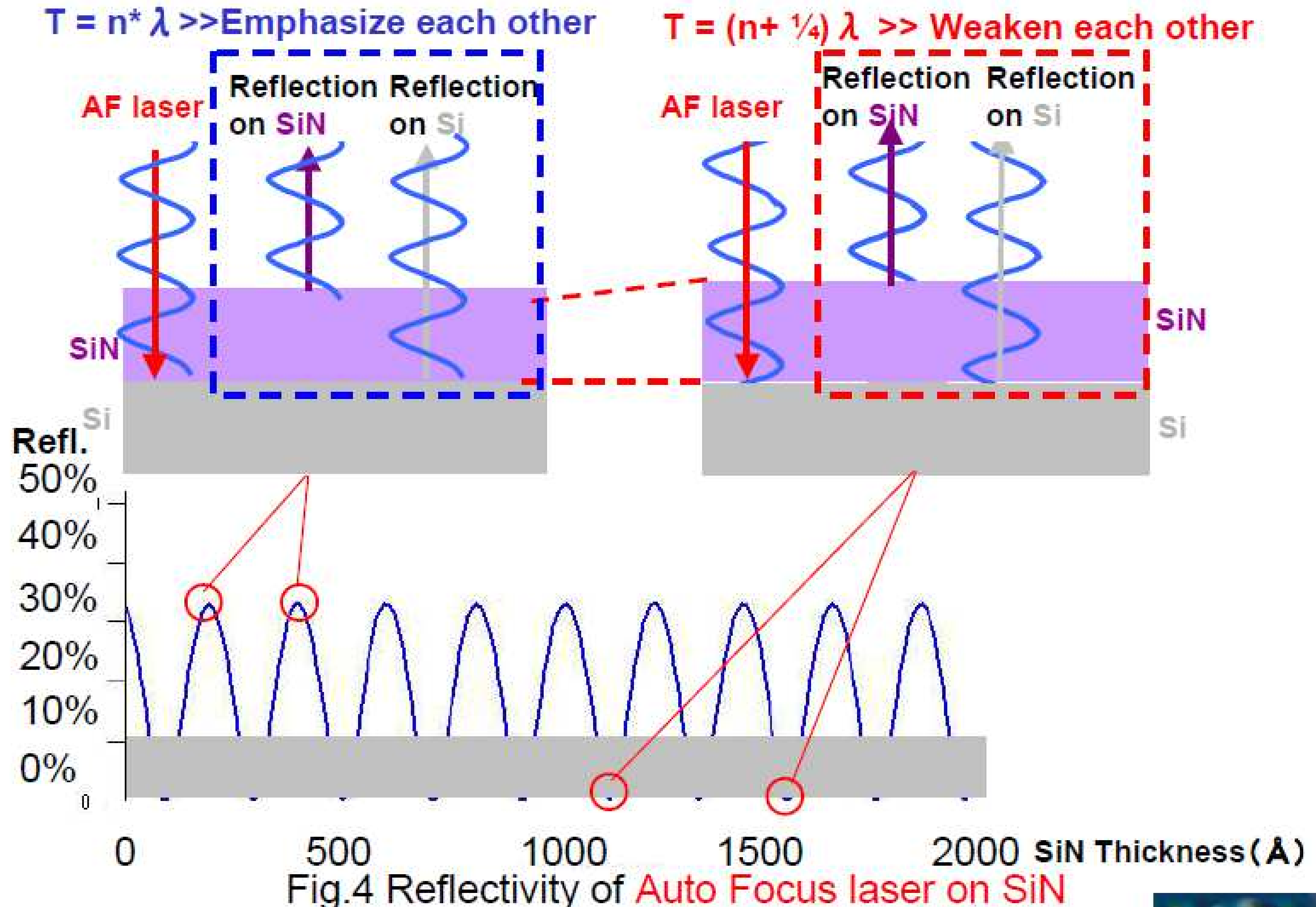
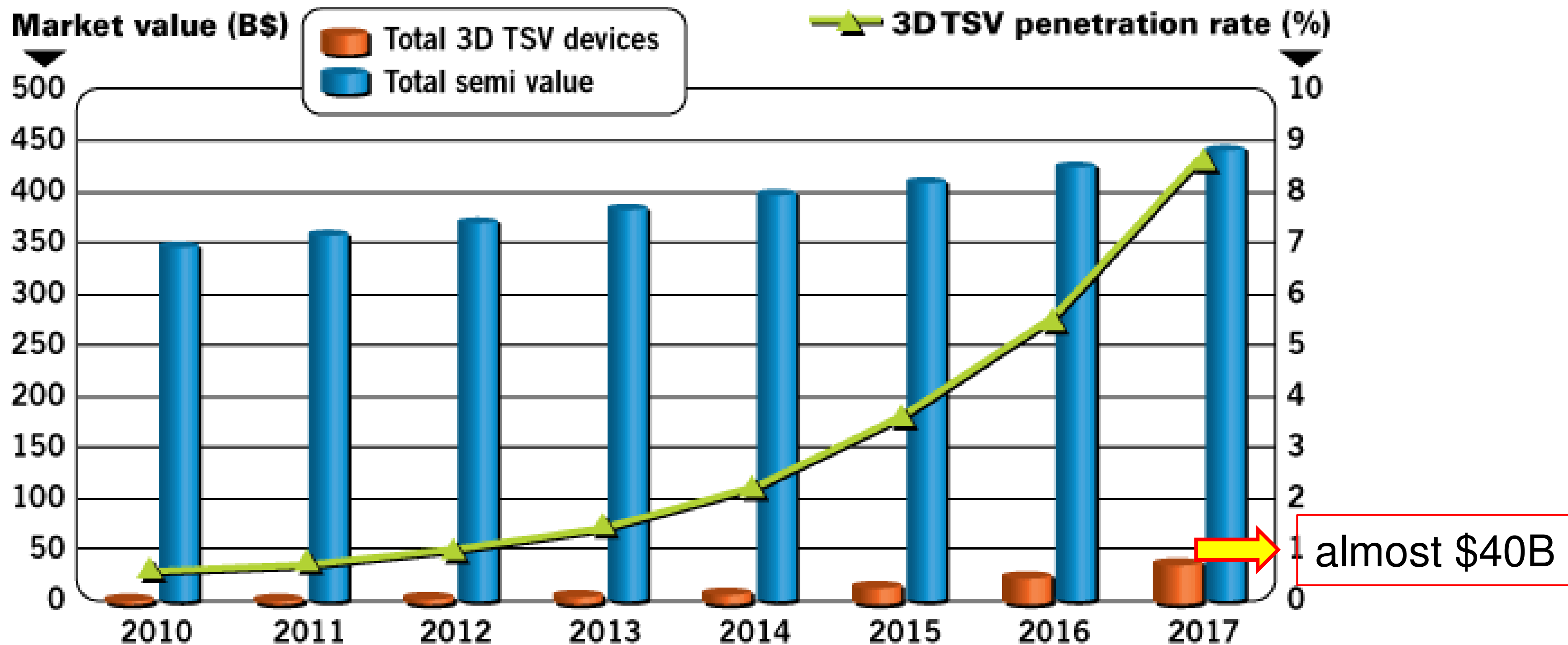


Fig.4 Reflectivity of Auto Focus laser on SiN

TSV Market Value



3D through silicon via (TSV) chips will represent 9% of the total semiconductors value in 2017, hitting almost **$40B**. Packaging, assembly and test market will reach to **$8B,** the middle-end wafer processing activity such as TSV etching filling, wiring, bumping, wafer testing and wafer-level assembly will reach to **$3.8B.**

Source : Yole Développement, Jul. 2012

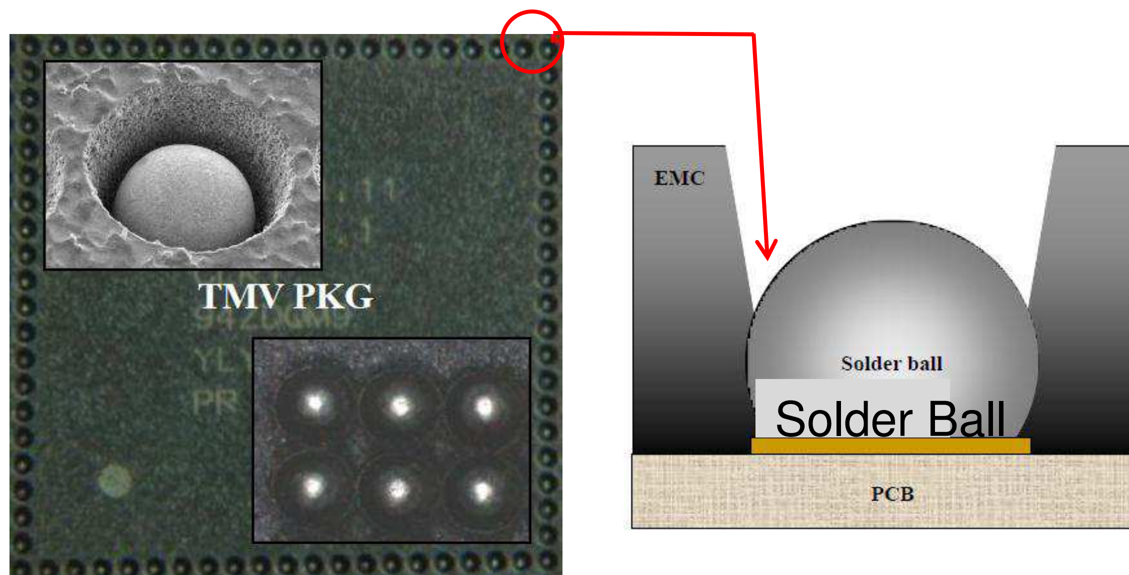
3D_TSV Commercialization Status

Amkor Technology®

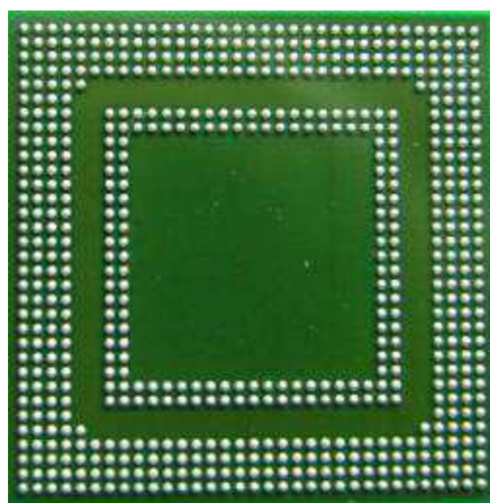
Key to 3D commercialization is a cost/performance ratio!

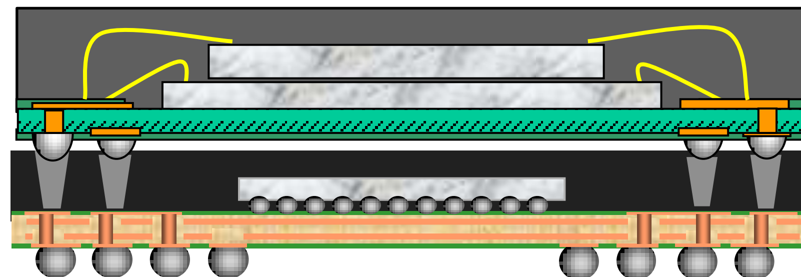
Application	Driver	Status	Barrier
Image sensors	Performance, Form factor	Production	None
CPUs + memory	Performance	28nm Si node or beyond	Cost, process, yield, infrastructure
GPUs + memory	Performance	2014	Cost, process, yield, infrastructure
FPGAs	Performance	Production	process, yield, infrastructure
Wide I/O memory with processor	Performance (bandwidth extension, lower power consumption), Form factor	2013	Cost, process, yield, KGD, infrastructure (including business logistics)
Memory (stacked)	Performance, Form factor (z-height)	2013	Cost, process, yield, assembly

Package Stack with TMV™ Technology

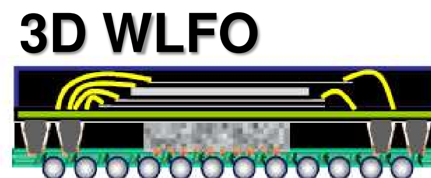


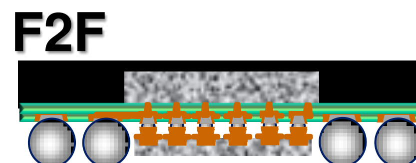
Via Formed by laser machining

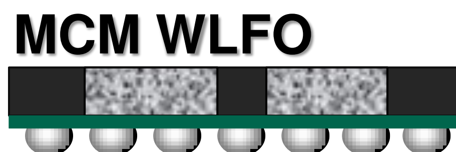


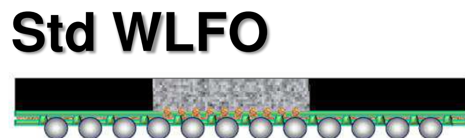


Package Stack with WLFO Technology









Thank you