Foundry TSV Enablement For 2.5D/3D Chip Stacking

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Hot Chips 24

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Customer-Driven Foundry Solutions

Outline

- 2.5D/3D Applications
- Foundry TSV Enablement
- Ecosystem Work Flow
- Summary

2.5D/3D Applications

2.5D Si Interposer Stacking

Cu dual damascene BEOL process for fine pitch RDL and passive device

Cu-pad

UBM

Capacitor

C4 bump

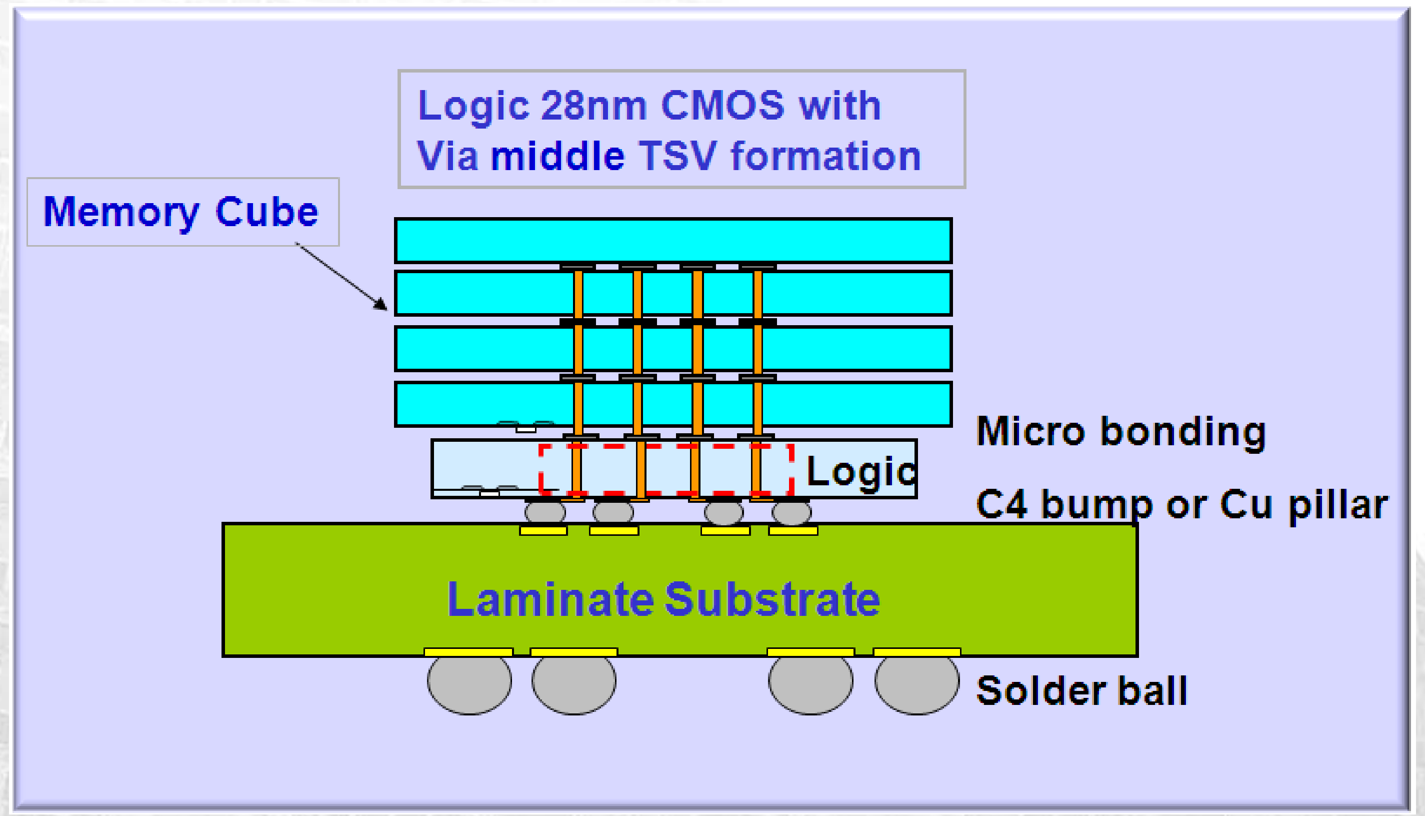
Laminate Substrate

Solder Ball

- Logic/logic: FPGA, networking infrastructure
- Logic/memory: Gaming, HPC

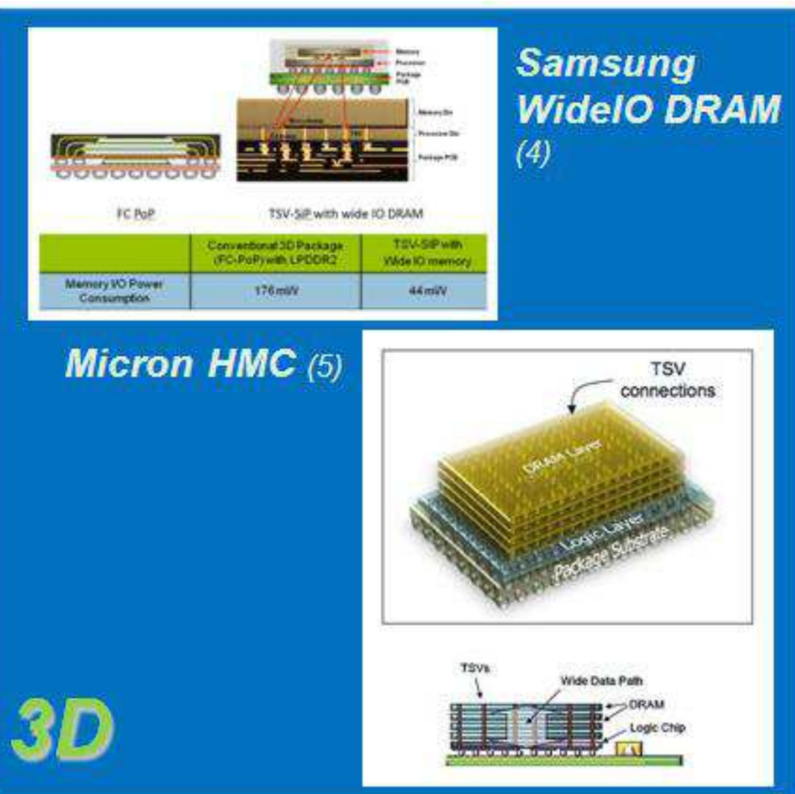
3D Logic/Memory Stacking

- Via-Middle TSV 28nm Logic + Memory Cube



- Mobile WideIO, Computing WideIO, HMC

Application Examples
- More are being developed



(1) http://low-powerdesign.com/sleibson/2011/10/25/generation-jumping-2-5d-xilinx-virtex-7-2000t-fpga-delivers-1954560-logic-cells-consumes-only-20w/
(2) http://eda360insider.wordpress.com/2012/06/01/friday-video-3d-thursday-xilinx-virtex-7-h580t-uses-3d-assembly-to-merge-28gbps-xceivers-fpga-fabric/
(3) eSilicon, "GSA 3D Working Group", July 2012
(4) http://www.ecnmag.com/news/2011/03/samsung-wide-io-memory-mobile-products-deeper-look
(5) http://denalimemoryreport.com/2012/06/28/arm-hp-and-sk-hynix-join-hybrid-memory-cube-consortium-hmcc-first-spec-due-by-end-of-year/

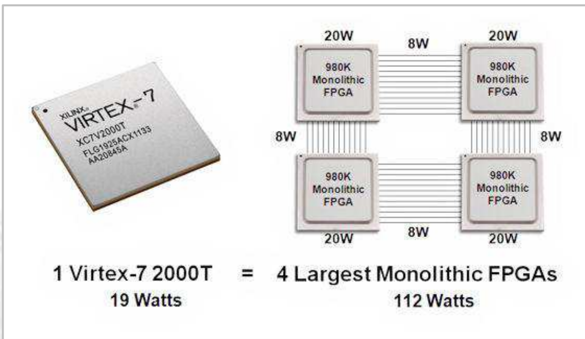
Cost-of-Ownership Advantages

Motivations:

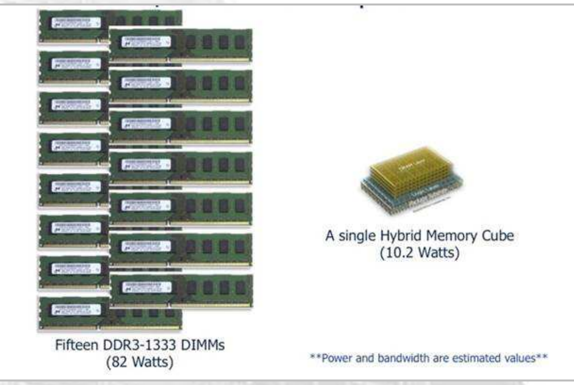
- Higher BW, lower W/BW, smaller form-factor

Opportunity of return on 3D IC investment:

- Chip process node optimization
  - Homogeneous partition
  - Cross-node combinations
- BOM cost optimization
  - Less demanding substrate/PCB, lighter cooling assembly, ...
- Ultimately: better product, better margin



Xilinx Virtex 7 *(1)*



Micron HMC *(2)*

(1) http://low-powerdesign.com/sleibson/2011/10/25/generation-jumping-2-5d-xilinx-virtex-7-2000t-fpga-delivers-1954560-logic-cells-consumes-only-20w/
(2) http://www.i-micronews.com/news/Micron-Samsung-TSV-stacked-memory-collaboration-closer-look,7766.html

Foundry TSV Enablement

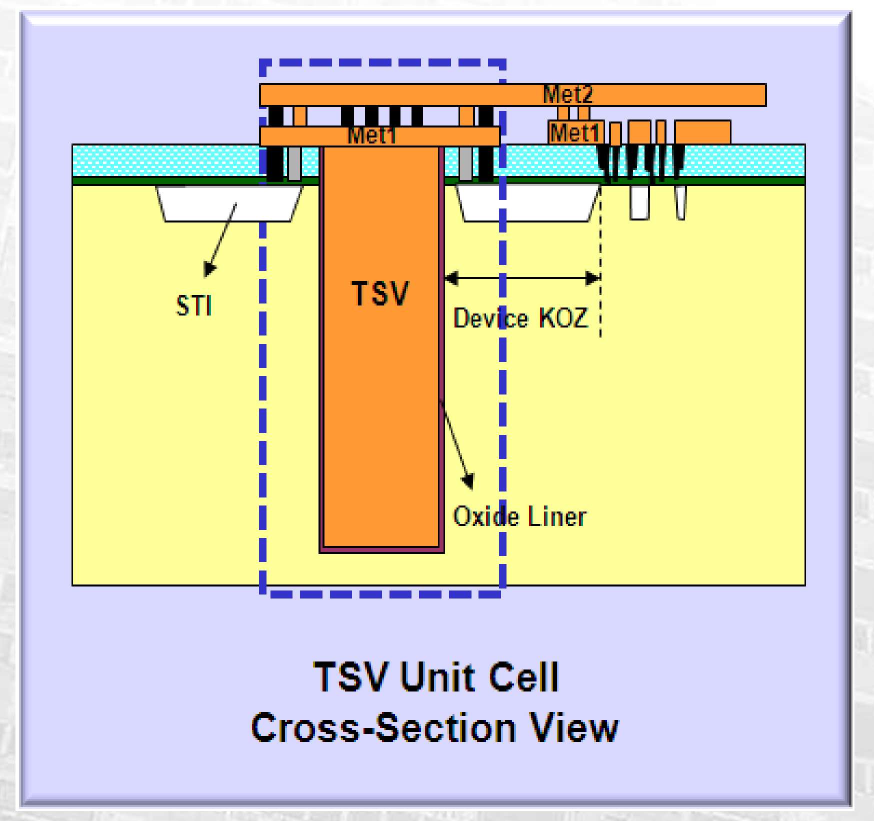
Customer-Driven Foundry Solutions

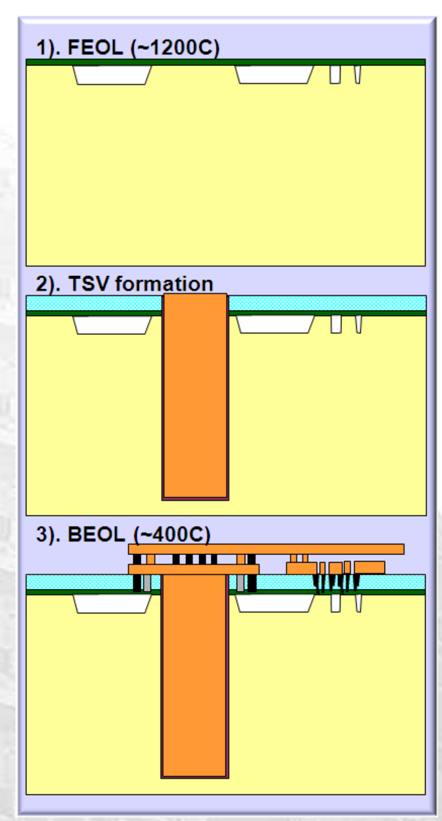
Foundry TSV Process Technology

- Mainstream: Via-middle Cu TSV
  - 2.5D: 65nm-generation BEOL
  - 3D: 28nm CMOS logic
- After 28nm entry, TSV for 3D may come as a standard option for foundry CMOS logic at 20nm and beyond

Example TSV Unit Cell

- Via-Middle TSV for 3D

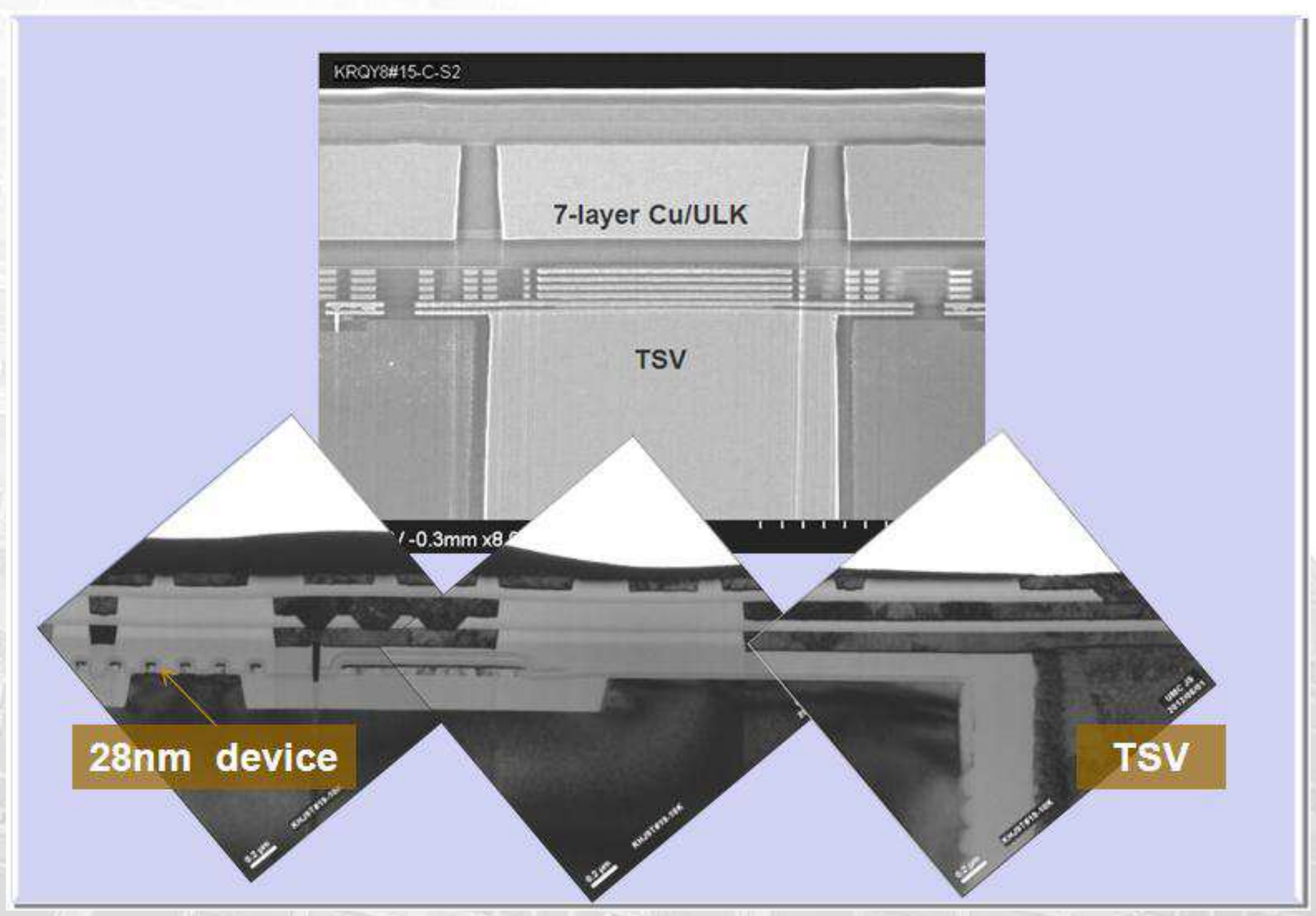




(drawn not to scale)

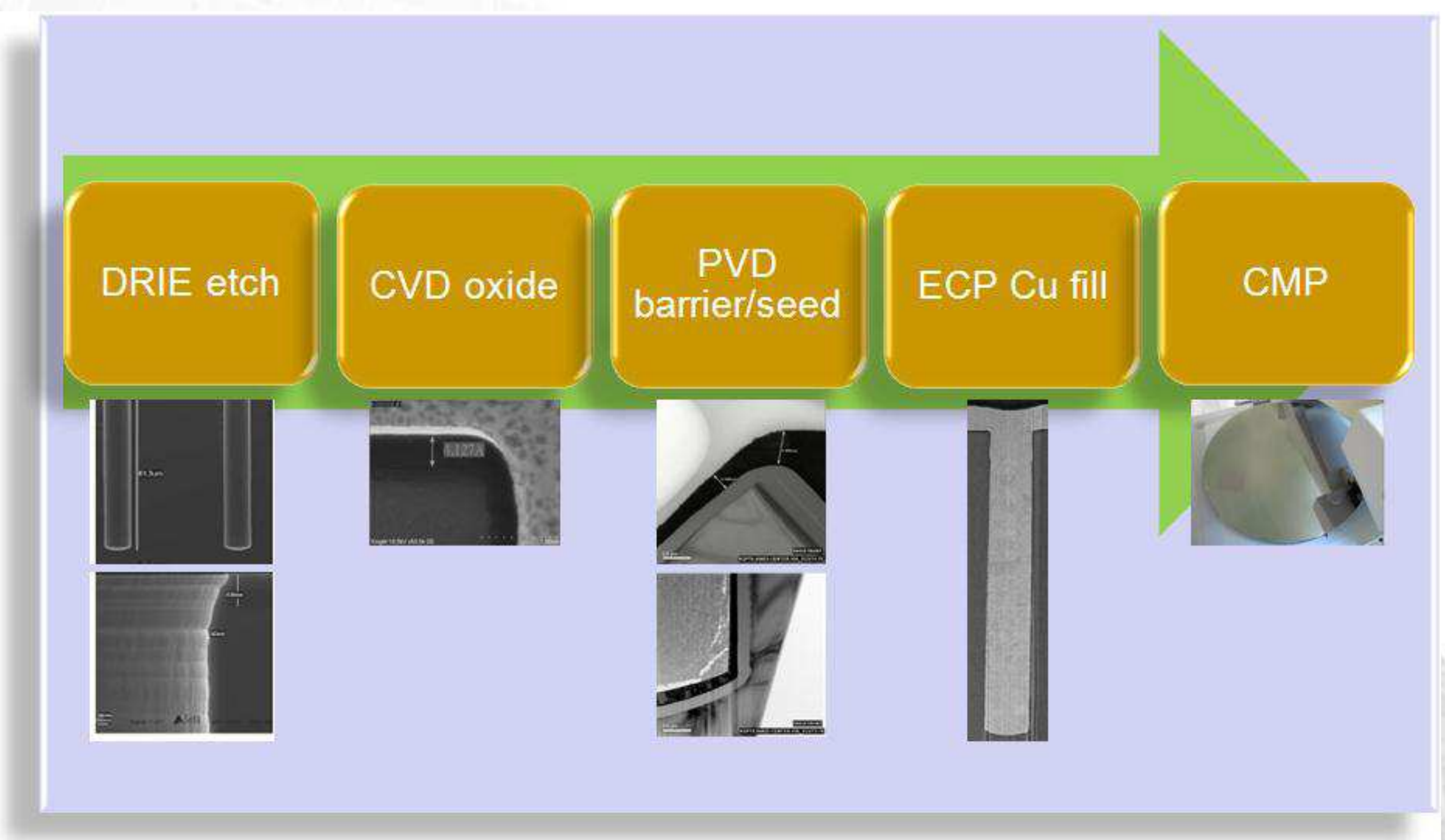
- TSV formed after CMOS, before contact/metal

UMC 28nm 3D IC



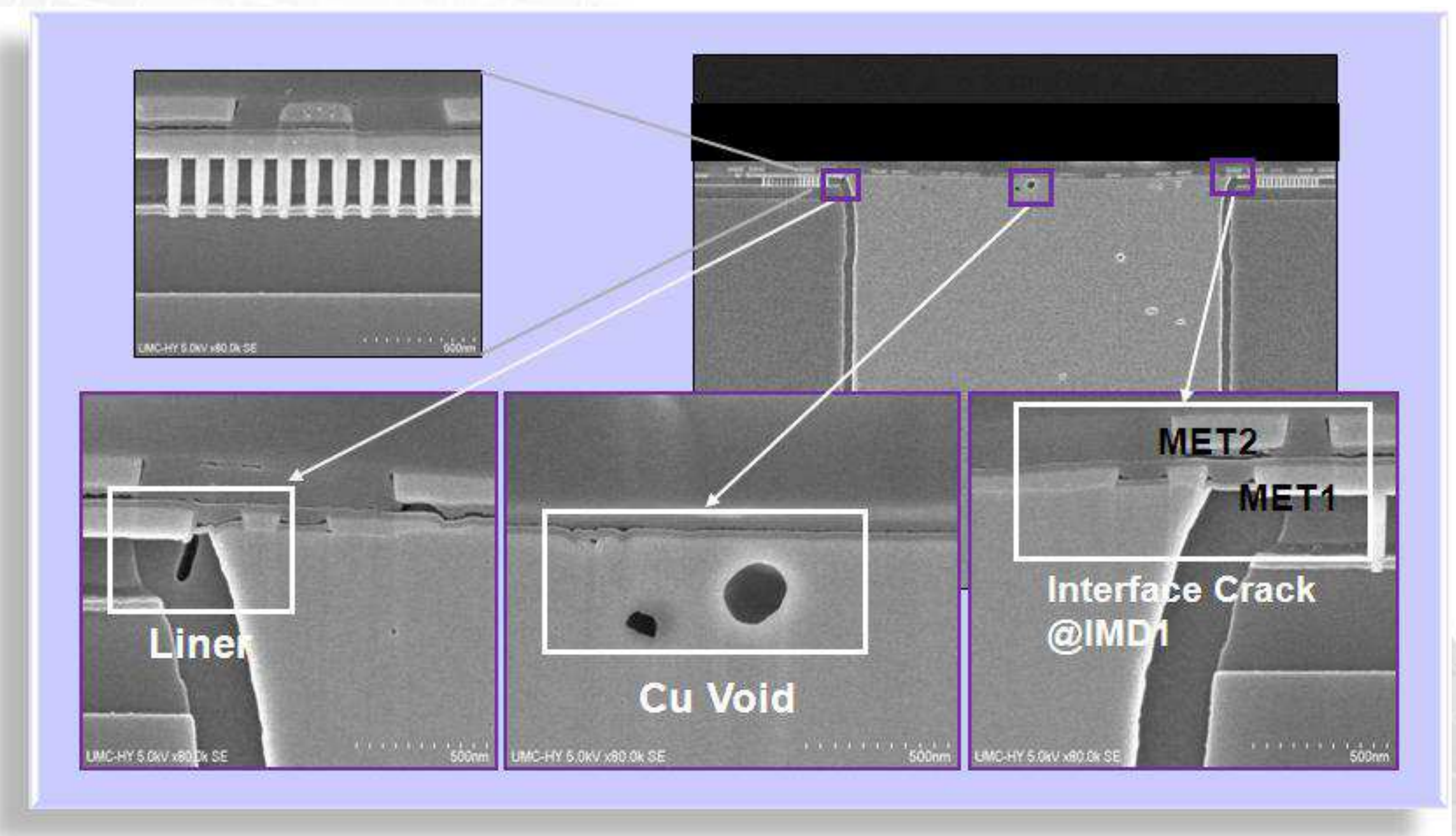
(CMOS device and TSV in proportion)

UMC Via-Middle TSV Unit Process



- Leveraging existing CMOS tools and capability
- Size is new to fab practice: diameter/depth

Early Stage TSV Process Issues



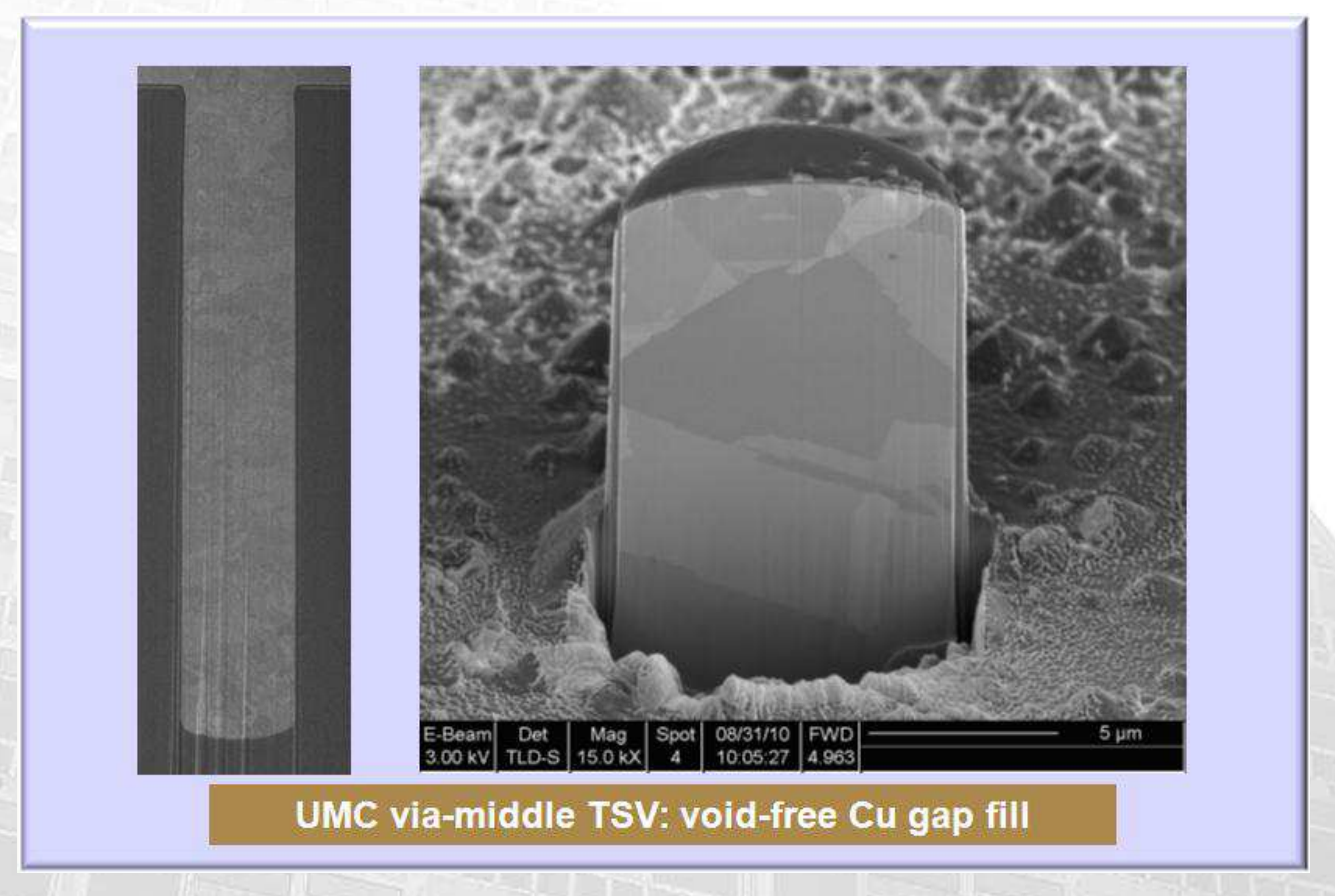
- TSV integrity – Cu fill, oxide liner, metal stack

ECP Cu Fill Process Optimization

- Cu pumping reduction

- ECP Cu plating critical to TSV integrity

UMC Via-Middle TSV Solution



UMC via-middle TSV: void-free Cu gap fill

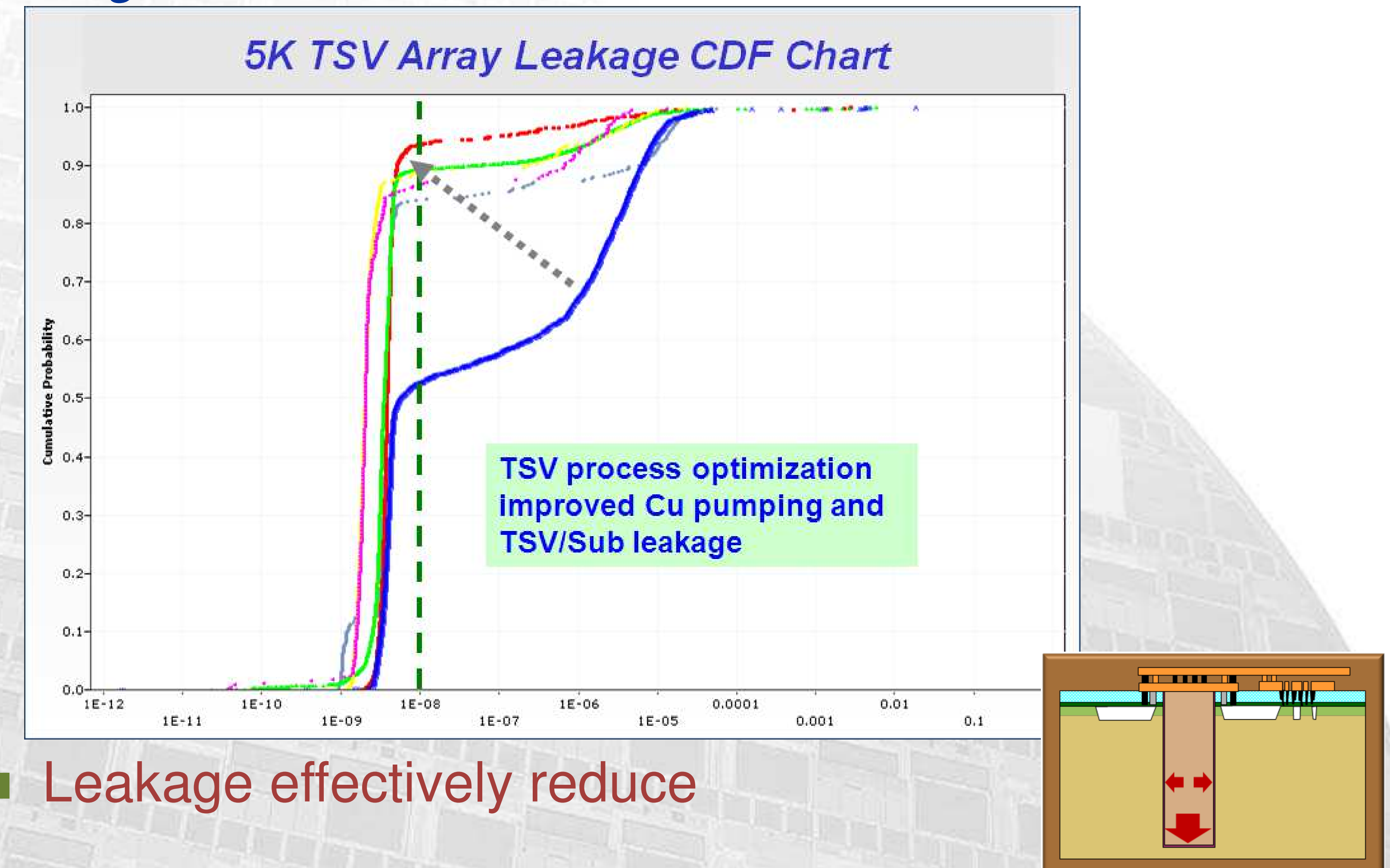
TSV Top Side Impact Evaluation
- BEOL WAT testkeys

WAT test item	Layer	Testkey rule (w/s)	Above TSV	Cross TSV	Beside TSV	After Sinter
Metal Bridge	M3	1x W /1x S	Passed	Passed	Passed (min. x=1)	No significant change
		2x W /2x S	Passed	Passed	n/a	
	M4	1x W /1x S	Passed	Passed	Passed (min. x=1)	
		2x W /2x S	Passed	Passed	n/a	
Metal Resistance	M3	1x W /1x S	Passed	Passed	Comparable for variable x	No significant change
		2x W /2x S	Passed	Passed	n/a	
	M4	1x W /1x S	Passed	Passed	Comparable for variable x	
		2x W /2x S	Passed	Passed	n/a	
Via Bridge	V3	Com_run Via	Passed	Passed	Comparable for variable x	No significant change
		Non_com Via	Passed	Passed	Comparable for variable x	

- Routing over TSV allowed

TSV Bottom Side Impact Evaluation

- Leakage CDF



- Leakage effectively reduce

CMOS Impact Evaluation (3D)

- Keep-Out Zone (KOZ) Characterization

Core NMOS W/L=0.2/0.04um offset @H50V40

NMOS

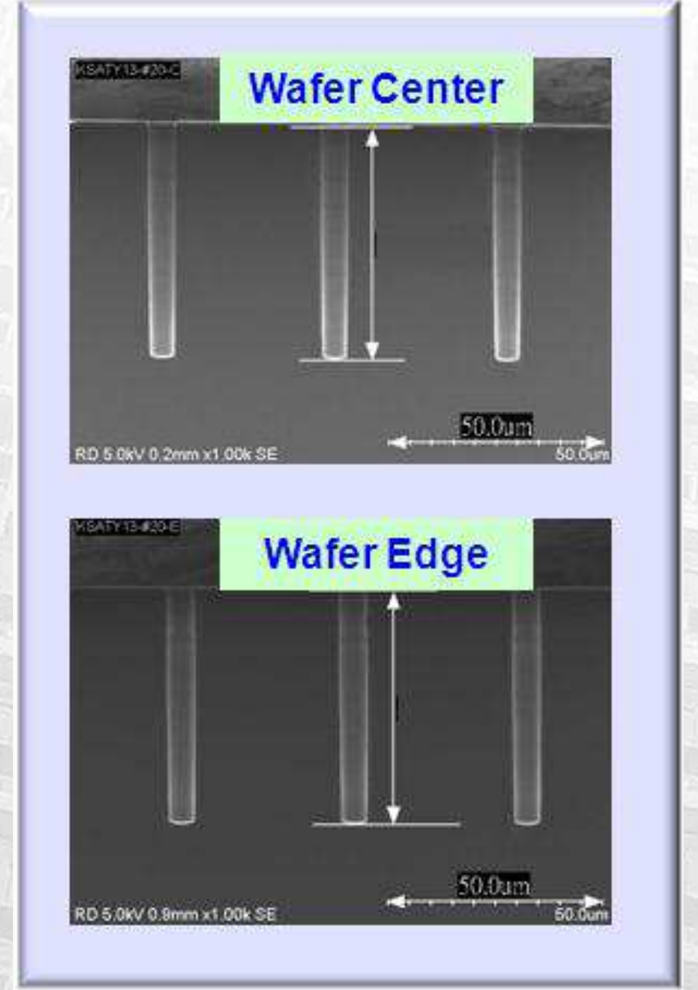
Core PMOS W/L=0.2/0.04um offset @H50V40

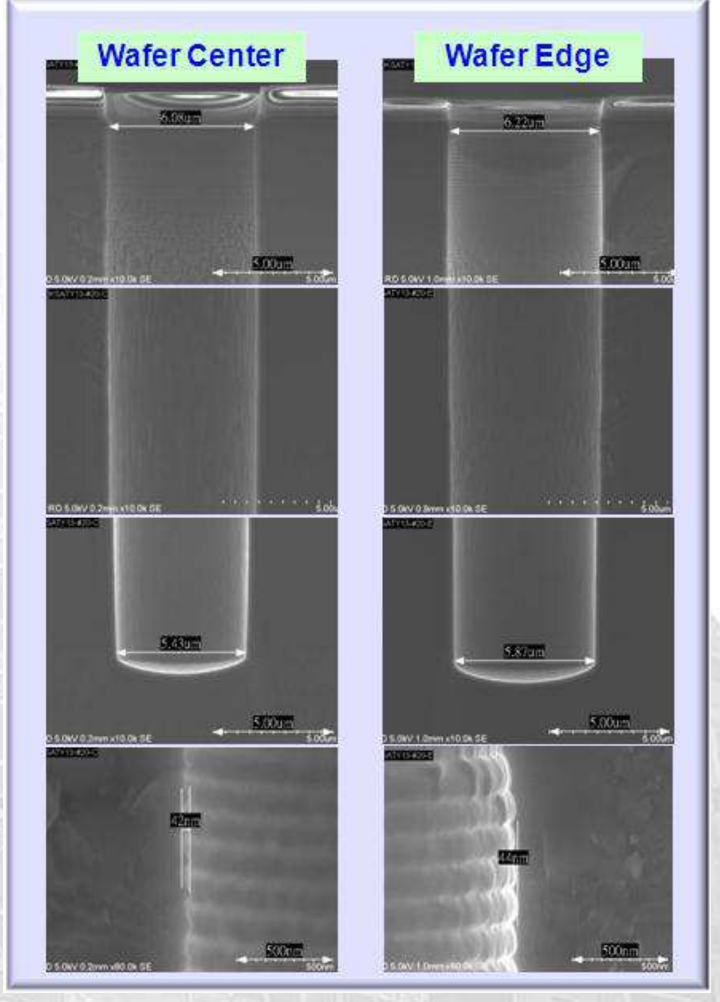
PMOS

- KOZ: DIon< 3% at distance >=5um
  - Device: 28nm HKMG core device
  - TSV pitch: JESD229 50/40um

Via Middle TSV (3D)

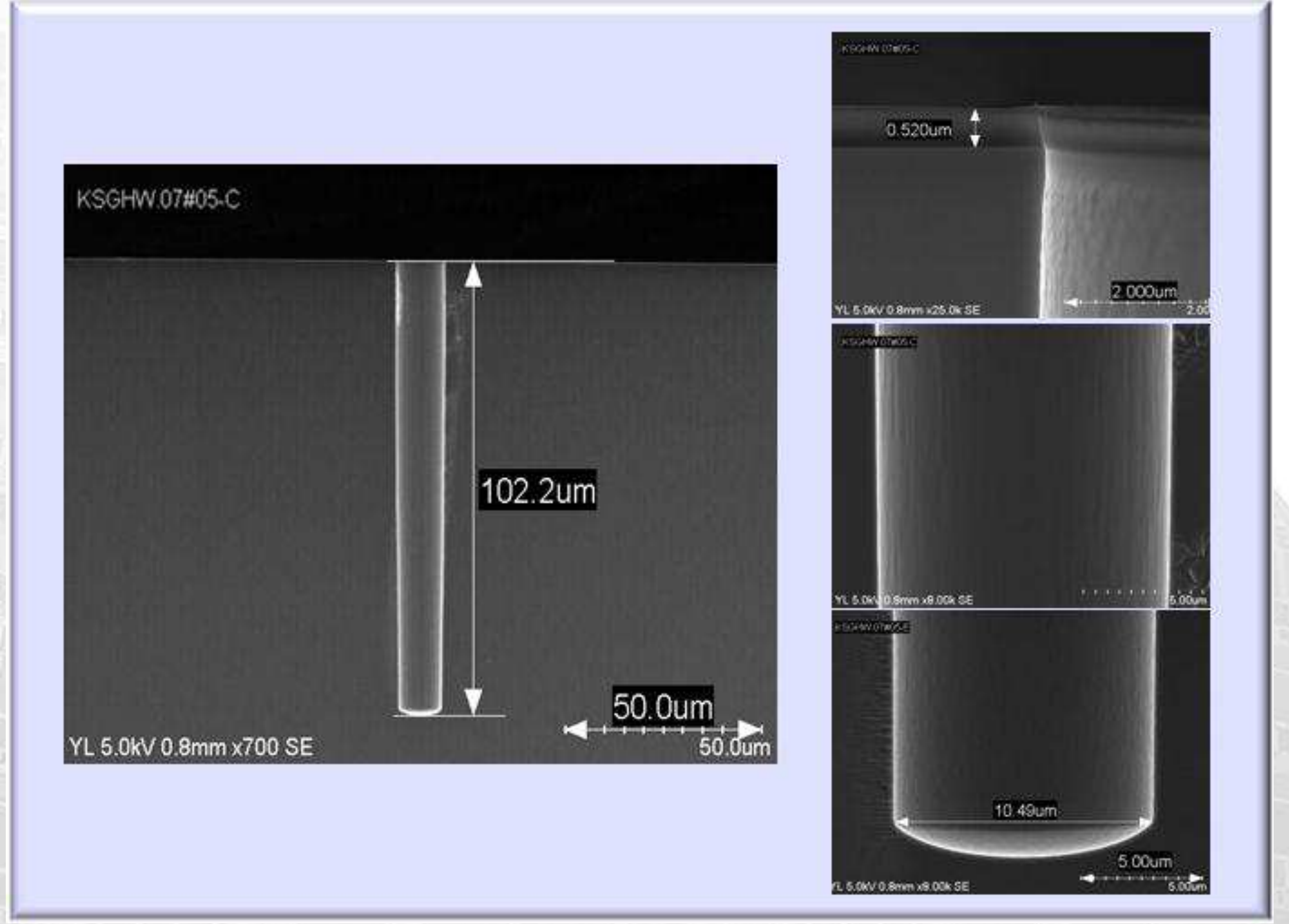
- 6um diameter, 54um depth





Si Interposer TSV (2.5D)

- 10um diameter, 100um depth



Uniformity Evaluation

- 2.5D Si Interposer, 10x100um

TSV (μm)

AVG+3S:106.5

AVG:105.97

AVG-3S:105.43

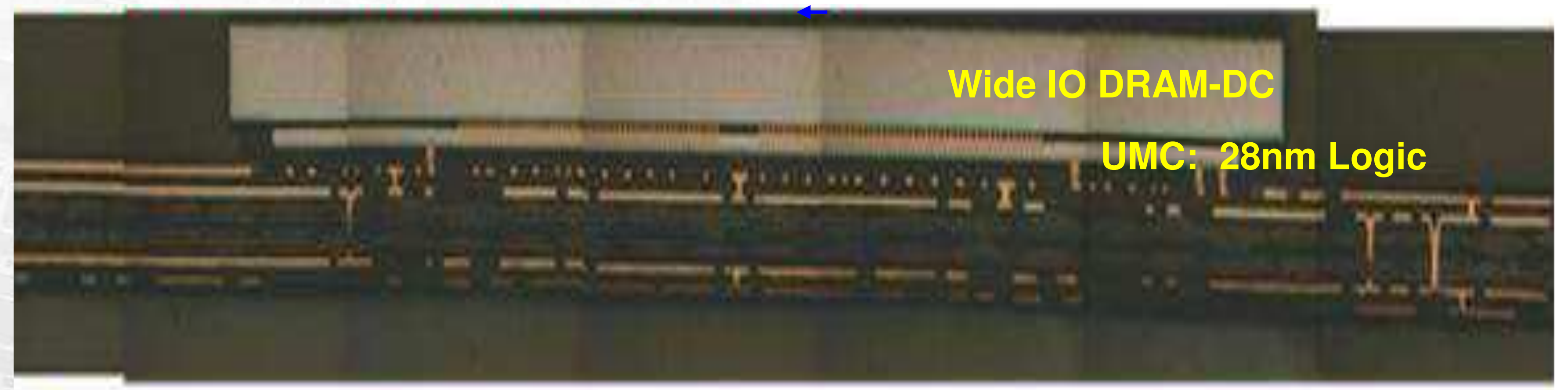
Standard Deviation = 0.2um

TSV (μm)

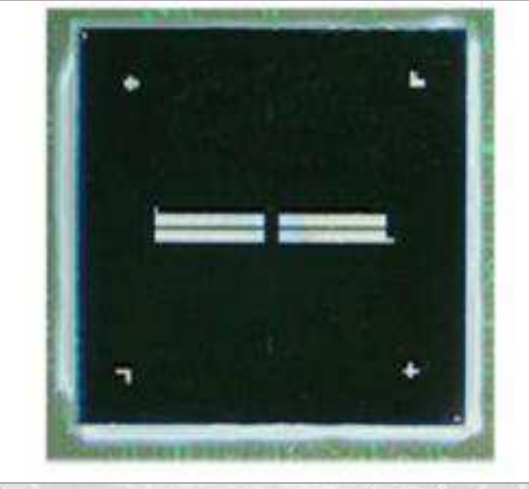
Chip No.

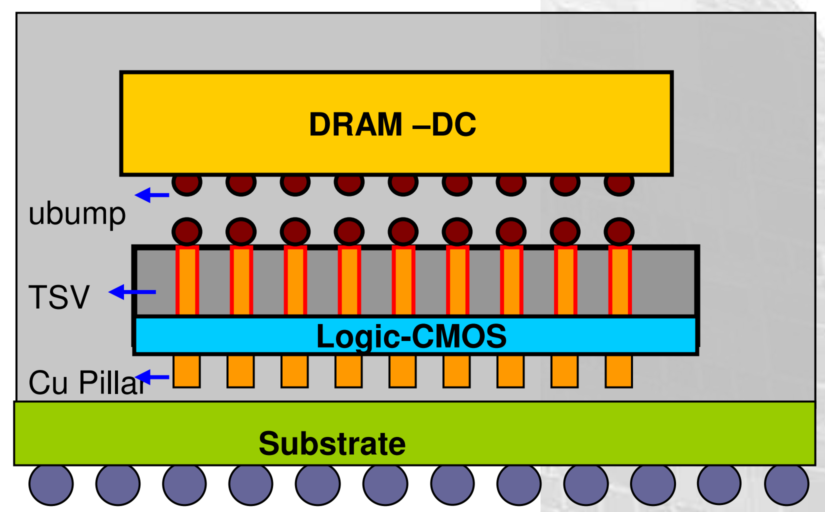
Chip No.	1	2	3	4	5	6	7	8	9	10	11	13	14
N	6	6	6	6	6	6	6	6	6	6	6	6	6
AVG	105.92	106.04	105.87	105.79	106.01	106	106.08	105.85	105.89	106.03	105.97	106.11	106.02
MIN	105.72	105.97	105.67	105.65	105.72	105.81	105.97	105.62	105.56	105.81	105.88	105.83	105.87
MAX	106.19	106.17	106.15	106.03	106.22	106.19	106.22	106.14	106.2	106.26	106.15	106.38	106.22
SD	0.1728	0.081483	0.18275	0.14248	0.17959	0.1631	0.10336	0.17108	0.22308	0.17138	0.10939	0.23341	0.15301

UMC 3D IC TV Stacking & Package



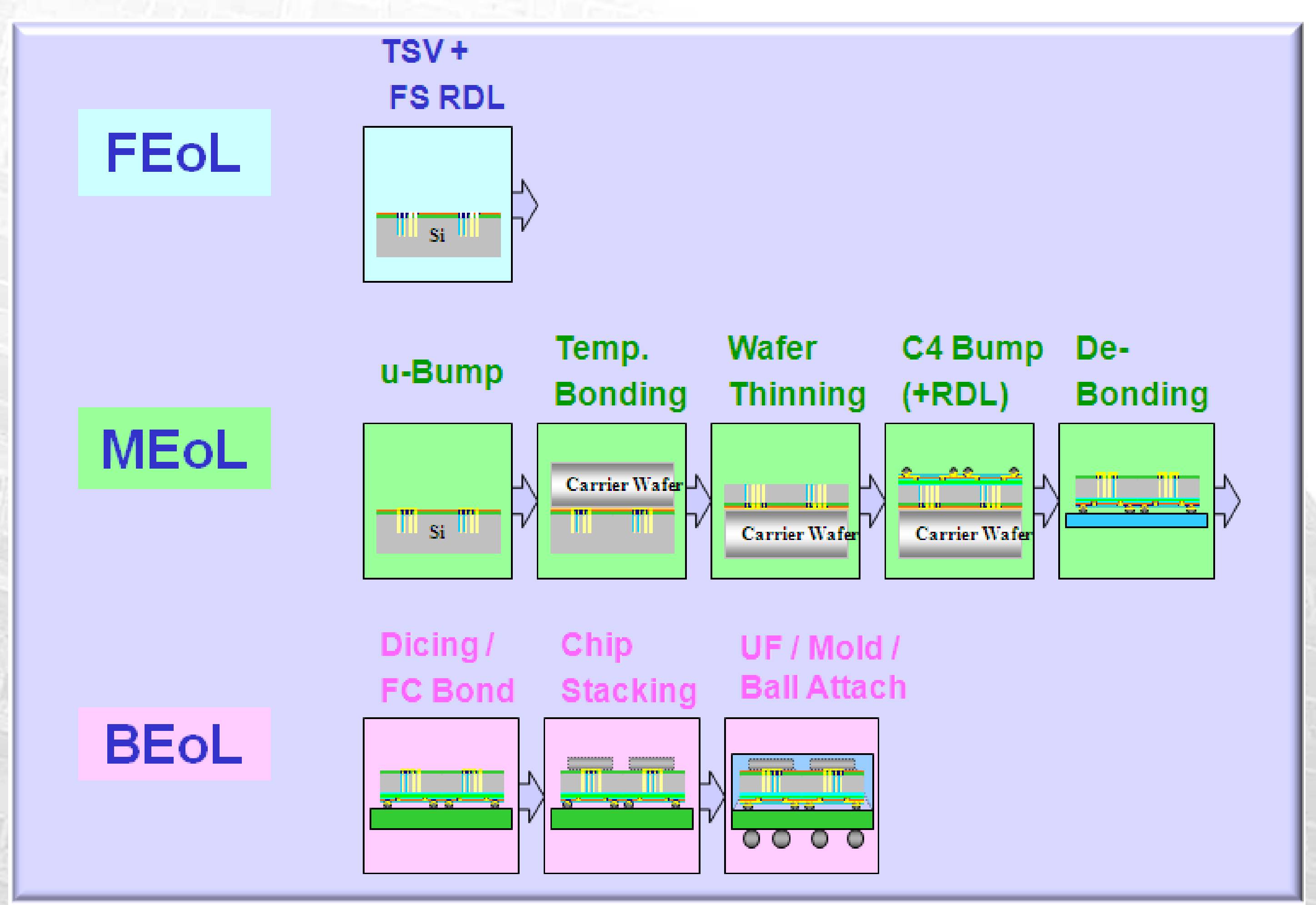
JEDEC WideIO interface





Ecosystem Work Flow

Example 2.5D Stacking Flow



Various Work Models

<table>
<tr><th colspan="2" rowspan="2"></th><th colspan="2">FEOL</th><th colspan="2">MEOL</th><th colspan="2">BEOL</th></tr>
<tr><th>Logic</th><th>TSV + FS RDL</th><th>Wafer Thinning</th><th>BS RDL + Bump</th><th>Assembly</th><th>Test</th></tr>
<tr><td rowspan="3">2.5D</td><td>OSAT MEOL</td><td></td><td>Foundry</td><td colspan="4">OSAT</td></tr>
<tr><td>Foundry MEOL</td><td></td><td colspan="3">Foundry</td><td colspan="2">OSAT</td></tr>
<tr><td>Foundry Turnkey</td><td></td><td colspan="5">Foundry</td></tr>
<tr><td rowspan="3">3D</td><td>OSAT MEOL</td><td colspan="2">Foundry</td><td colspan="4">OSAT</td></tr>
<tr><td>Foundry MEOL</td><td colspan="4">Foundry</td><td colspan="2">OSAT</td></tr>
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</table>

- Service scopes distinguished by MEOL inclusion
  - Consult your foundry/OSAT
- Work flow optimization may depend on BOM cost, stack recipe and test strategy

Foundry TSV Design Collaterals

Scheme	Feature Size				Document Status				
	TSV CD/Depth (um/um)	RDL Cu Layers	Cu Thickness /L /S (um/um/um)	Al Thickness (um)	Topologic Layout Rule	Electrical Design Rule	Interconnect Model	DRC Command File	LVS Command File
1.0um-wide	10/100	0.13 Inductor	2.0 /1.00/1.00	2.50	Ready	Ready	Ready	Ready	Ready
0.4um-wide	10/100	55nm 4X	0.8 /0.40/0.40	1.45	Ready	Ready	Ready	Ready	Ready
0.56um-wide	10/100	65nm 6X	1.25 /0.56/0.56	3.60	Ready	Ready	Ready	Ready	Ready

(UMC 2.5D Si interposer documents)

- Consider TSV a passive device with rule decks/models
  - Typical foundry engagement applies under ecosystem work flow

UMC Ecosystem Effort

Quarter	Effort
1Q12	• Foundry TSV process optimization
2Q12	• MEOL flow & QA alignment
3Q12	• MEOL 2.5D/3D chip stacking
4Q12	• Product level packaging & testing • Reliability assessment

Summary

Summary

- Foundry TSV process demonstrated
  - Applicable to both 2.5D/3D
  - Leverage existing CMOS process technology
  - Key process issues identified & conquered
- Ecosystem work flow
  - Typical foundry/OSAT engagement flow applies for both 2.5D/3D, among other models
- Foundry TSV next step: ecosystem focus
  - Product level reliability assessment
  - Potential EDA collaboration for emerging 3D tools

Thank you for your attention!

Contact foundry@umc.com or info@hotchips.org .

Thank You!