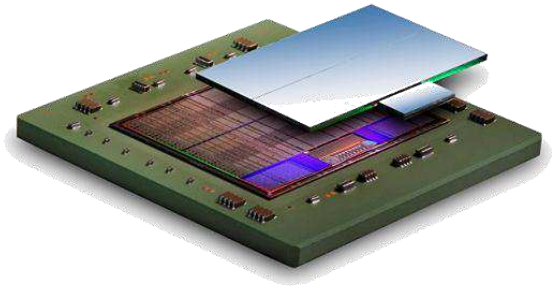
3-D Stacking Tutorial Introduction

AMD Amkor Technology QUALCOMM UMC XILINX

Liam Madden
Corporate Vice President
Xilinx
Aug 27th 2012



Dedicated to the Memory of Chuck Moore: Visionary

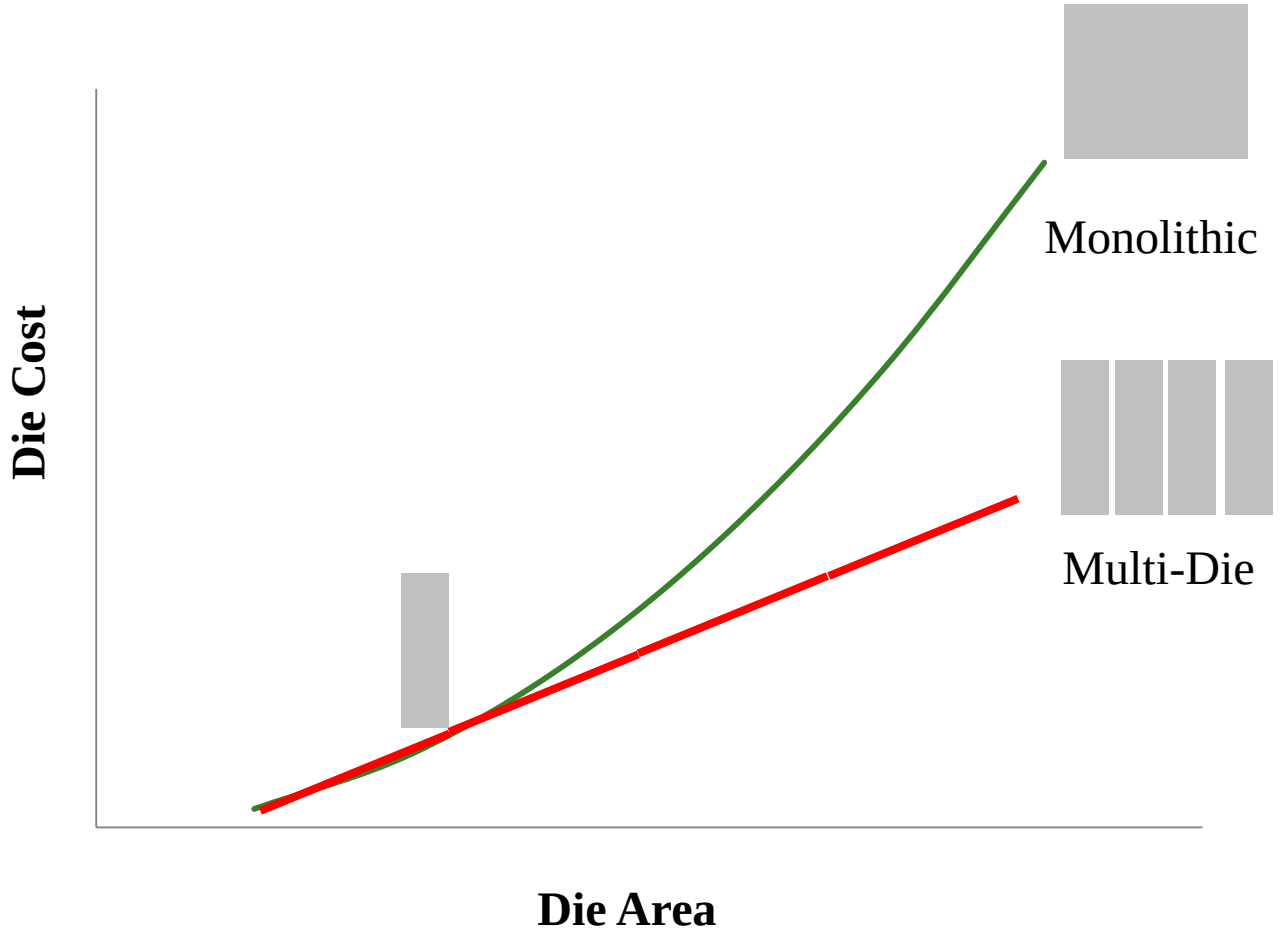
Chuck Moore,
AMD Corporate Fellow
1961-2012

Agenda

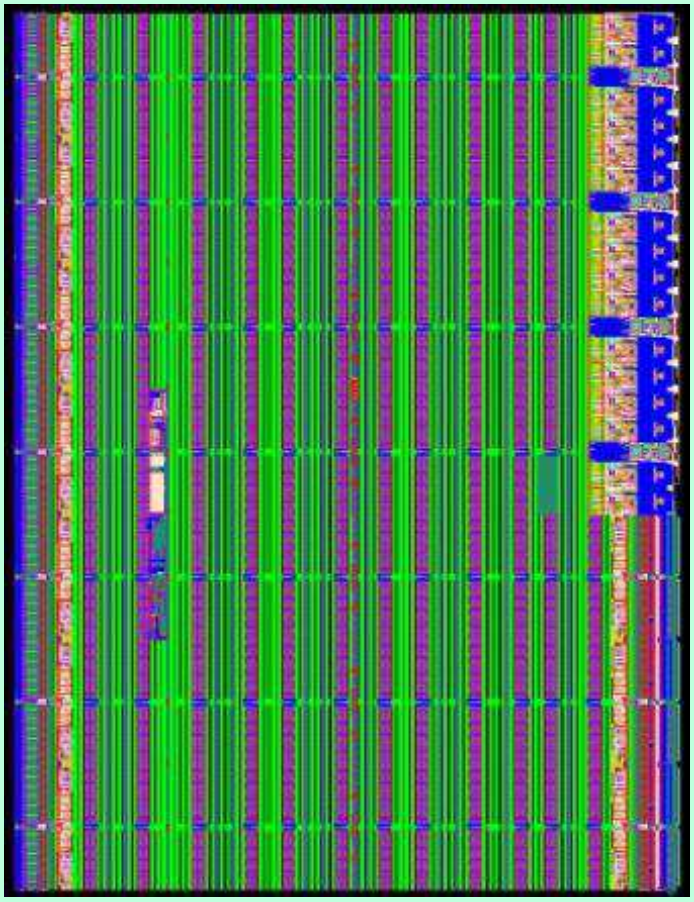
- Introduction: Liam Madden, Corp VP, Xilinx (2:00-2:15)
- Technology: (2:15-3:05)
  - Foundry: Remi Yu, Director Marketing, UMC
  - OSAT: ChoonHeung Lee, Corp VP, Amkor
- Design Considerations: (3:05-3:55)
  - Mobile Communications: Riko Radojcic, Director, Qualcomm
  - FPGA: Shankar Lakka, Director Integration, Xilinx
- Break (3:55-4:10)
- System Implications (4:10-5:00)
  - Processor and GPU: Bryan Black, Senior Fellow, AMD
  - Integrated Optics, Ephrem Wu, Senior Director, Xilinx
- 5:00-5.30 Panel Discussion

Cost Comparison: Monolithic vs Multi-Die

"Moore's Law is really about economics" Gordon Moore



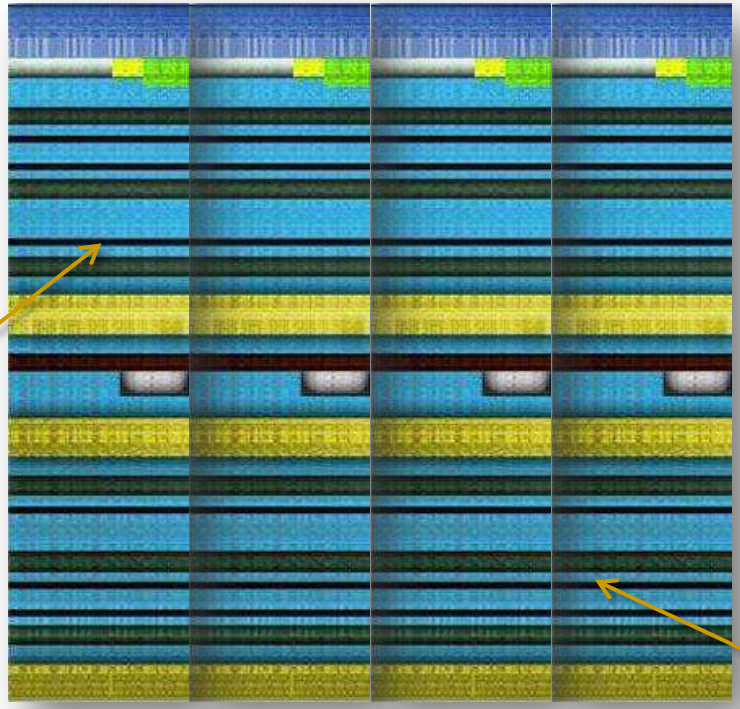
Why is first 3D logic product an FPGA?



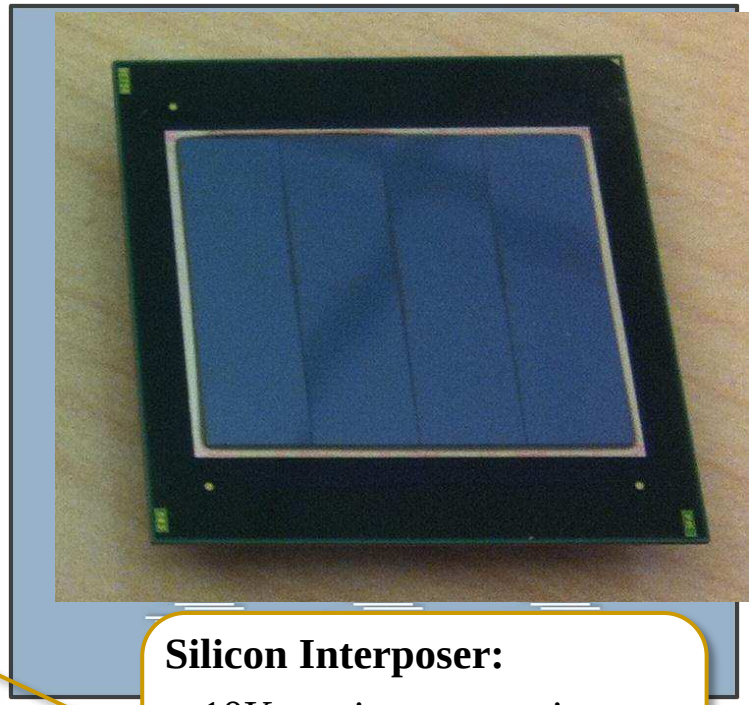
- Natural partition using “long lines”
- Very low “opportunity cost”
- No 3rd party dependence
- “Size matters” to customers
- Compelling value proposition “next generation density in this generation technology”

Virtex 2000T: Homogeneous 2.5D

FPGA slice



FPGA Slices Side-by-Side

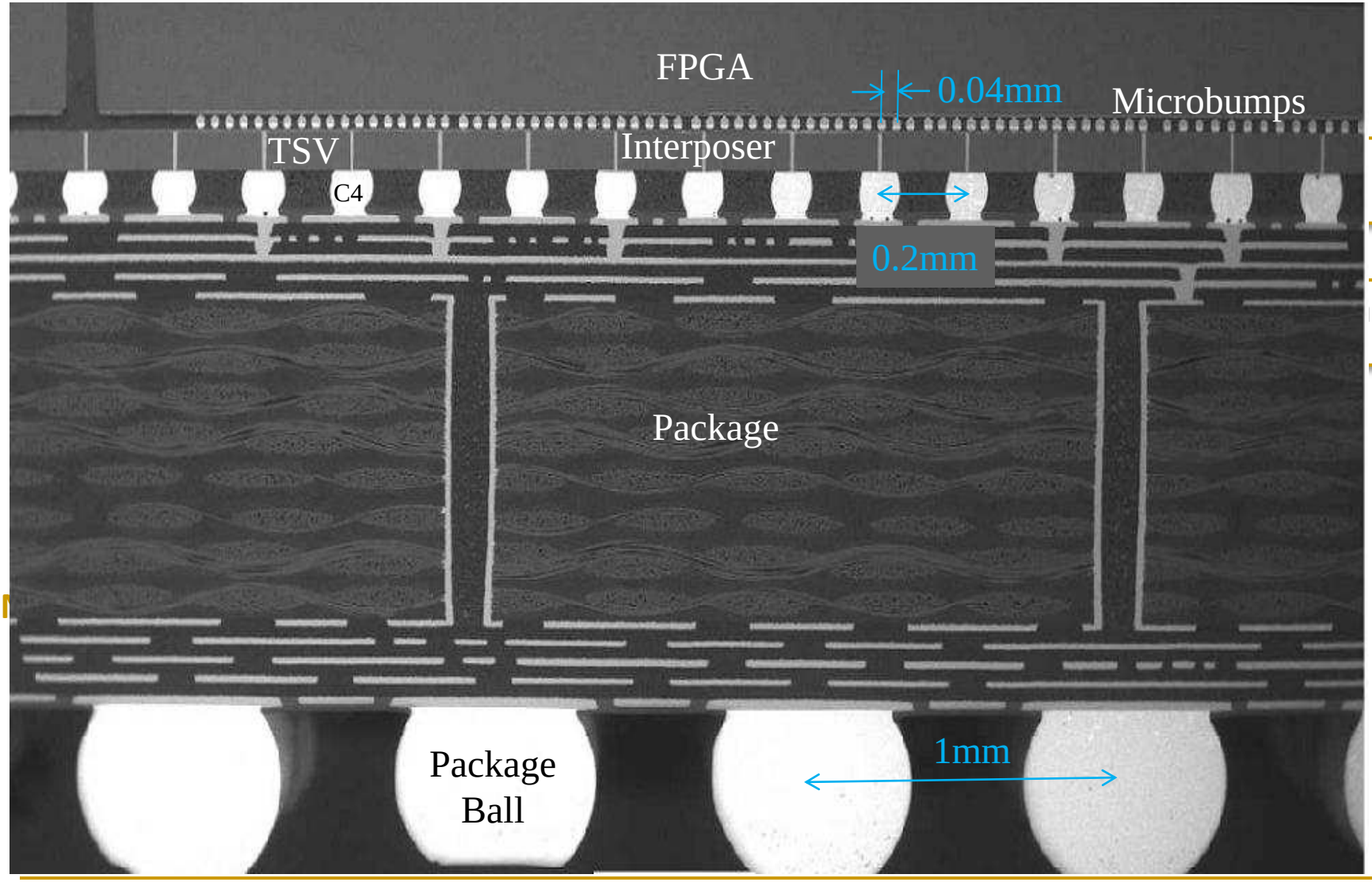


Silicon Interposer:

>10K routing connections between slices

~1ns latency

Elements of SSIT

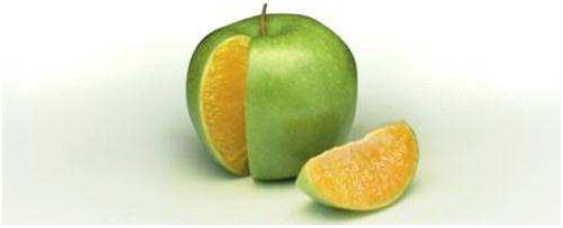


3 Decades of Microprocessor Integration: A personal history

"Integrate or be integrated" Fred Webber, former CTO AMD

Year	Company	Product		Integration Level						
				Core				L2$	North Bridge	GPU
				DP	Ctl	L1 $	FPU			

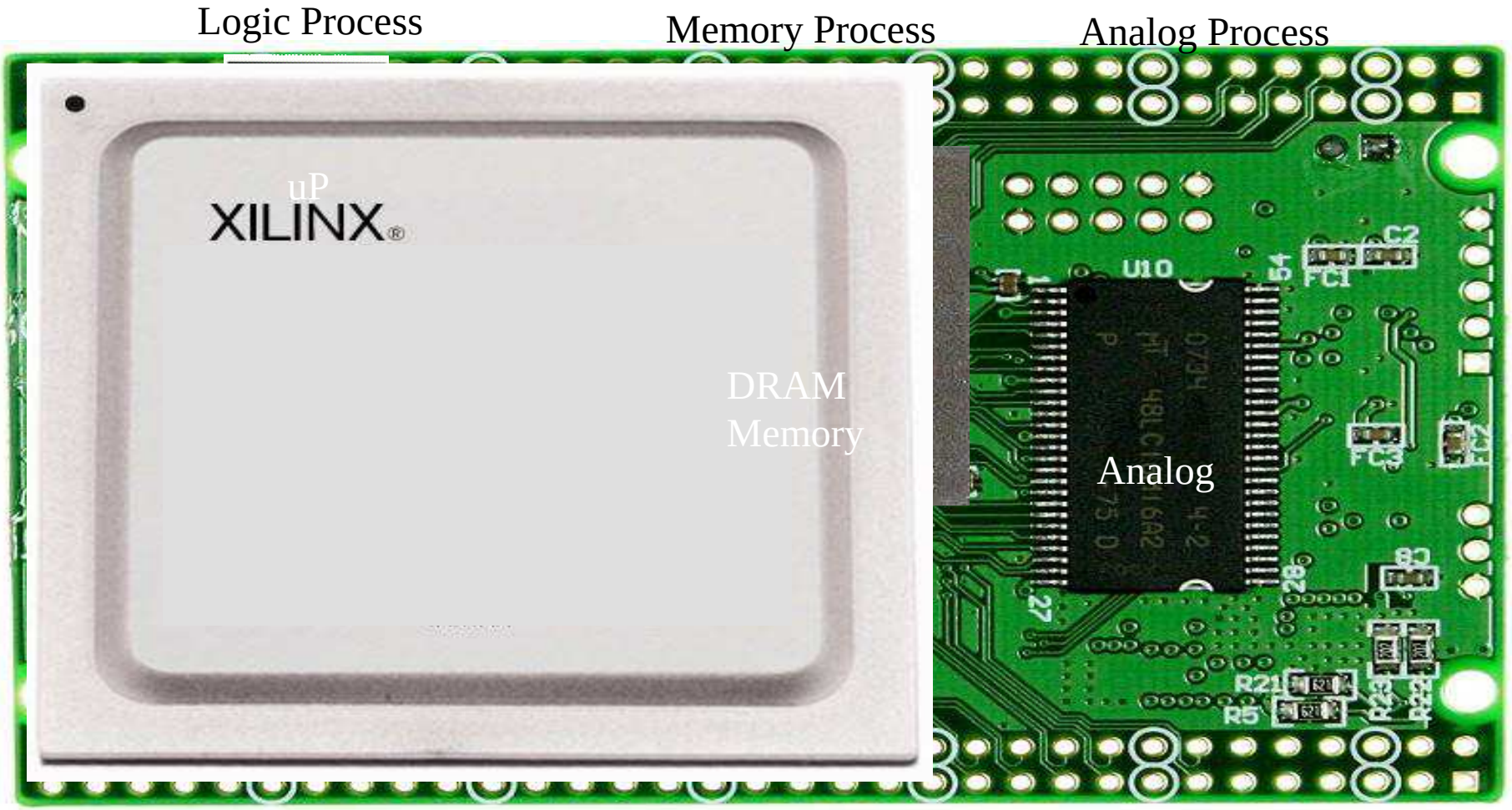
STACKONOMICS



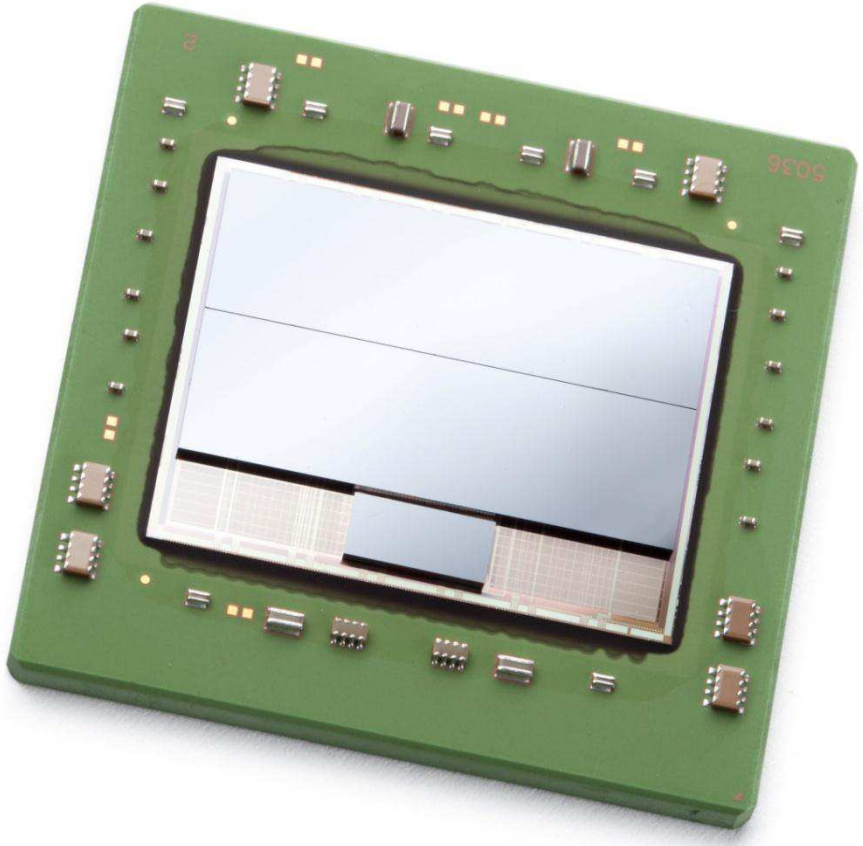
What happened to System on a Chip?

	Logic	Memory	Analog
Global Revenue 2011	$150B	$68B	$45B
Moore Scaling	Good (except I/O)	Good (except I/O)	Poor
Technology "Vintage"	2012	2012	2000
Transistor Characteristics	High performance/ Low leakage	Low leakage/ moderate performance	Stable with good voltage headroom
Metallization	>9 layers	<5 layers	<6 layers
Differentiators	High density logic	Charge storage	Passives, Optical

Crossing the packaging chasm



7V580T – Dual FPGA Slice with 8x28Gb/s SerDes Die



Virtex-7 HT @ 28Gbps