X-Gene™: 64-bit ARM CPU and SoC

Paramesh Gopi
Gaurav Singh
Greg Favor

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Cloud Computing Technology Trends

Fabric Interconnect between Rack Units

- **High Density Servers → " Sea of CPUs"**
  - Smaller & power-efficient CPUs; Beefier memory & IO subsystems
  - Distributed Fabric → networking & storage IO sharing & virtualization
- **Server-on-Chip (SoC) Approach**
  - Integrated NIC and IO chipset
  - CPU/ GPU combination for HPC applications
- **Active Power Management**
  - Firmware based optimization based on user Workload (Power is measured through TDP)
  - Maximize performance while managing TDP
- **Server Standardization**
  - Service provider specified
  - ODM designed & manufactured
  - Open Source/ non-commercial SW base
  - Open Stack, Open Compute

Cloud Servers - Typical Form Factors

Public Cloud

Applications

- Scale Out Services → Hosted Mail, Search, Social, Cloud Hosting

Platforms

- Dell PowerEdge C, HP ProLiant Microserver, DCS custom

Typical Specifications

- 1/2 Socket 2/4 core 2.8GHz, 80W
- 280 SpecIntRate
- System Power <500W; Cost <$2K

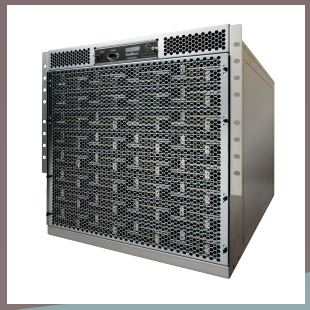
Building Out vs. Scaling Out

TODAY: 2 RU

- 2 Nodes per Rack Unit
- 2 Sockets @ 95W each
- Shared Chassis, Power Supply & Cooling
- Google, FB, Amazon Custom Datacenters

3 RU

- 8/12 Nodes in 3RU
- Single Socket @ 45W
- Shared Chassis, Power Supply, & Cooling
- Dell PowerEdge 5220, Supermicro MicroCloud



TOMORROW: 10 RU

- 256/ 512 Nodes in 10RU
- Single Socket @ 10-20W
- Shared IO Resources
- Integrated ToR Switch
- SeaMicro SM10000, HP Redstone

Opportunities from Hardware

Integration

- **Cores + memory + networking + I/O**
- Lower latency, better QoS
  - Multiple Priorities
  - B/W guarantees

Efficient Out-of Order Cores

- Break tradeoff between wimpy and brawny cores
- Energy efficiency at good performance (ARM-based processors are well suited here)

Virtualization Support

- Improve utilization without hurting performance

Highly Integrated Server on Chip

Efficient Low Latency Interconnect

Cloud Requirements →
Integrated, Right-Sized Compute. Memory. Network.

ARMv8 (Oban): Fully Backwards Compatible
New 64b ISA + Current 32b ISA

New: ARMv8

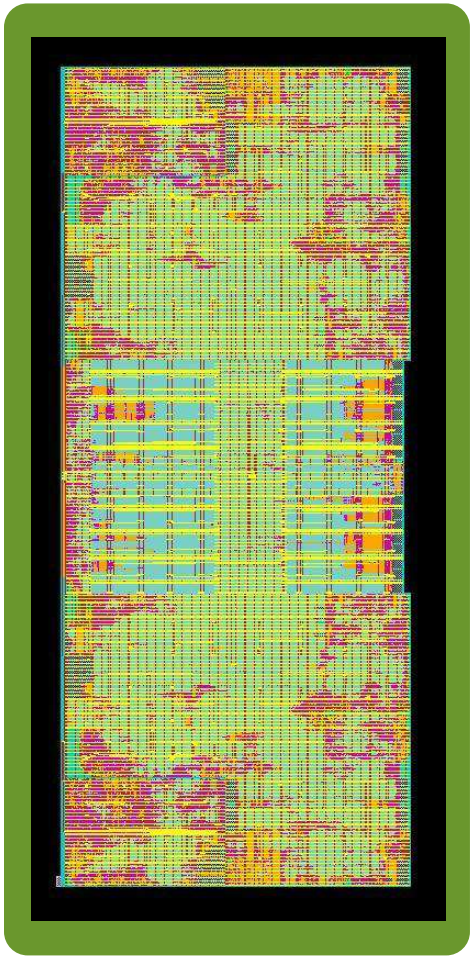
- 64b (General) and 128b (FP,SIMD) registers
- SP, PC no longer general purpose registers
- Uniform load/store addressing modes
- Larger data and instr. offset ranges
- Simplified load/store multiple instructions

- Reduced conditional instructions
- 32 128b FP/SIMD architecture registers
- No SIMD on general purpose registers
- New instructions for debug, TLB, barriers
- New Crypto acceleration instructions

ARMv8

- **New High Performance 64bit ISA + compatibility with existing 32bit ISA**
- **Full CPU, IO, Interrupt, Timer Virtualization**
- **Enhanced 128b SIMD operations**
- **High performance Floating-Point operations including FMADD**
- **Standard Performance Monitoring, Instr. Trace and Debug Architecture**

X-Gene™ CPU Design Goals



- **High-Performance Low-Power Microarchitecture**
  - Design point targets balance between performance, power, and size
  - Maximum “bang for the buck”
- **Low Power Microarchitecture Features**
  - Sophisticated branch prediction, Caches, Unified register renaming
  - Minimal instruction replay cases
  - Separate smaller schedulers per pipe
  - Full set of power management features
- ***Good* Single-Thread Performance, but also Efficiently Scalable to Many Cores**
  - Scalable CPU and interconnect architecture 2-128 cores
  - High bandwidth, low latency switch fabric > 1Tbps
  - High-performance distributed hardware cache coherency
- **Technology Portability**
  - Fully synthesizable RTL
  - Semi-custom cell-based design methodology
  - Small targeted set of custom macros (plus clock distribution cells/macros)

X-Gene™ Processor Module

Processor Module

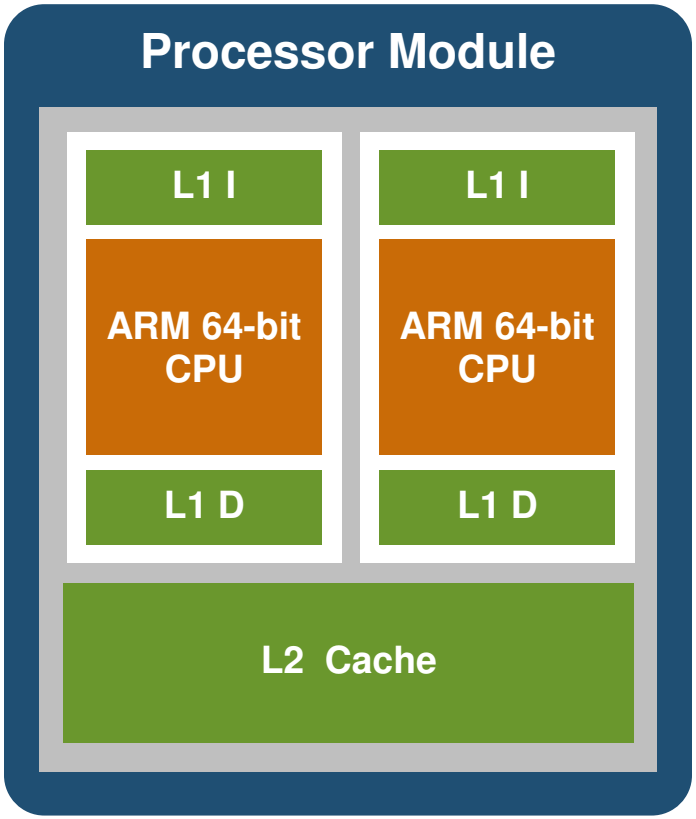
- 2 cores + shared L2 cache
- 4 wide out-of-order superscalar microarchitecture
- Integer, scalar, HP/SP/DP FPU and 128b SIMD engine
- Hardware virtualization support
- Hardware tablewalk and nested page tables
- Full set of static and dynamic power management features
  - Fine grain/macro clock gating, DVFS
  - C0, C1, C3, C4, C6 states

Cache Hierarchy

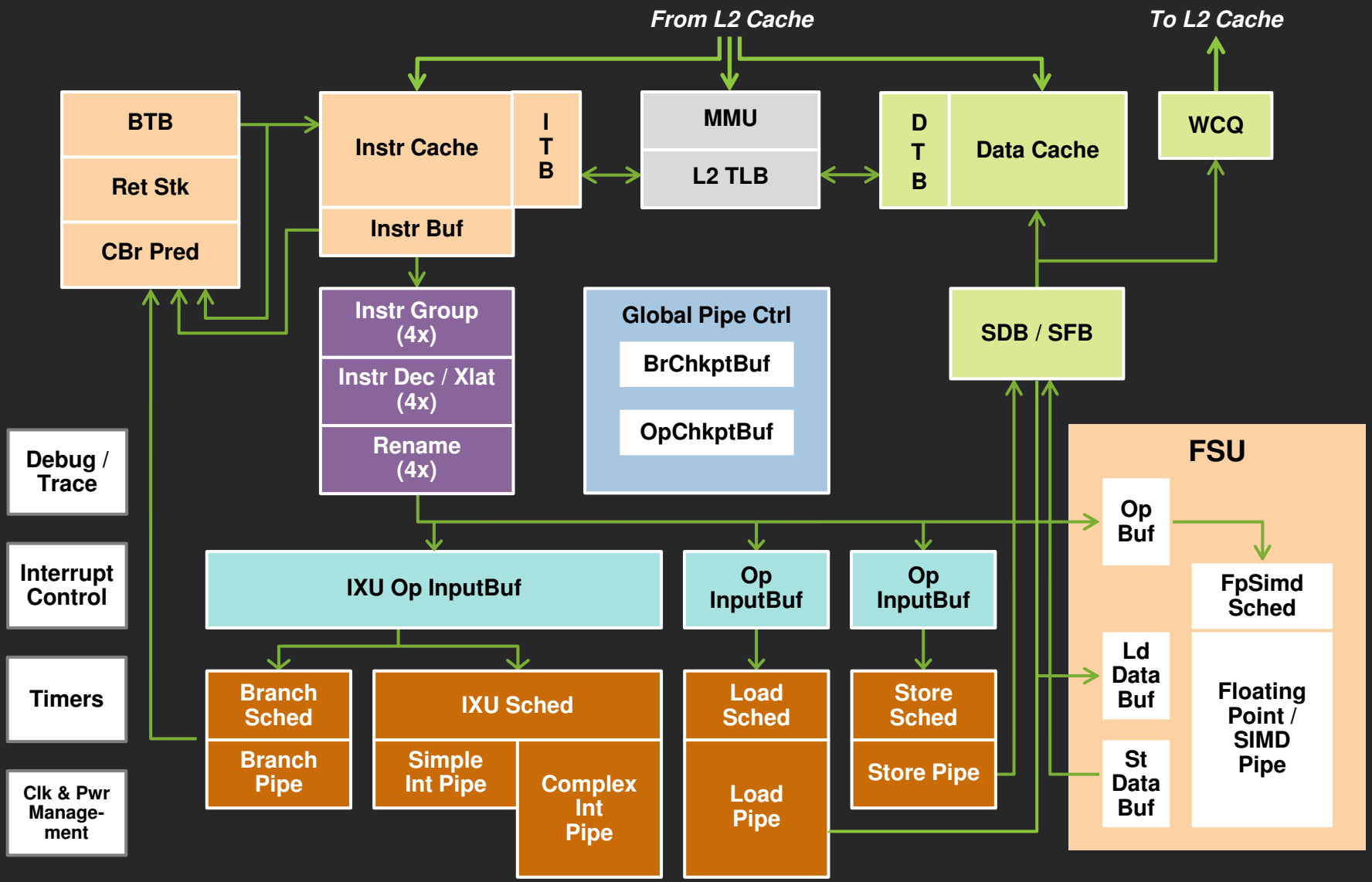
- Separate L1I and L1D caches
- Shared L2 cache among 2 CPUs
- Last-level globally shared L3 Cache
- Advanced hardware prefetch in L1 and L2
- L2 inclusive of L1 write-thru data caches

RAS

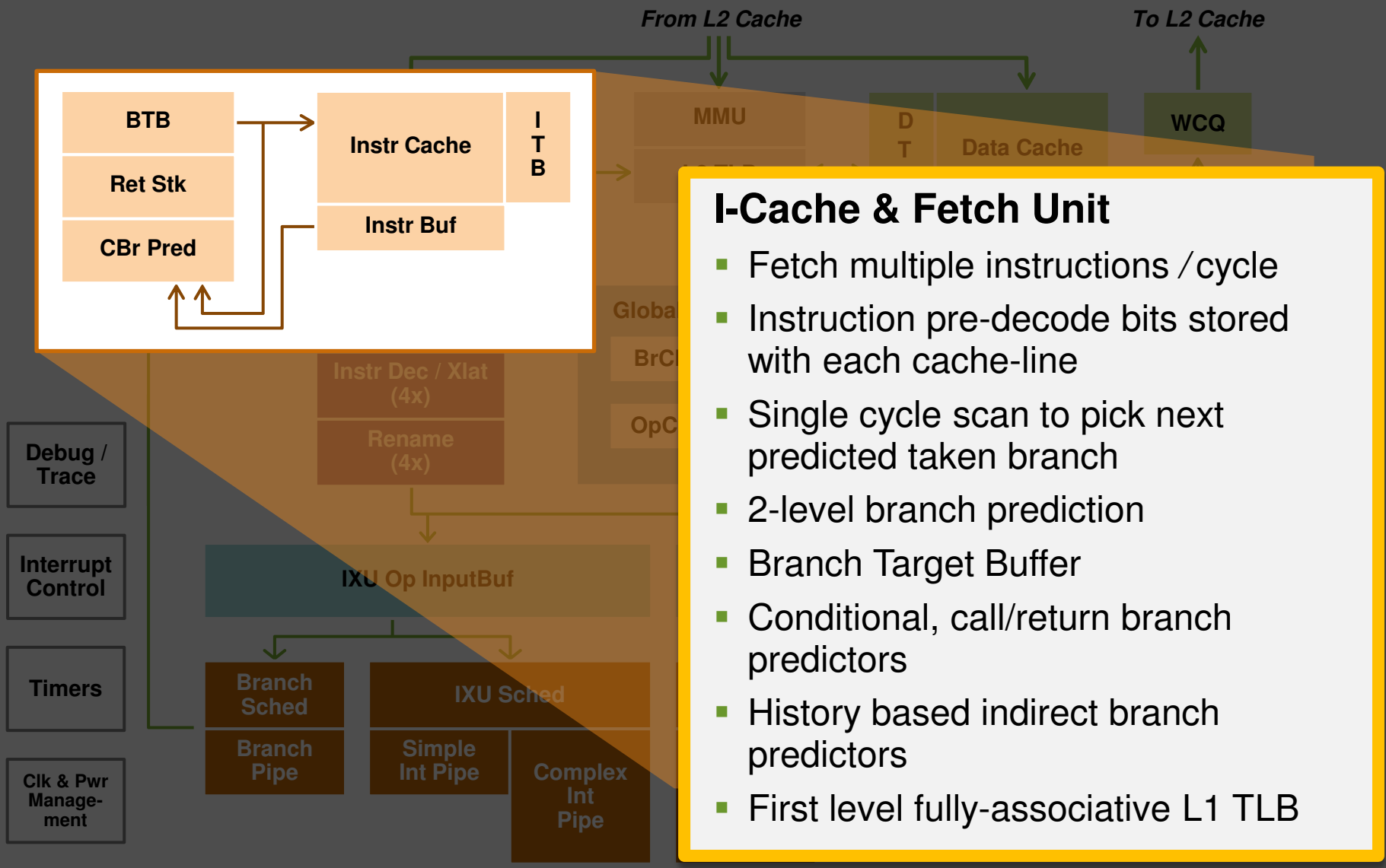
- ECC and Parity protection of all Caches,Tags,TLBs
- Data poisoning and error isolation



X-Gene™ CPU Block Diagram



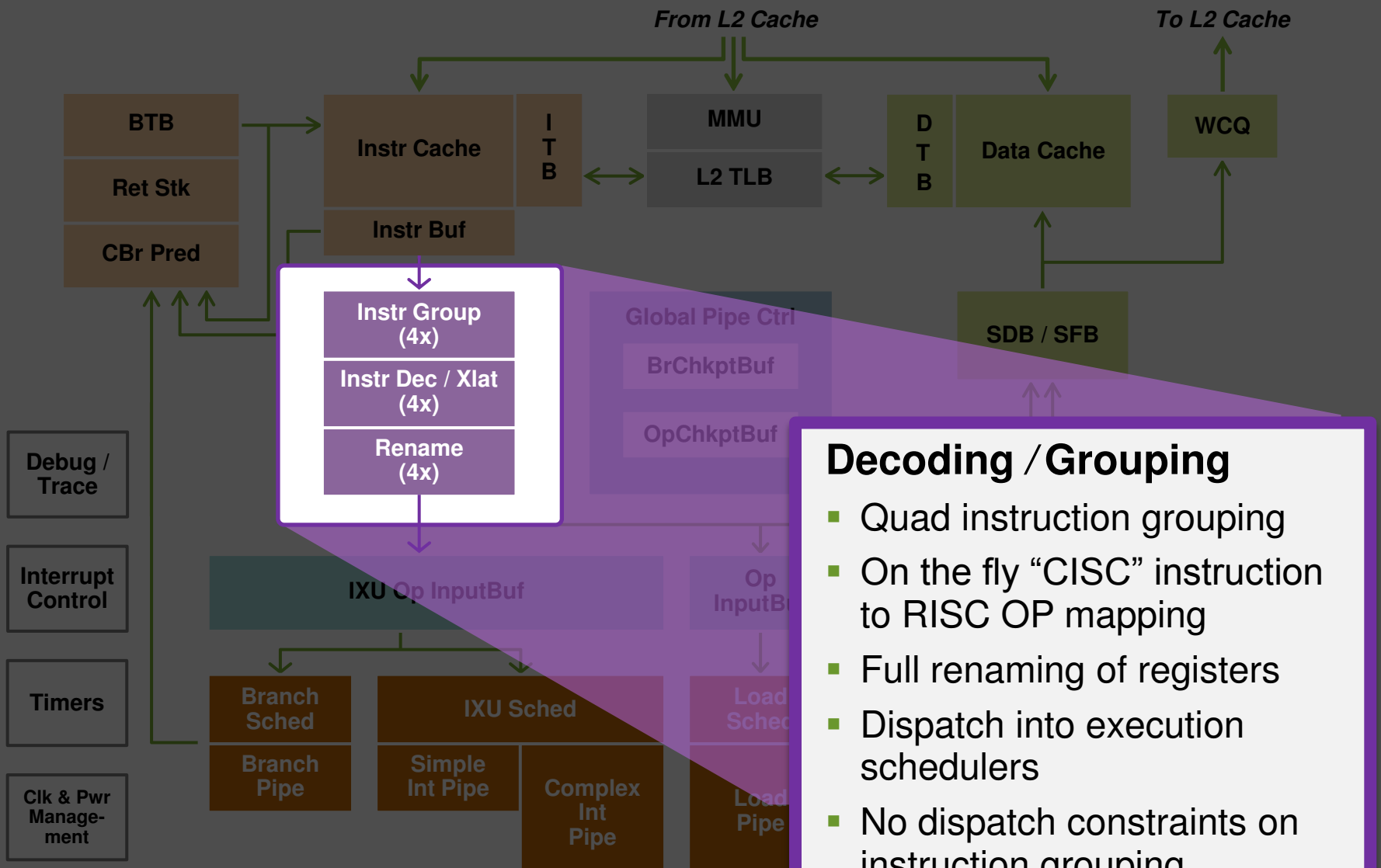
X-Gene™ Instruction Fetch



I-Cache & Fetch Unit

- Fetch multiple instructions /cycle
- Instruction pre-decode bits stored with each cache-line
- Single cycle scan to pick next predicted taken branch
- 2-level branch prediction
- Branch Target Buffer
- Conditional, call/return branch predictors
- History based indirect branch predictors
- First level fully-associative L1 TLB

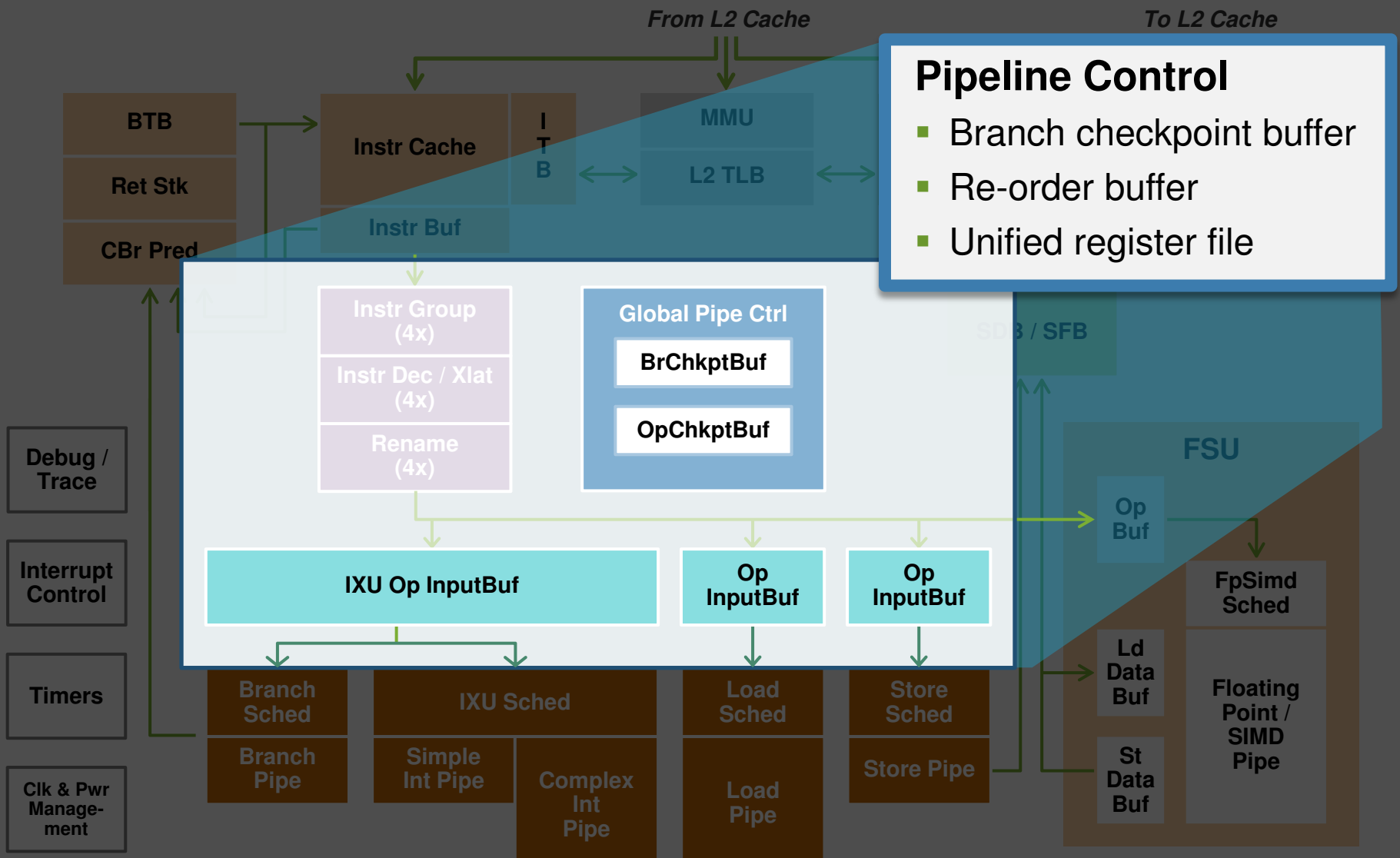
X-Gene™ Instructions Decoding/Grouping



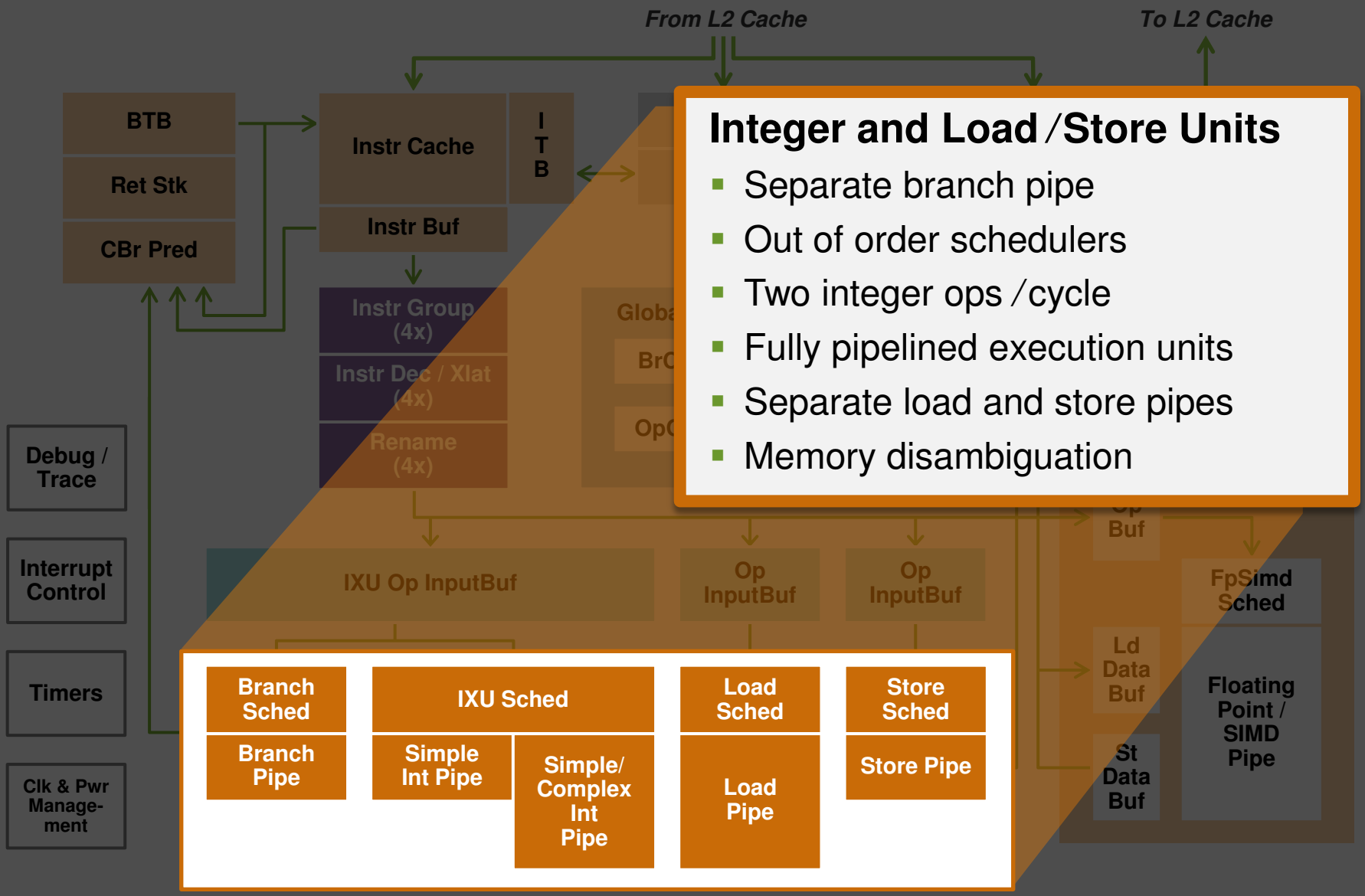
Decoding / Grouping

- Quad instruction grouping
- On the fly "CISC" instruction to RISC OP mapping
- Full renaming of registers
- Dispatch into execution schedulers
- No dispatch constraints on instruction grouping

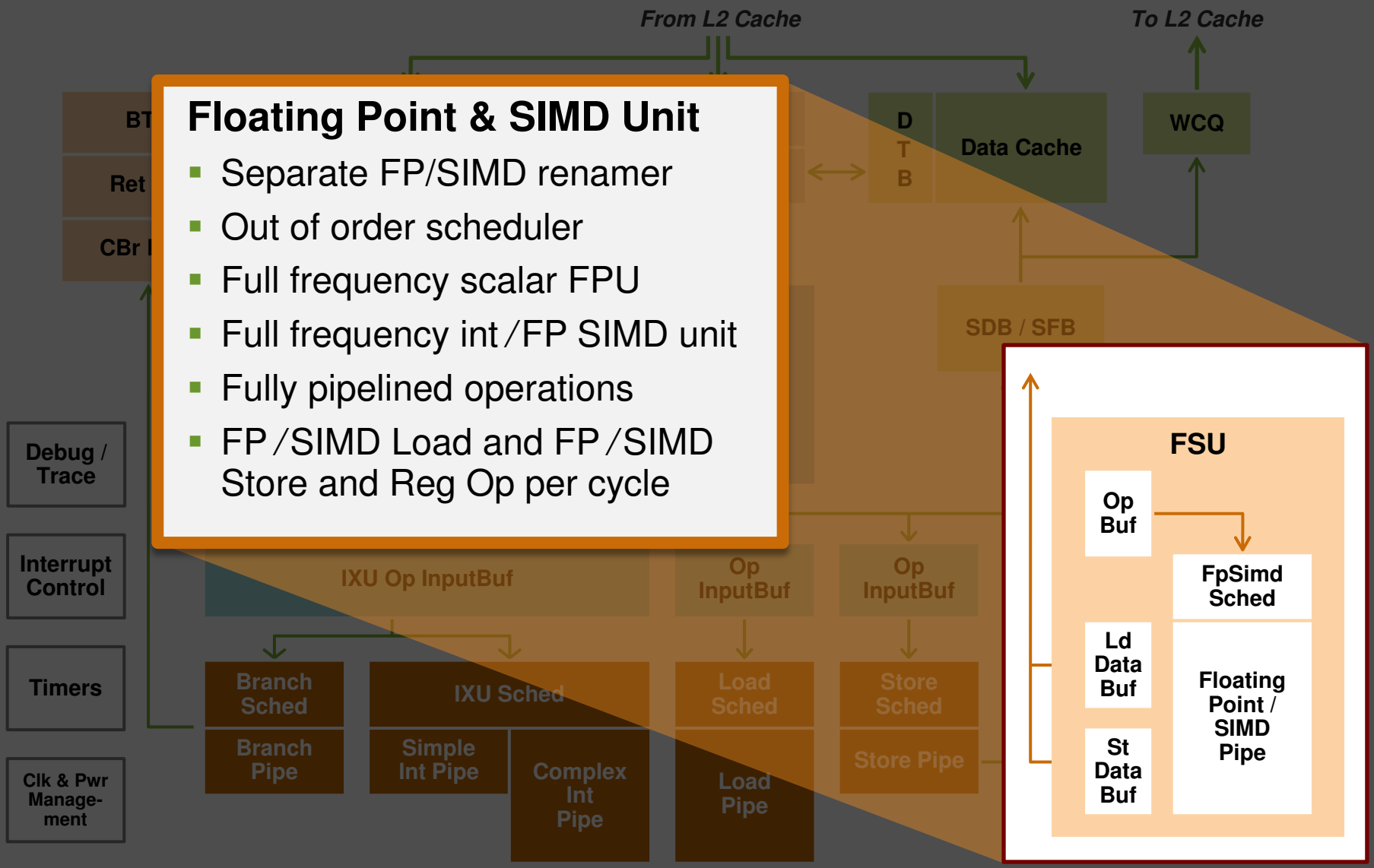
X-Gene™ Reorder Buffer, Dispatch and Control



X-Gene™ Integer, Branch, Load and Store Units



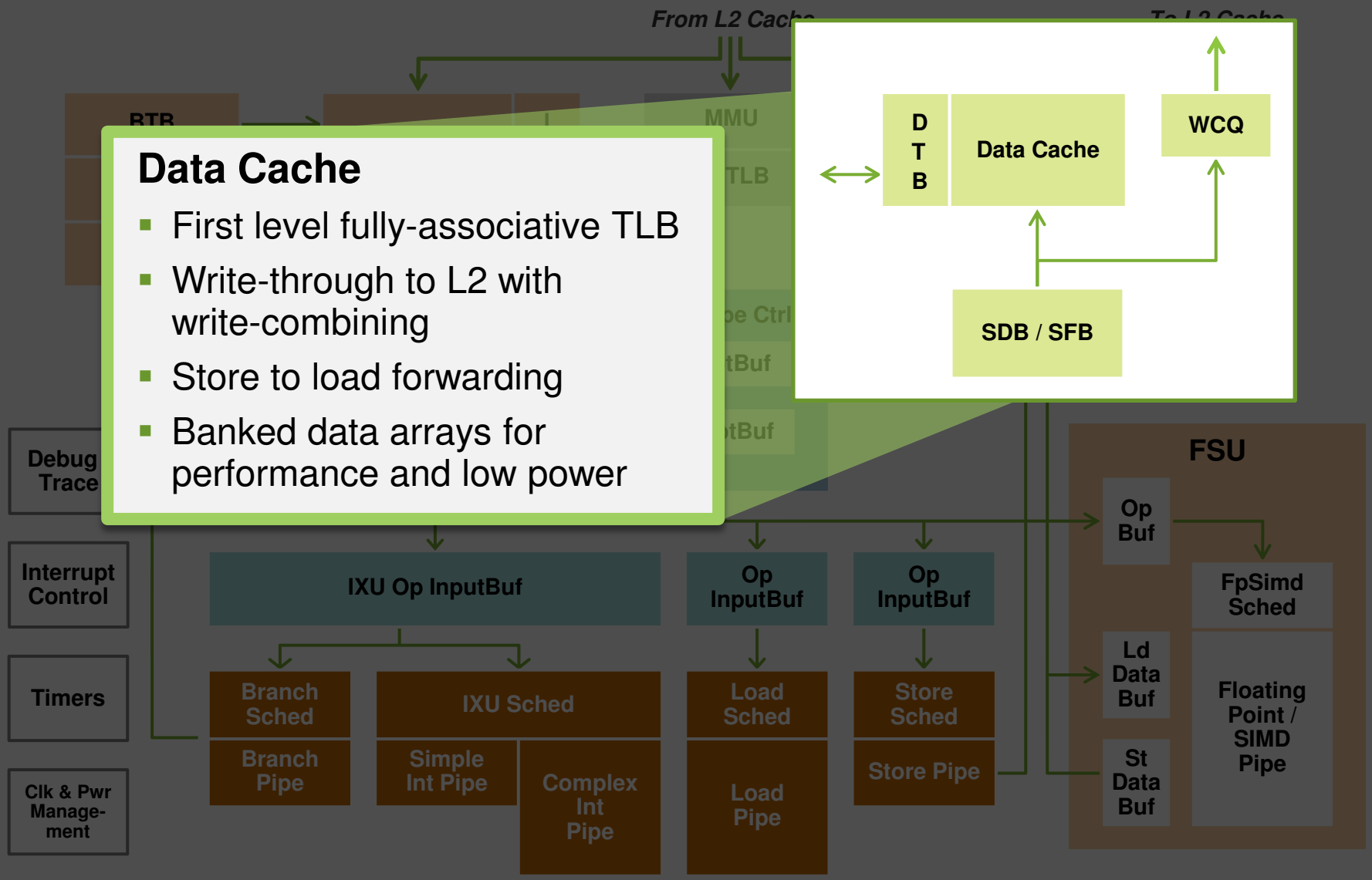
X-Gene™ FPU/SIMD



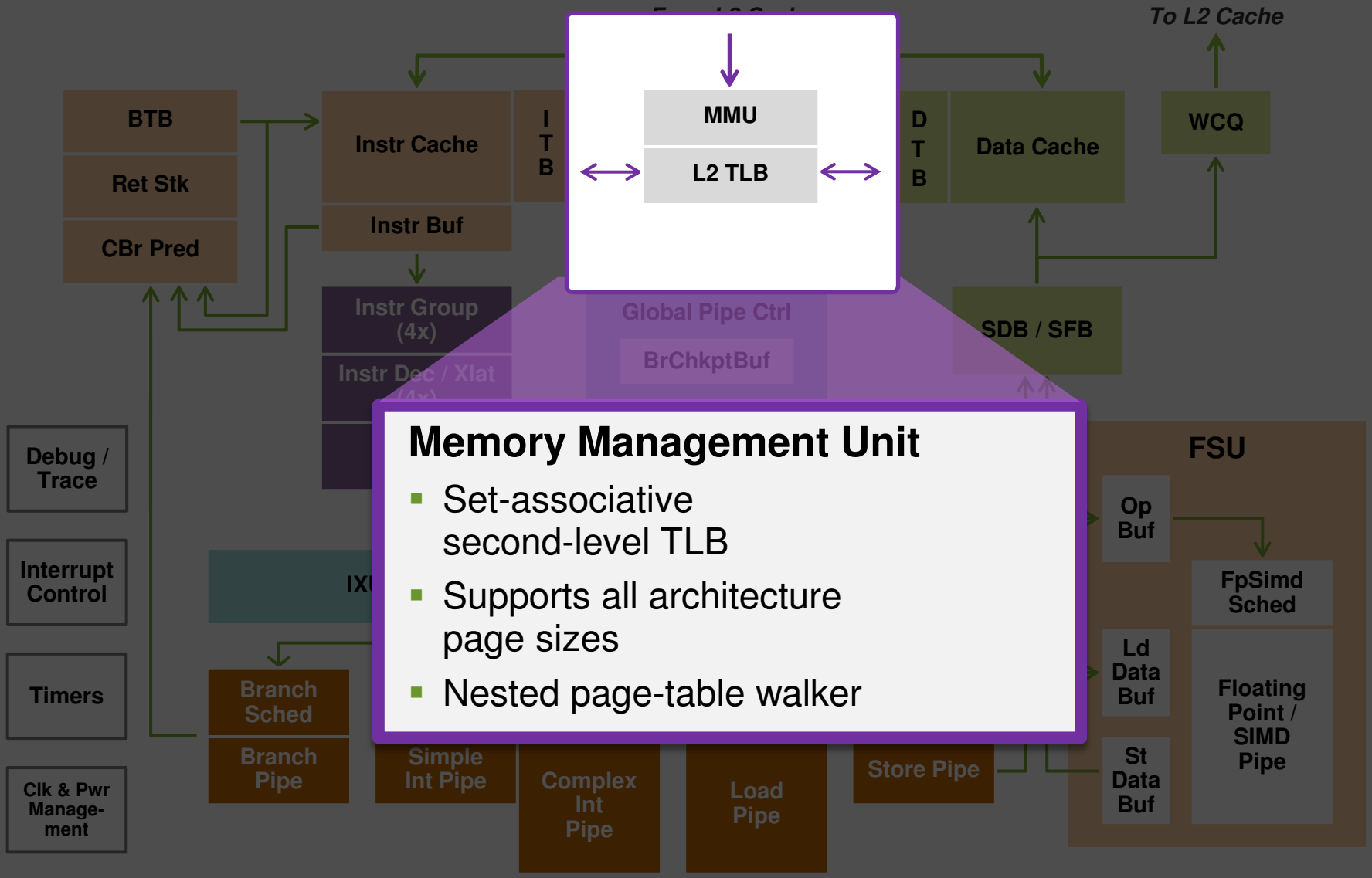
Floating Point & SIMD Unit

- Separate FP/SIMD renamer
- Out of order scheduler
- Full frequency scalar FPU
- Full frequency int/FP SIMD unit
- Fully pipelined operations
- FP/SIMD Load and FP/SIMD Store and Reg Op per cycle

X-Gene™ Data Cache



X-Gene™ Memory Management



Memory Management Unit

- Set-associative second-level TLB
- Supports all architecture page sizes
- Nested page-table walker

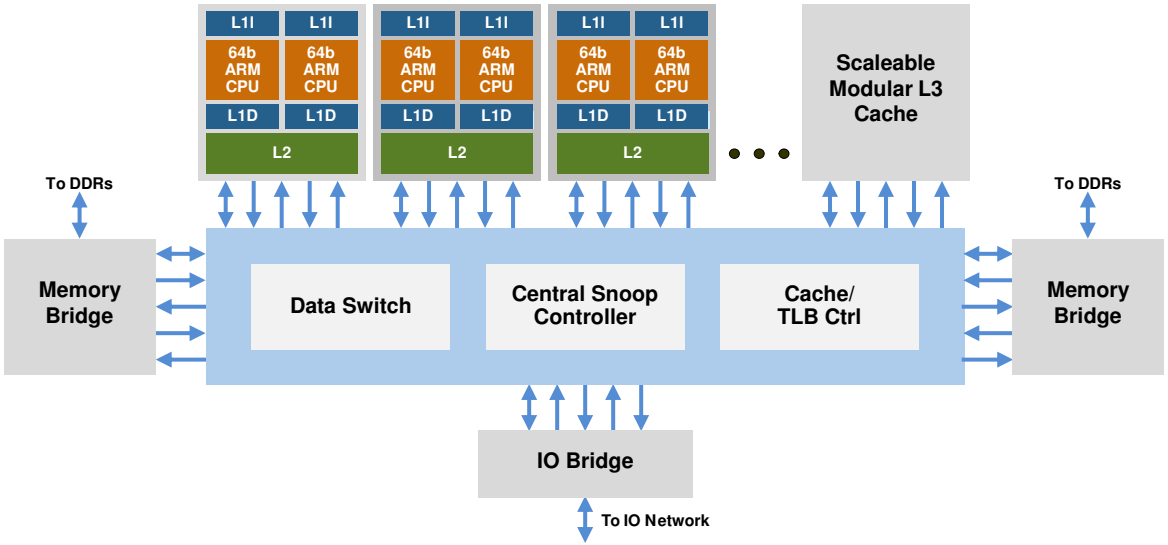
X-Gene™ – CPU Memory Subsystem

High-performance Symmetric Multi-core Design

- Modular architecture
- Three level cache hierarchy
- Globally shared L3 Cache

Coherent Network

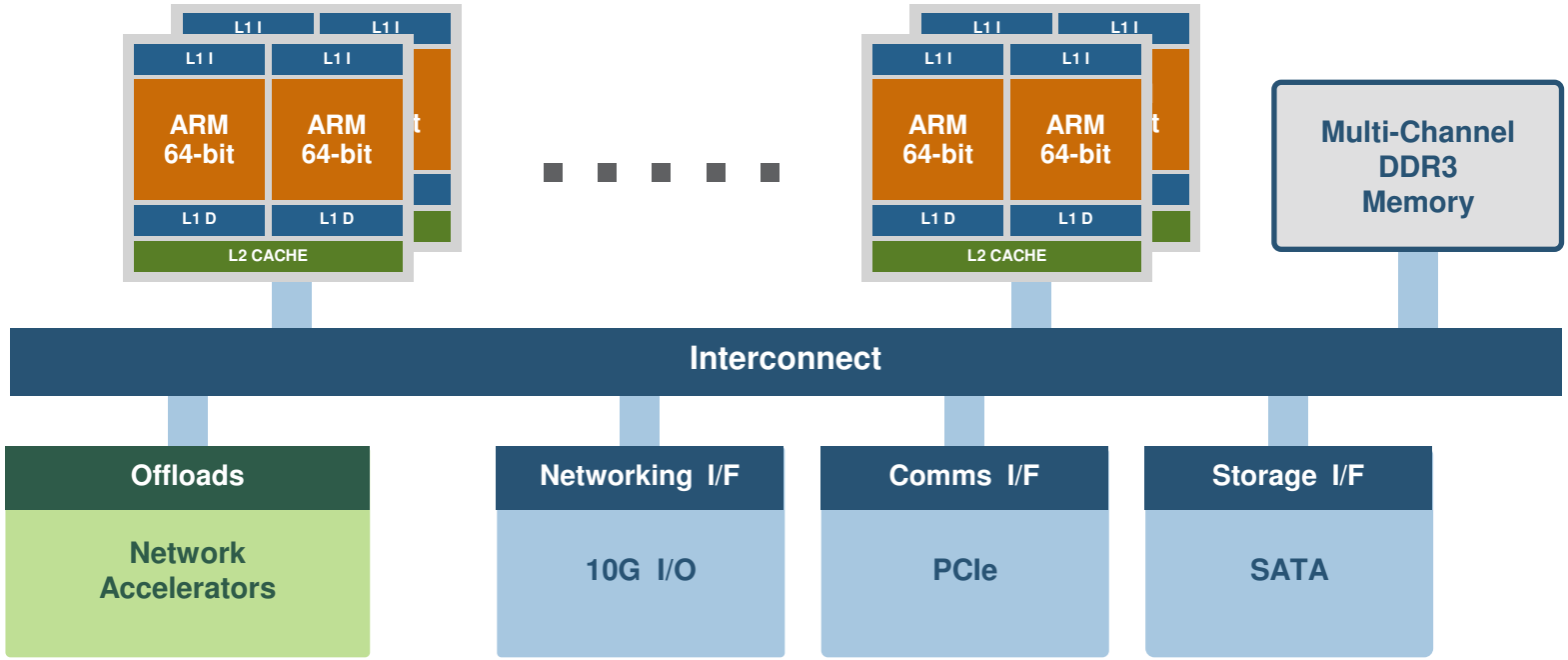
- Runs at full CPU frequency
- <15ns latency, ~200GB/s B/W
- Over 400 transactions in flight
- Central snoop controller and ordering point
- Decoupled frequency and power domains
- Support global cache and TLB inv operations



Bridges

- Memory Bridges to DRAM interfaces
- IO Bridge for SOC connectivity

X-Gene™ Server on Chip



64bit ARM Server Class CPU → Multi-core for Distributed Computing

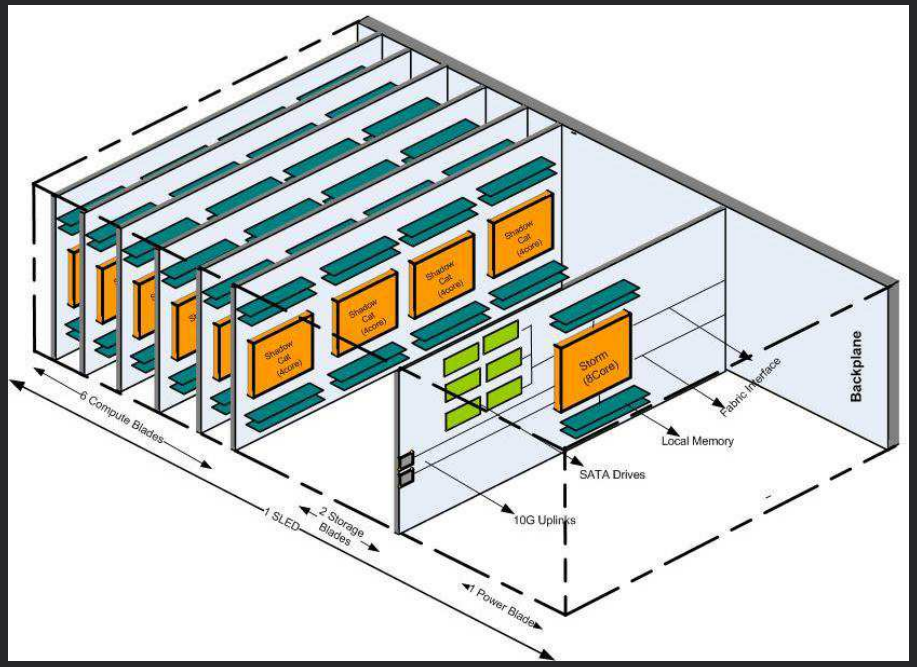
Increased Memory Capacity and 10G I/O Integration

Integrated Peripherals and L2 Switching

Workload Specific Acceleration

Available: 2H'12

Right Sizing + Connected On-Chip Fabric



Customizable Blade Design

- Configurable swappable blades within 1 sled
- Networking/ Compute/ Storage shared over common bed of CPUs → Saves Power & Cost

Overall System Optimization

- Integrated NIC and IO chipset
- Load Balancing Across multiple blades to Optimize System Balance
- Shared Resources for System Management, Power and Cooling

System Capabilities

- 1000s of CPU cores in 10RU
- 100s of CPU cores per blade
- 100s of Gbps of network bandwidth
- 10s of Tbps of interconnect fabric bandwidth

X-Gene™