



Medfield Smartphone SOC Intel® Atom™ Z2460 Processor

Rumi Zahir
Intel Corporation



Outline

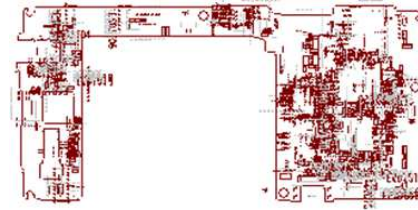
- Low power platform progression
- Medfield platform for the Smartphone form-factor
 - Constraints, Ingredients, Package
- Penwell SOC
 - Block Diagram
 - Intel Atom™ CPU power management
 - SOC power management
 - Power management software architecture
- Medfield reference platform
- Smartphone roadmap

Low Power Platform Progression

Moorestown (45nm)



Medfield (32nm)

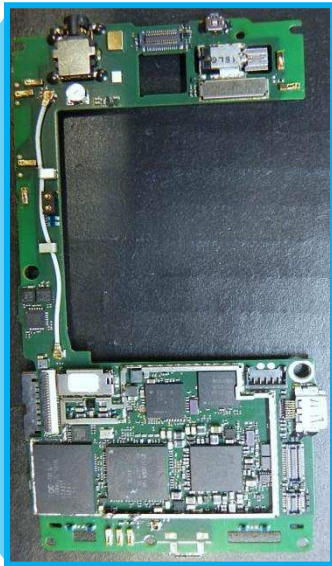


Board size	5,000mm ²	4,150mm ²	(↓ 17%)
Standby power	21mW	14mW	(↓ 33%)
Browsing power	1.2W	0.85W	(↓ 29%)
Video	+ 720p encode	+ 1080p encode	
Camera	5 mega-pixel	up to 16 mega-pixel	
Graphics	800 MPPS	2,000 MPPS	(↑ 250%)

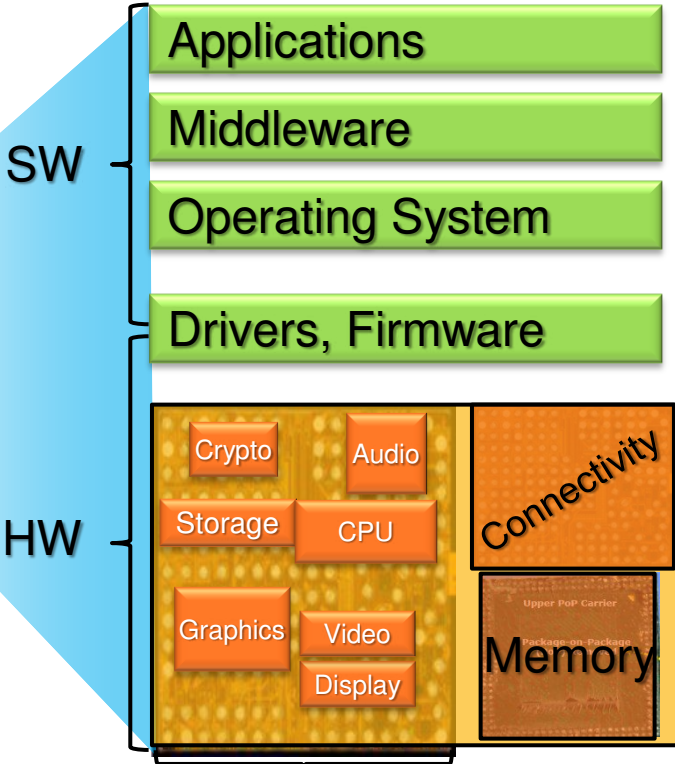
Smartphone through the Systems Lens



Intel Form Factor Reference Design



Board Design

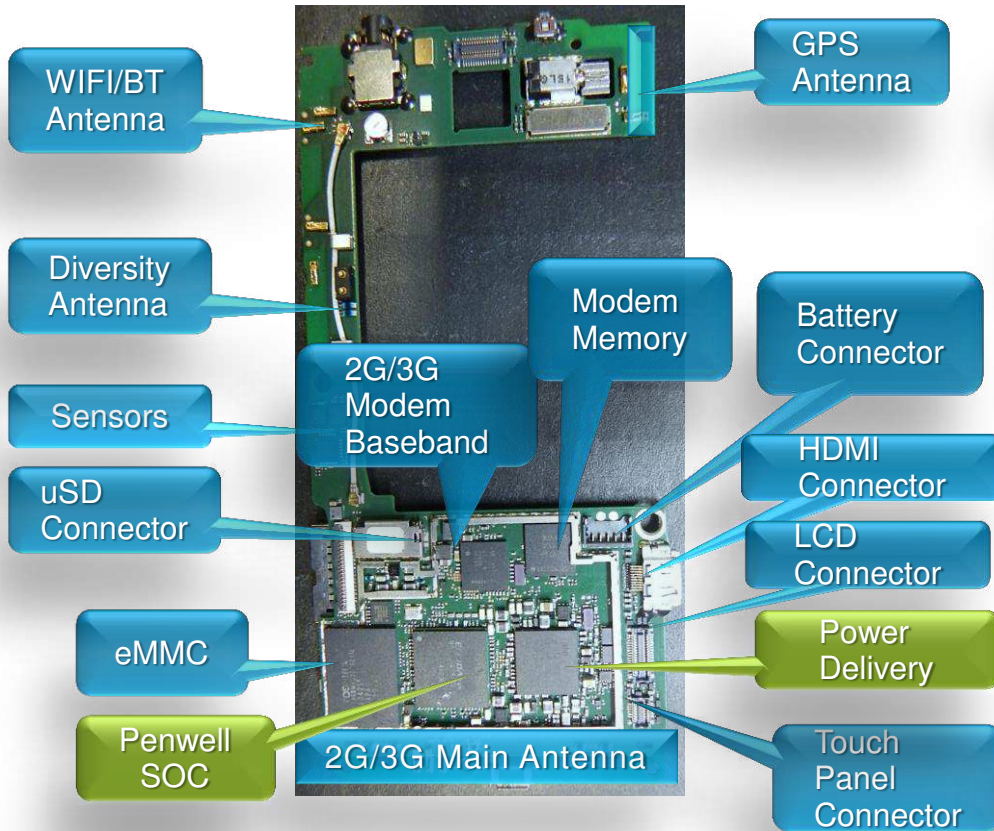


System-on-A-Chip Integration

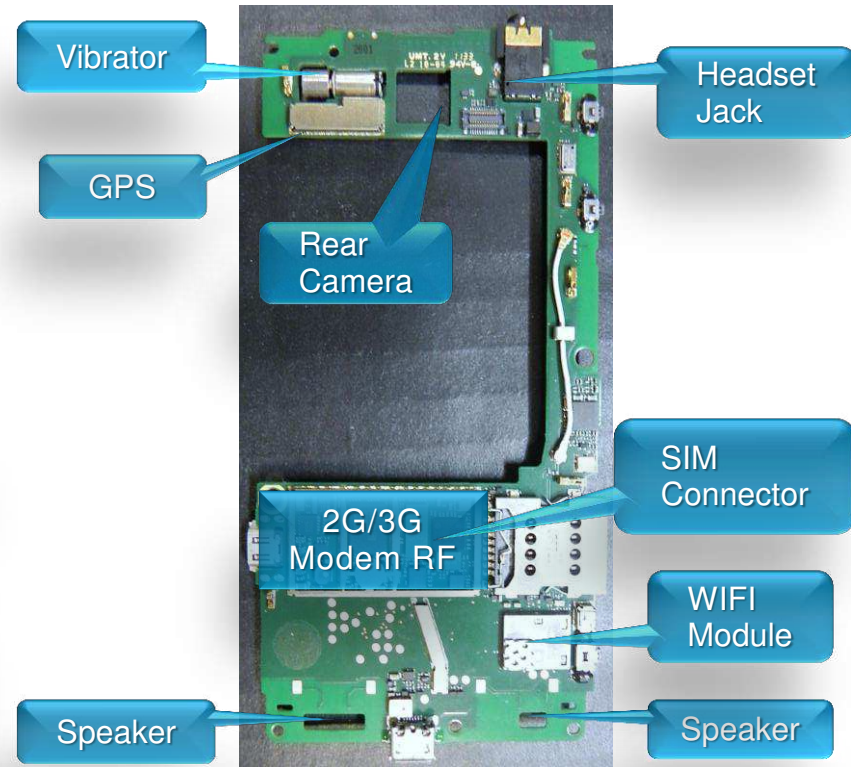
Design to meet Smartphone cost/power/performance requirements



Medfield System Ingredients

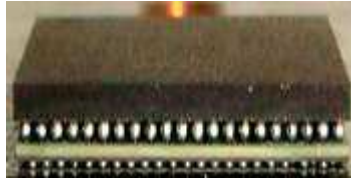
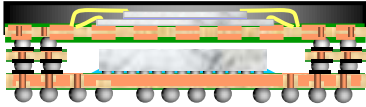


Front



Rear

Penwell SoC Package Size



Package-on-Package (POP)

- 12 x 12 mm PoP FCMB4 – 32nm
- Non PoP SoC < 0.8 mm
- PoP z height < 1.4mm
- OEM/ODM can solder up to 2 GB of LPDDR2 memory on top of SOC

- **Memory Peak Bandwidth**

- ✓ 6.4GB/s @ 800MT/s
- ✓ Channels and ranks

- **Dual 32 bit channels**

- ✓ Supports 1 or 2 ranks per channel

- **Memory Size and Density**

- ✓ Supports total memory size of 128MB, 256MB, 512MB and 1GB per channel
- ✓ Supports 1Gb, 2Gb and 4Gb chip

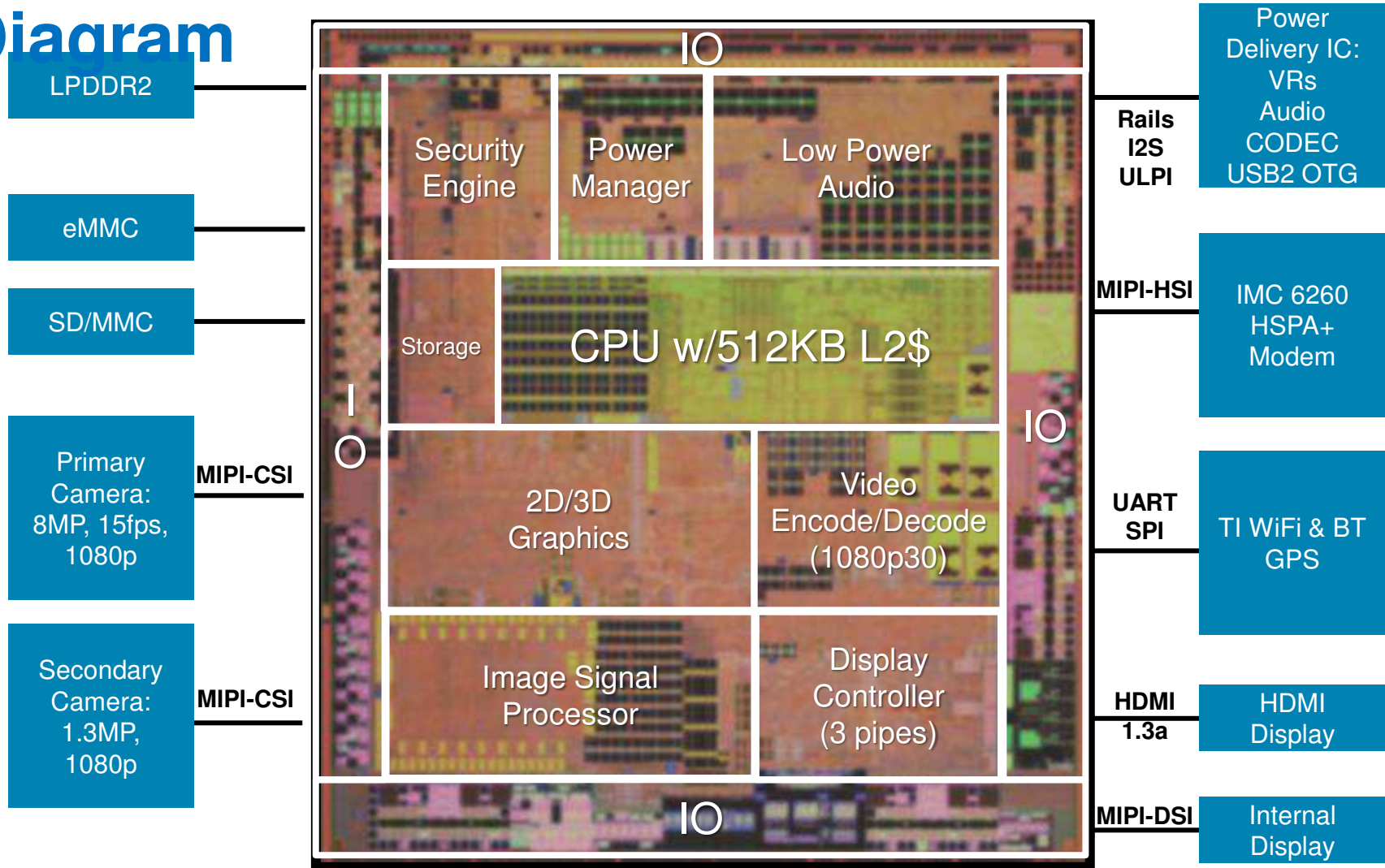
densities

- **Other Features**

- ✓ Aggressive power management to reduce power consumption
- ✓ Proactive page closing policies to close unused pages
- ✓ Supports different physical mappings of bank addresses to optimize for performance

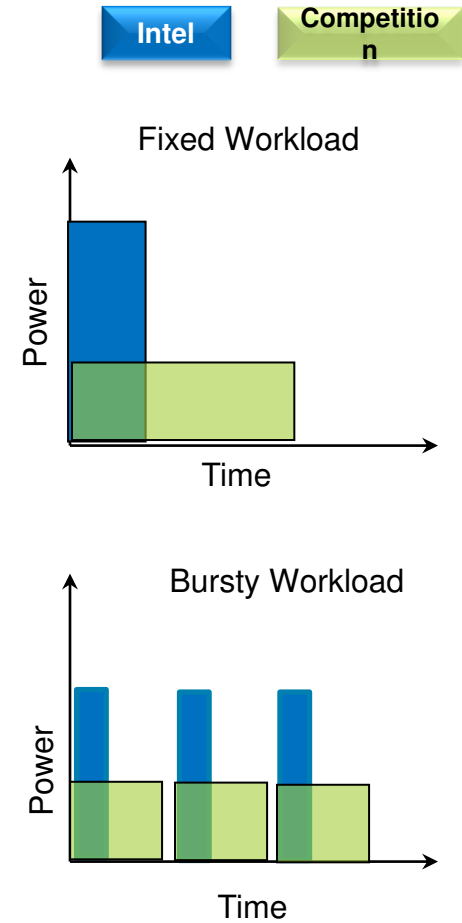
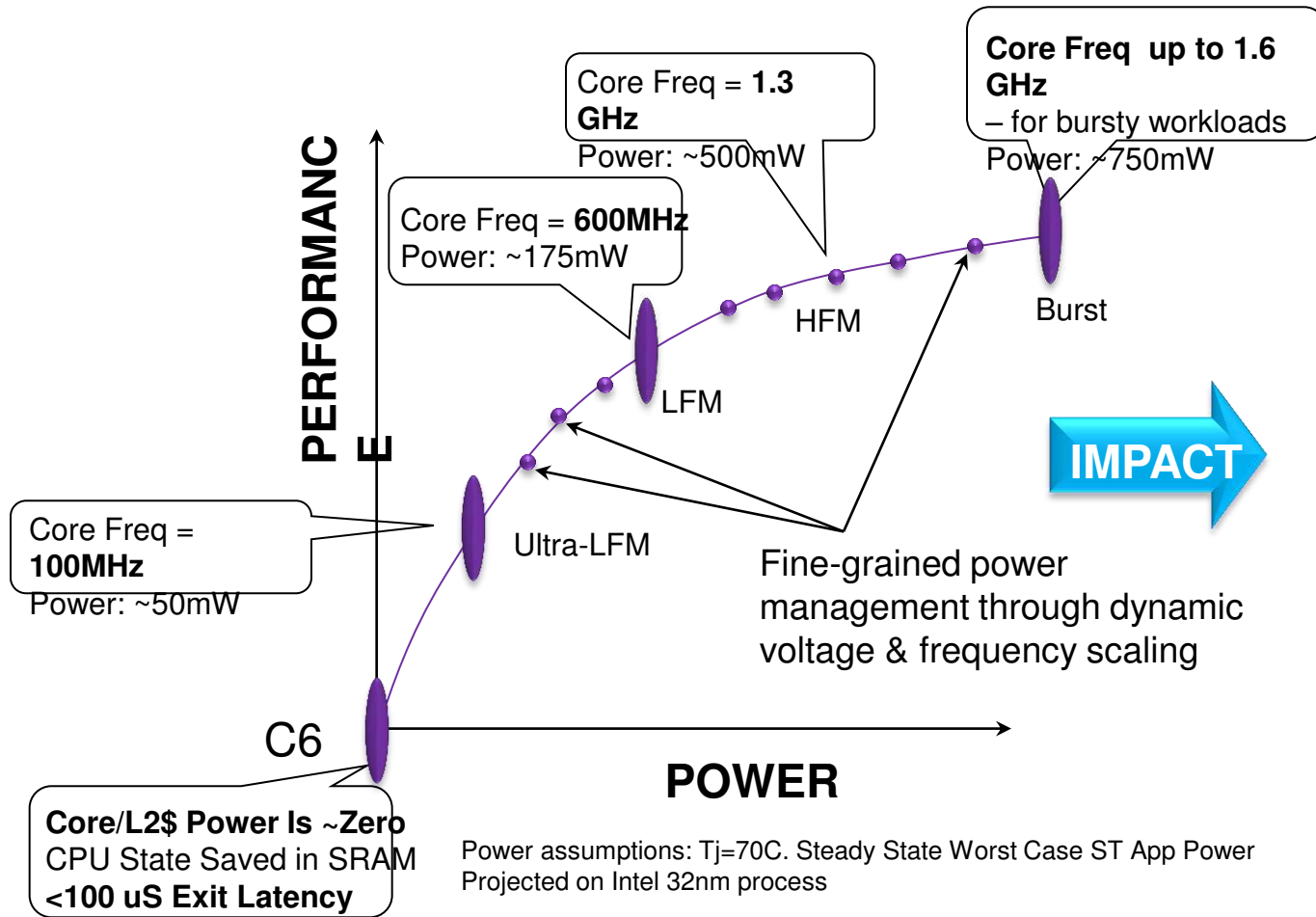
Medfield with Penwell SOC Block Diagram

Diagram



Penwell SOC (Intel Hi-K 32nm Process Technology)

Penwell CPU Dynamic Range































Wide Dynamic Range & Fast Exit Latencies = Big Energy Savings

Browser Results Summary

P0	600 MHz	900 MHz	1,500 MHz
Frequency	1x	1.5x	2.5x
Performance	1x	1.41x	2.24x
Power	1x	1.29x	1.81x
Energy	1x	0.92x	0.81x

“Race to Idle” at higher frequency uses more power, but is lower energy

Power C-States

	C0 HFM	C0 LFM	C1/C2	C4	C6
Core voltage					
Core clock			OFF	OFF	OFF
PLL				OFF	OFF
L1 caches				 flushed	 off
L2 cache				 Partial flush	 off
Wakeup time	active	active			
Power					

The OS Is Responsible For Identifying When The Processor Needs To Be In A Certain C State And Requests The Processor To Enter That State

New Platform Level: “S” Ultra Low Power States

S0i1

- Used during idle (e.g. home screen, web browsing)
- Ultra Low Power: mW
- Entry-Exit Latency: μ s

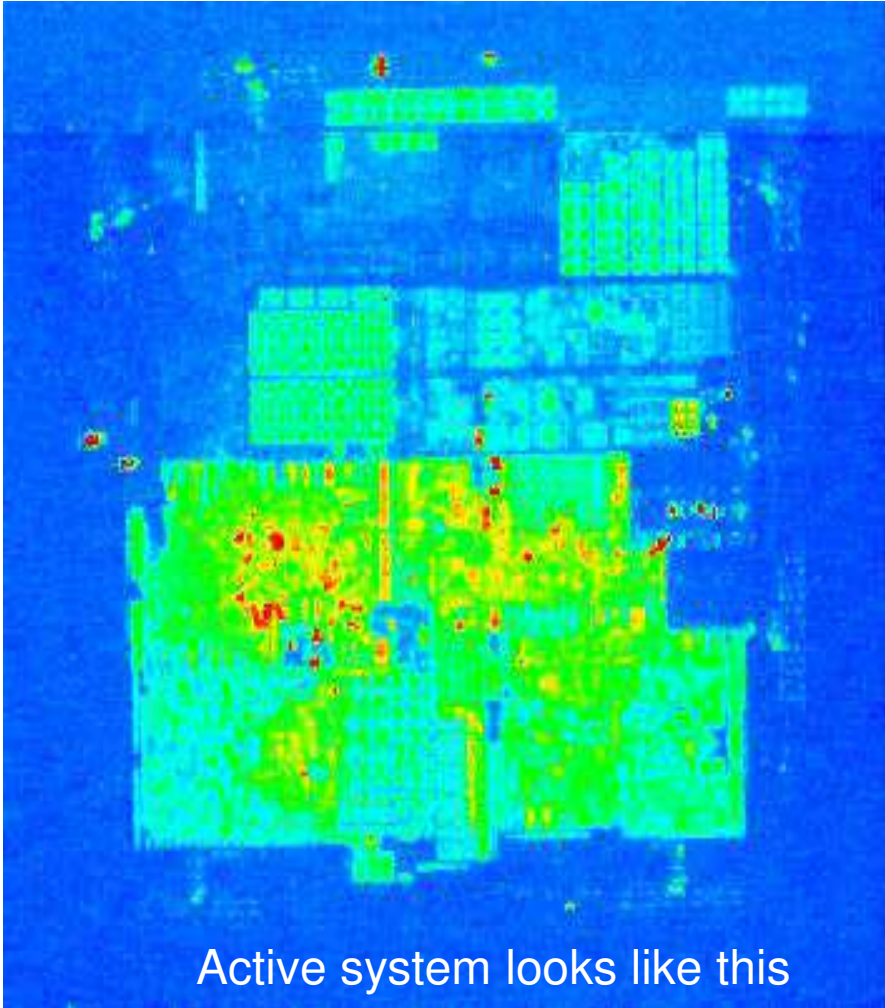
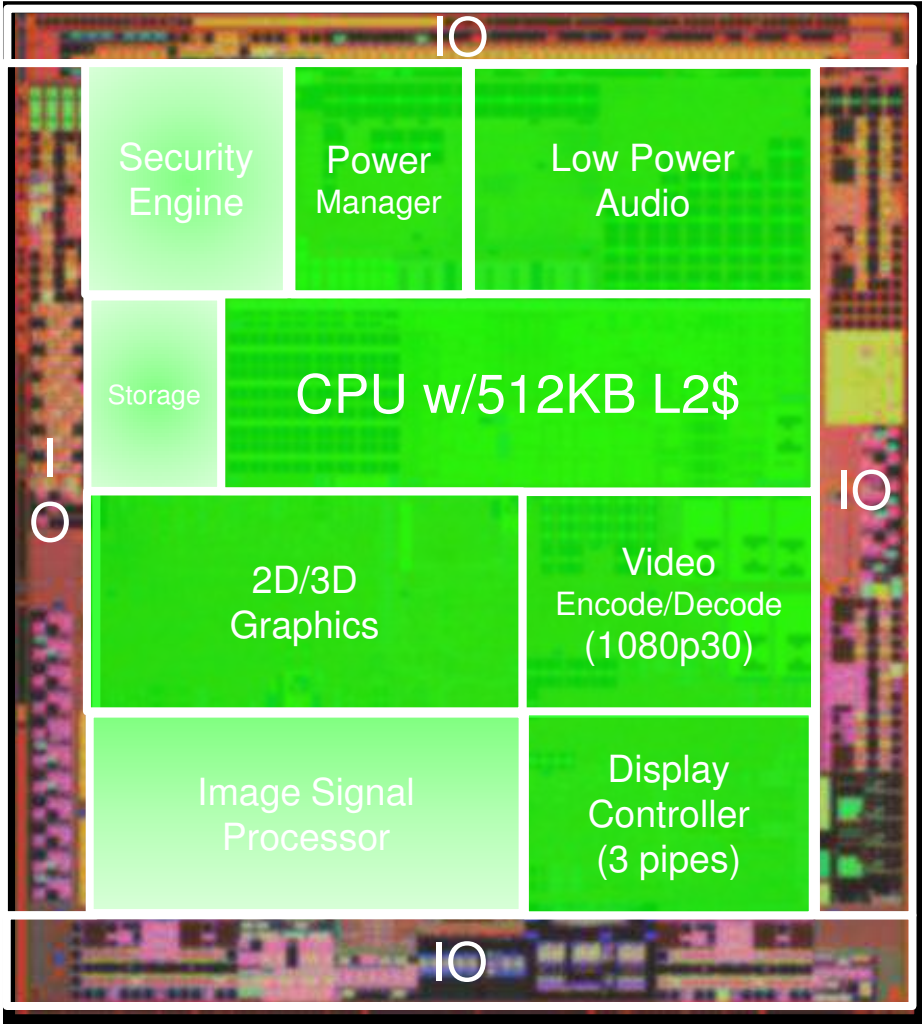
S0i3 / S3

- Used when NOT interacting with the device (e.g. standby mode)
- SoC power: μ W
- Entry-Exit Latency: ms

Platform Islands	S0: C0-C6	S0i1	S0i3
CPU	C-state dependent	C6	OFF
LP DDR2	ON/SR	SR	SR
Power Manager	ON	ON	ON
Graphics	ON/Power-Gated	Power-Gated	OFF
Video Decode			
Video Encode			
Display Controller			
Image Signal Processor			
Display	ON	ON	

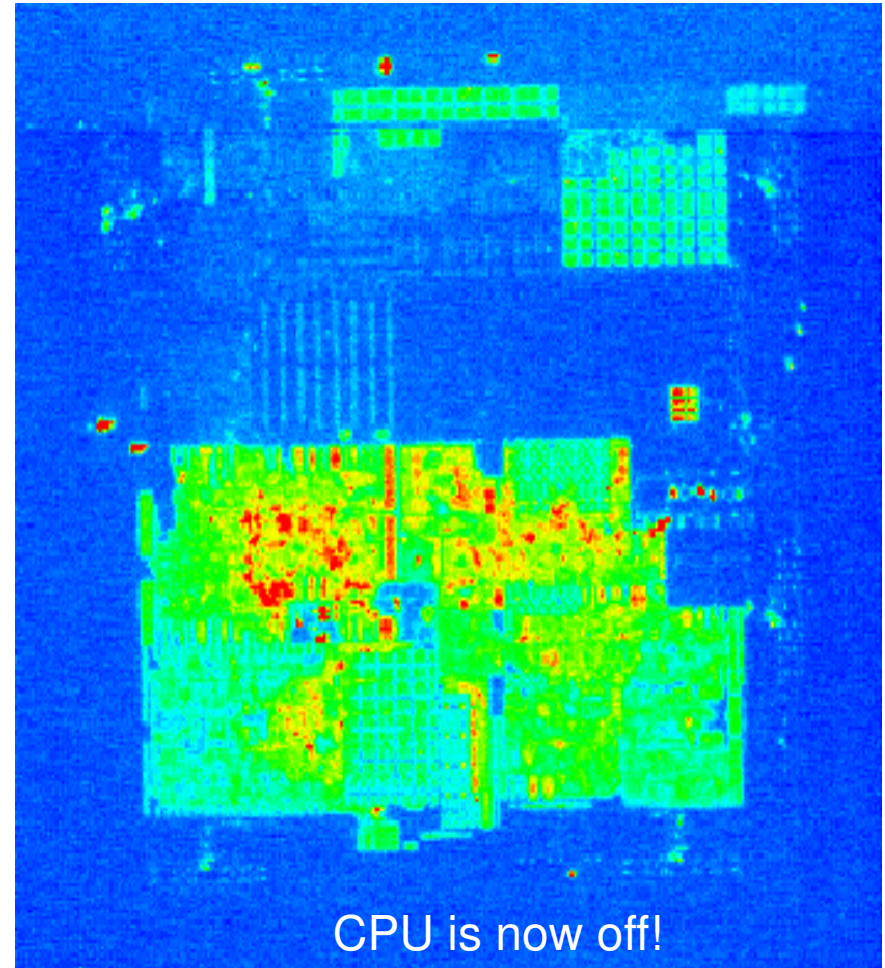
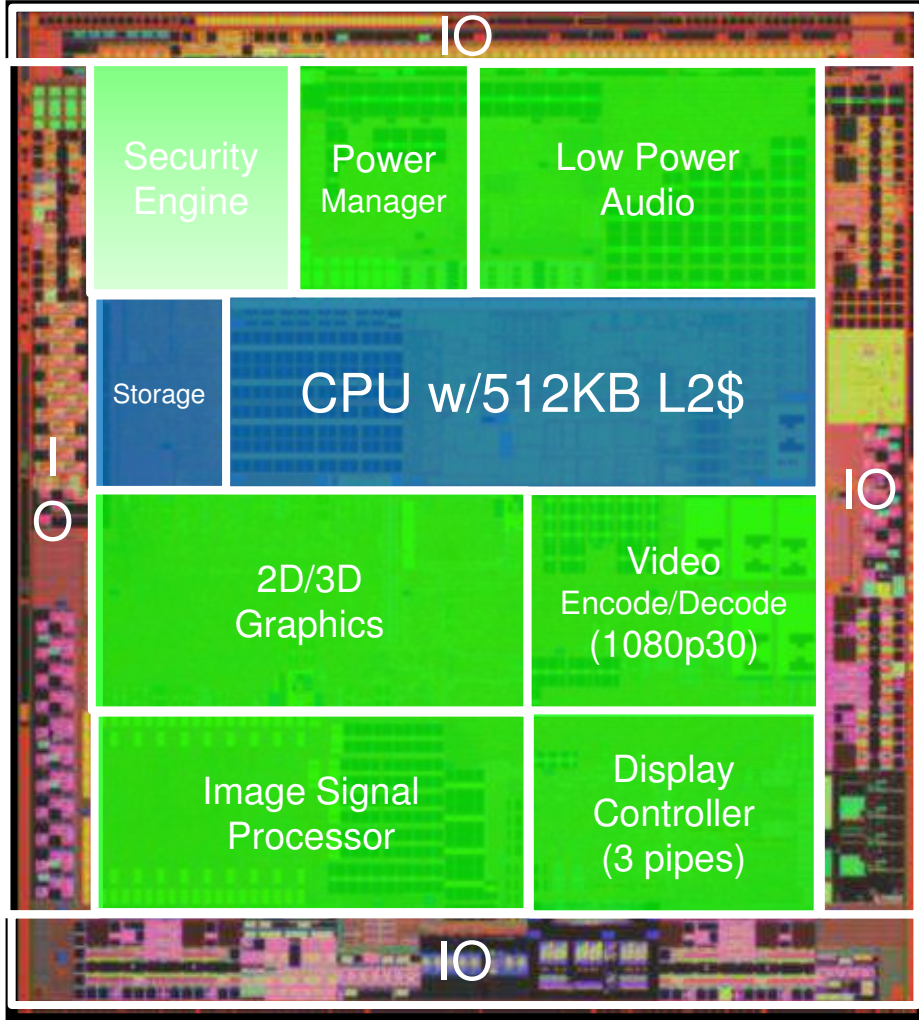
Achieves Ultra Low Power States with Best-in-Class Latency

CPU Active

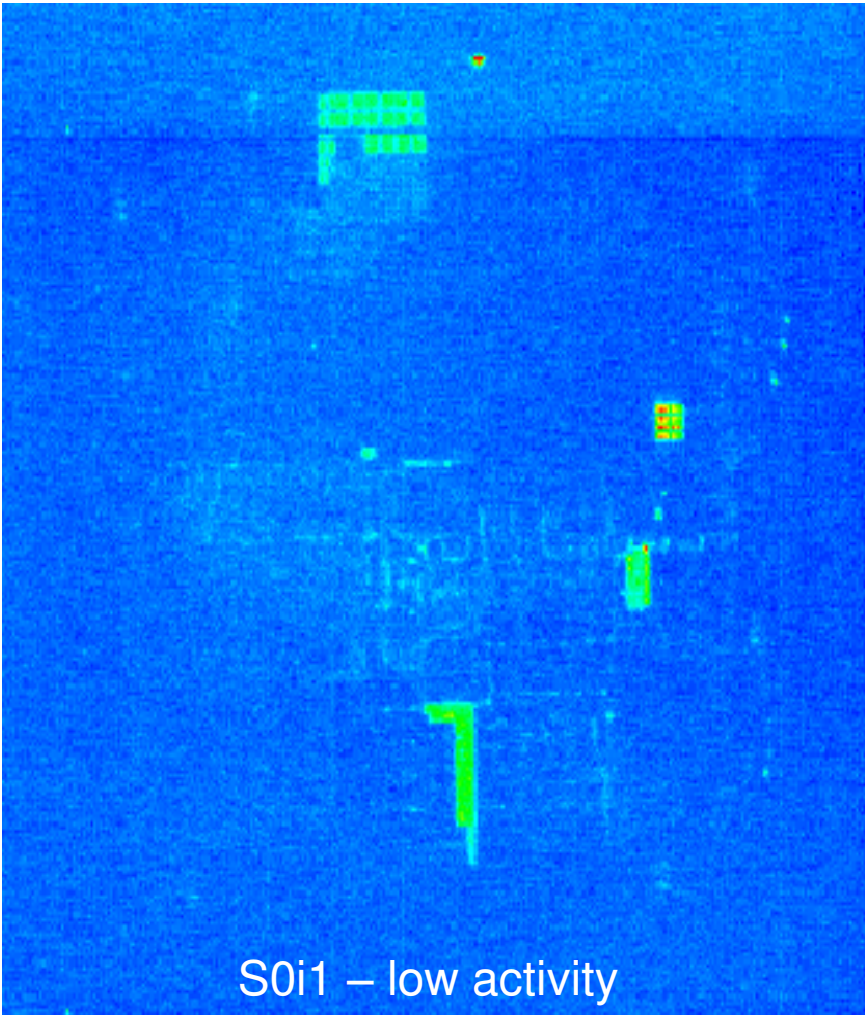
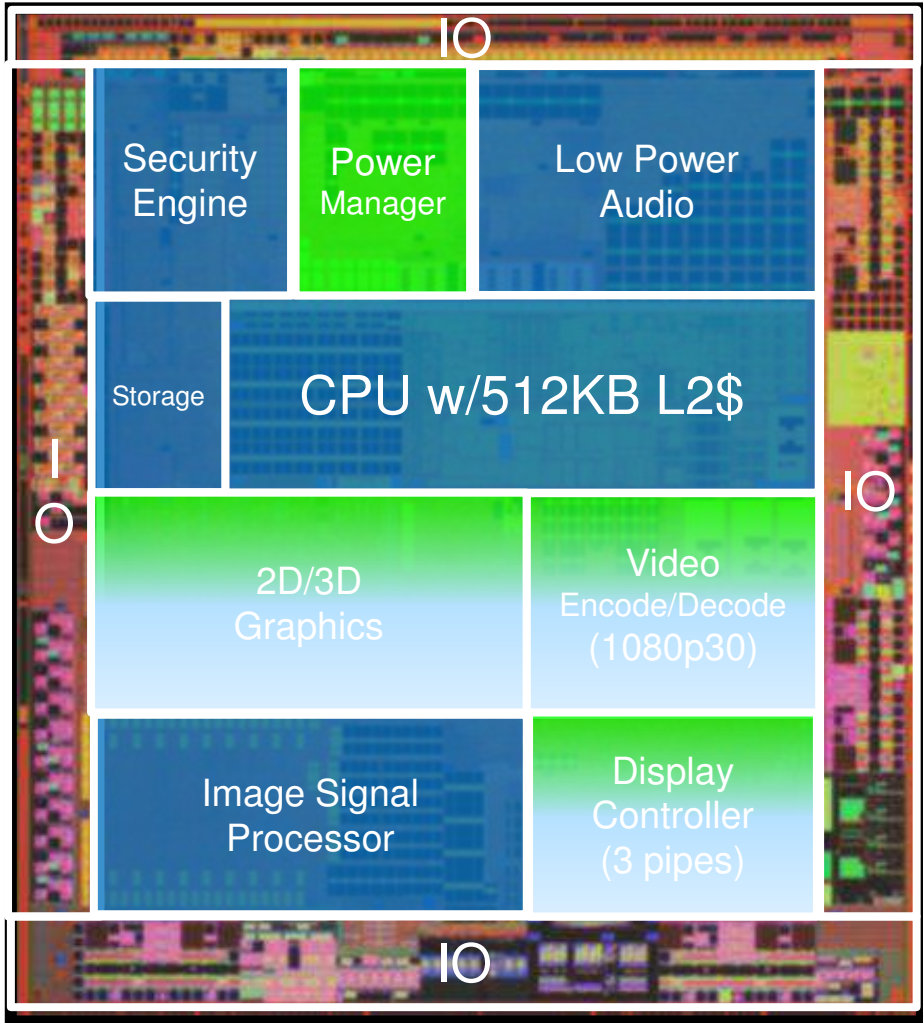


Active system looks like this

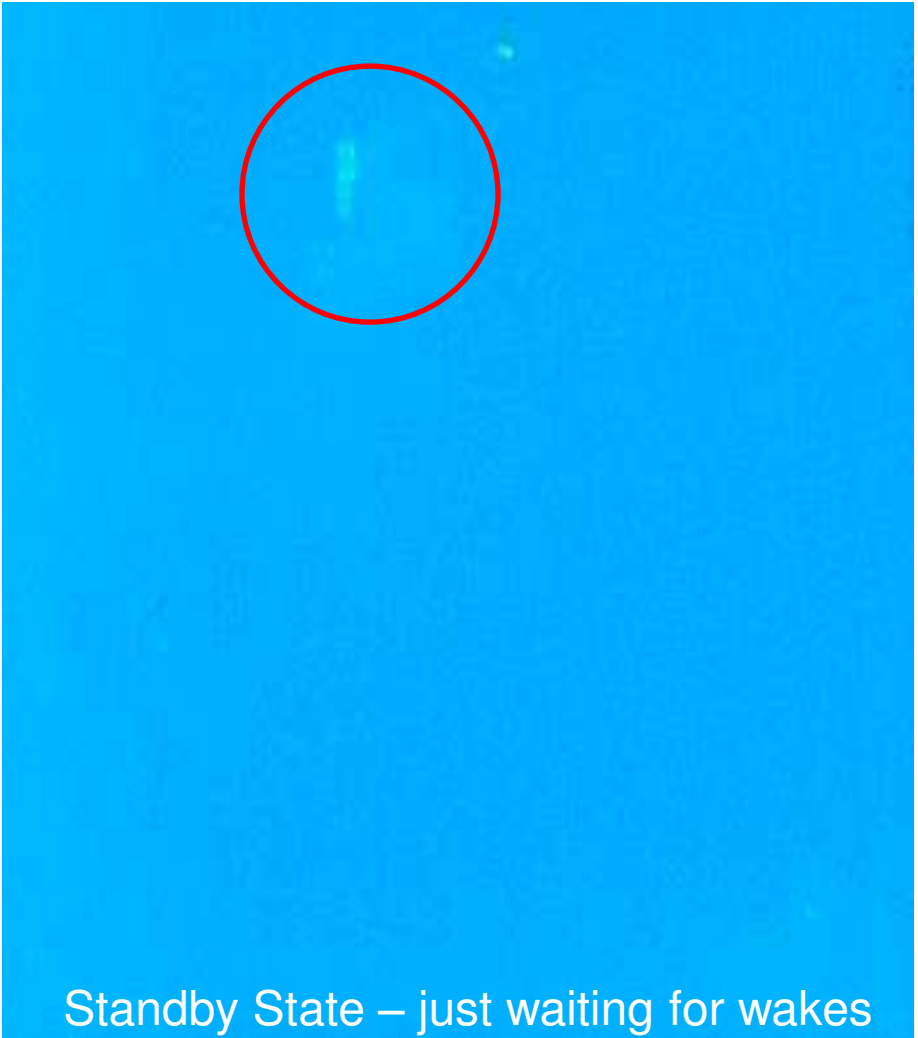
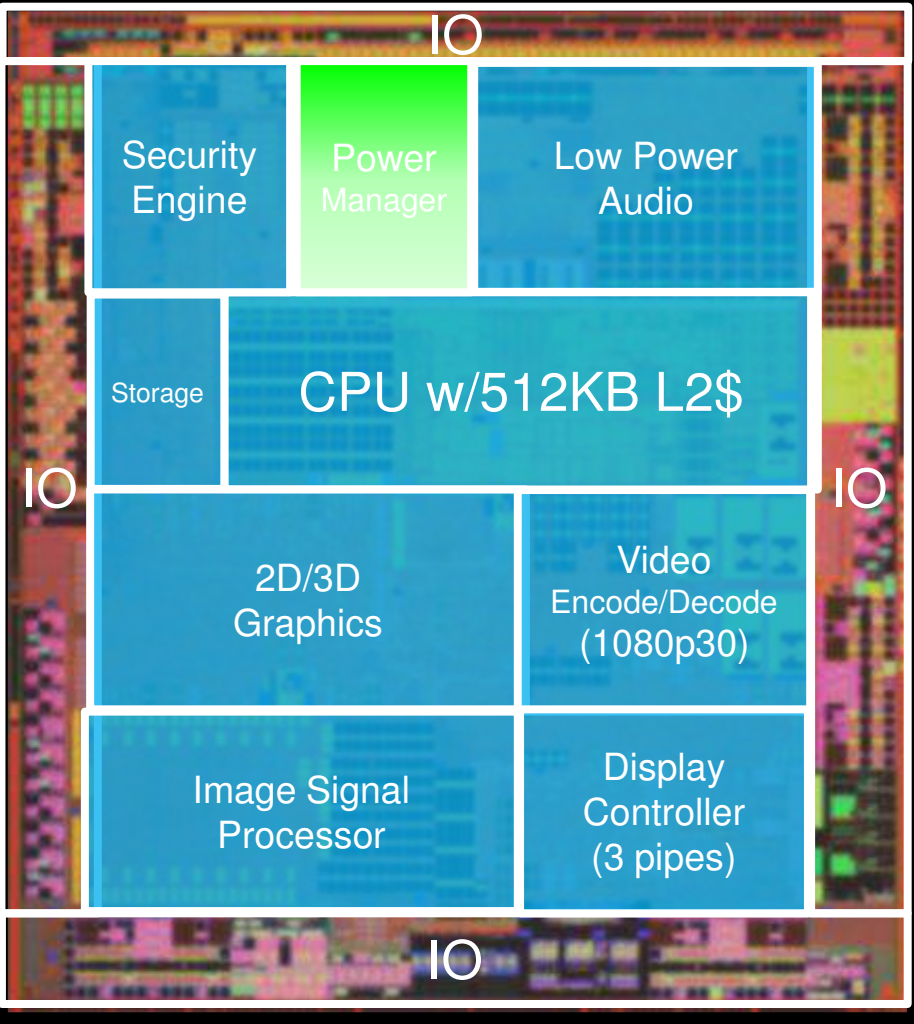
CPU Off



S0i1 System State

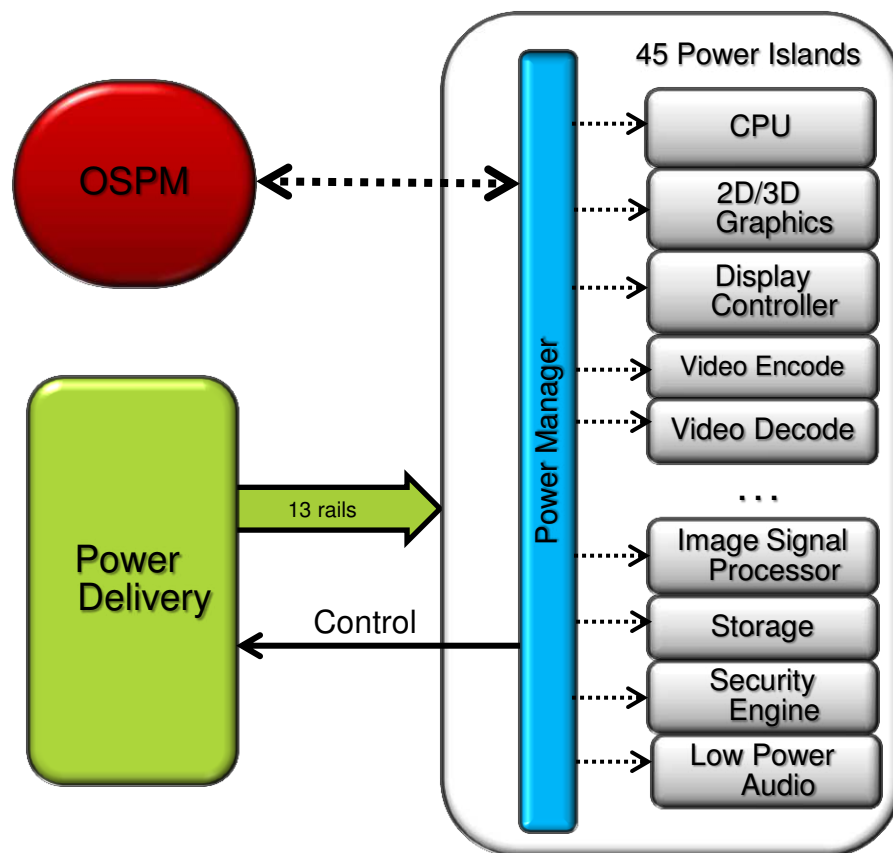


S0i3/S3 System State



New OS Power Management (OSPM)

- Pervasive Power Management
 - ✓ Integrated PMU
 - ✓ Dedicated Power Delivery IC
 - ✓ Active management through HW, FW, SW
- Software-Directed
 - ✓ Operating system power management
 - ✓ Manages all hardware capabilities
- Fine Grain Power Management
 - ✓ 13 rails for IO & logic voltages
 - ✓ 45 Power islands for sub-systems
 - ✓ Aggressive power and clock gating
 - ✓ Integrated clocks and VR power down



OSPM Directs Entire Platform to Lowest Power State

Platform Power Management Architecture

Android Power Manager

■ User Level

Android Power Management Kernel

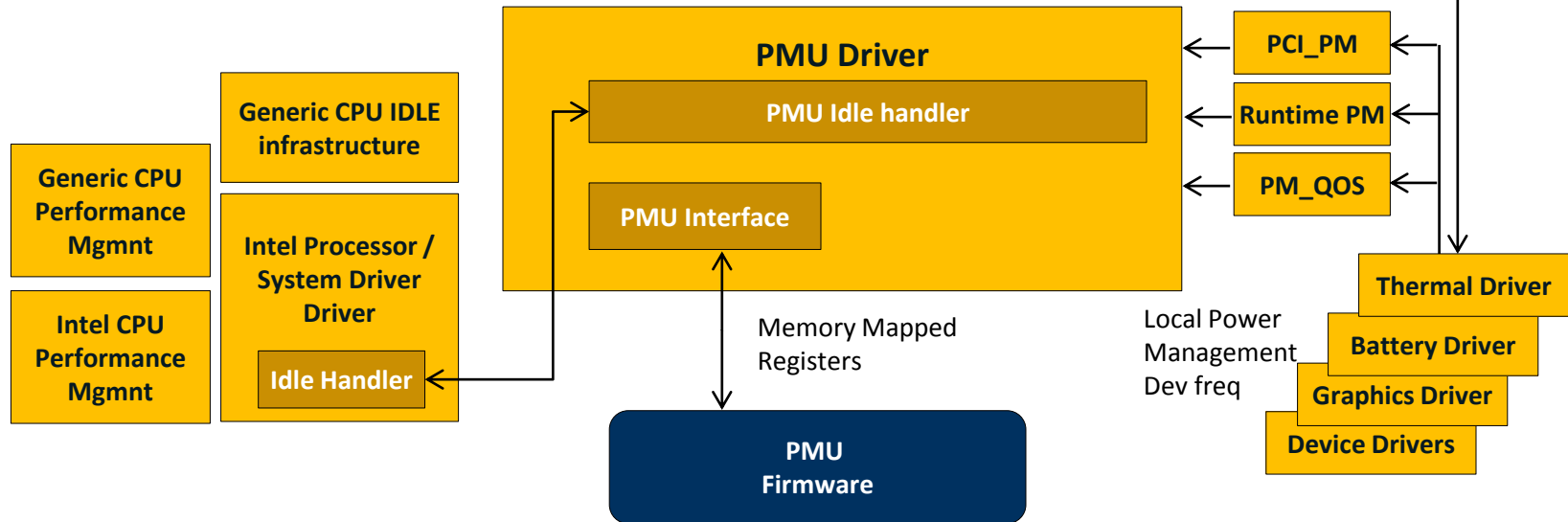
■ Kernel Level

Linux PM

Wakelocks

Early Suspend

■ Firmware



Medfield Reference Platform

High Performance CPU

1.6 Ghz Intel® Atom™ Processor Z2460

Full HD Video

1080p, 30fps Video Encoding

1080p, 30fps Video Playback

Advanced Imaging

Intel Image Signal Processing (ISP)

Advanced UI/UX from Intel

Great Graphics

PowerVR SGX 540 @ 400 MHz

High Speed Connectivity

Intel XMM 6260 21/5.8Mbps HSPA+

Apps

Google* Play (Android* Apps)



High Resolution Display

Internal : 1024x600;1024x768p capable

External : 1920x1080 p30.8" i60

Optimized Android Support

Customizable User Experience

Enhanced Power/Battery life

Standby: 14 days**

Video (1080p): 6 hours

Browsing 3G: 5 hours

Voice Call: 8 hours

Security

Programmable Security Engine

Remote Management Features

Operating System

Android 2.3.7 (Gingerbread)

Android 4.0.4 (Ice Cream Sandwich)

Current Design Wins

Lava XOLO X900 in India

Lenovo K900 in China

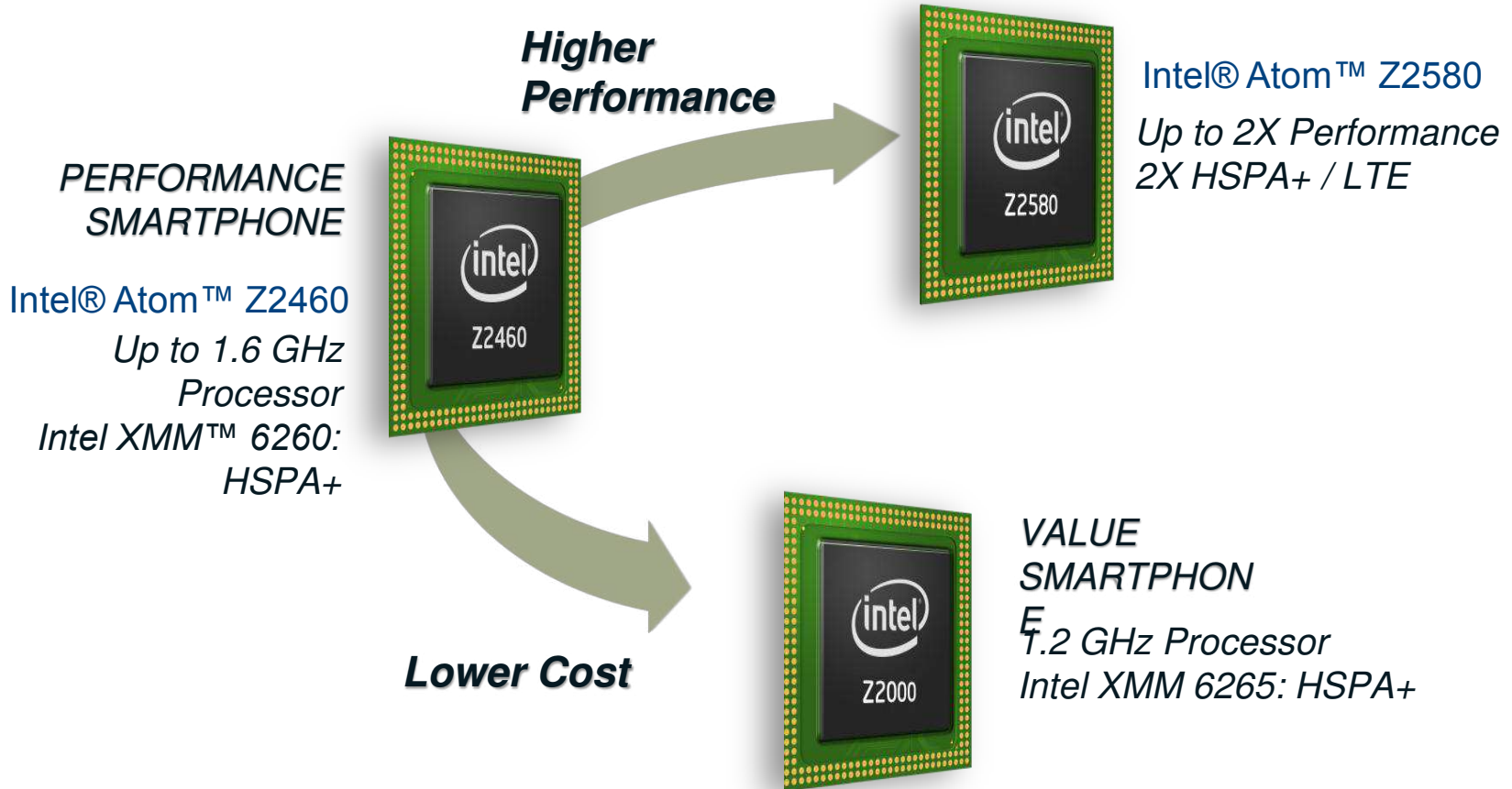
Orange San Diego in UK

Orange with Intel Inside® in France.

* other brands and names may be claimed as the property of others

** Battery: 1500mAh, 3.7V

Smartphone Platform Roadmap



Medfield Summary

- Medfield meets tight Smartphone power consumption constraints and provides outstanding scalar CPU performance
 - ✓ “Race to Idle” minimizes energy consumption while providing excellent end-user experience
 - ✓ Ultra low power SOC states cater to common “user idle” and “system idle” scenarios
 - ✓ Accelerators for Video, Camera, Audio processing provide energy optimized media capabilities

