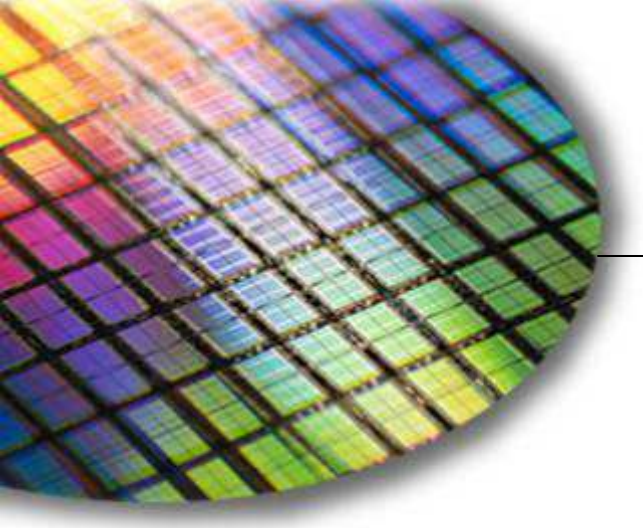

The World Leader in High Performance Signal Processing Solutions

ADI's Revolutionary BF60x Vision Focused Digital Signal Processor System On Chip : 25 Billion Operations/Sec @ 80 mW and Zero Bandwidth

Robert Bushey, Principal Architect & Technologist,

Processor & Digital Signal Processing Core Products & Technologies Group, ADI

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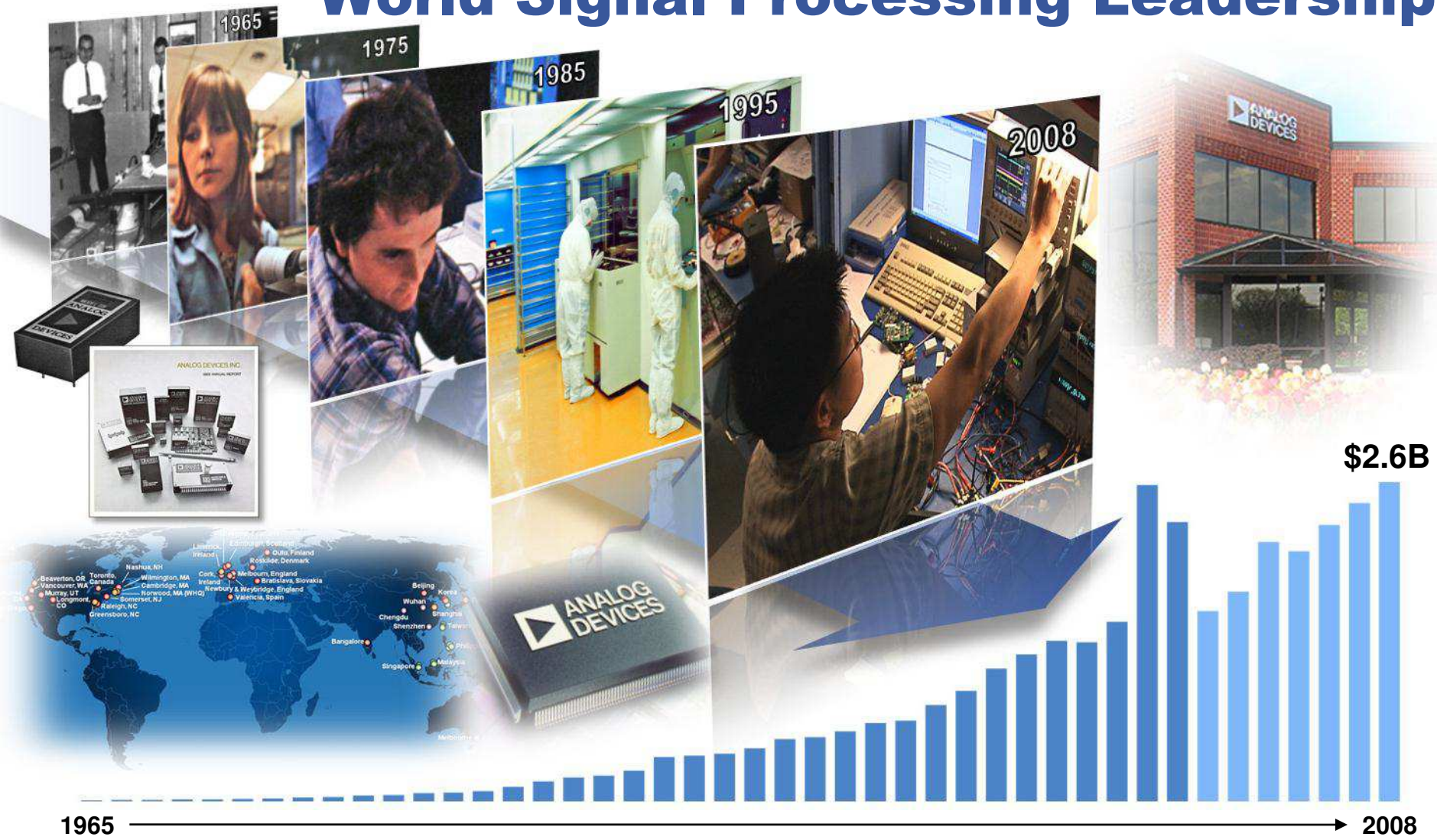
Innovation Has Driven 40+ Years of Real-World Signal Processing Leadership



Source: *ADI revenue history from ADI financial data. Years 2002-2008 represent continuing operations.*

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Two New Groups

Collaborating to Address Customer Needs in Market-specific Ways

Core Products & Technologies Group

Converters

MEMS/ Sensors

Processor-DSP

Power

Linear & RF

Share Segment and Applications Expertise to Enhance Core Technologies

Integrate Core Technologies into Solutions for Key Segments and Applications

Strategic Market Segments Group

Automotive

Communications Infrastructure

Consumer

Healthcare

Industrial & Instrumentation

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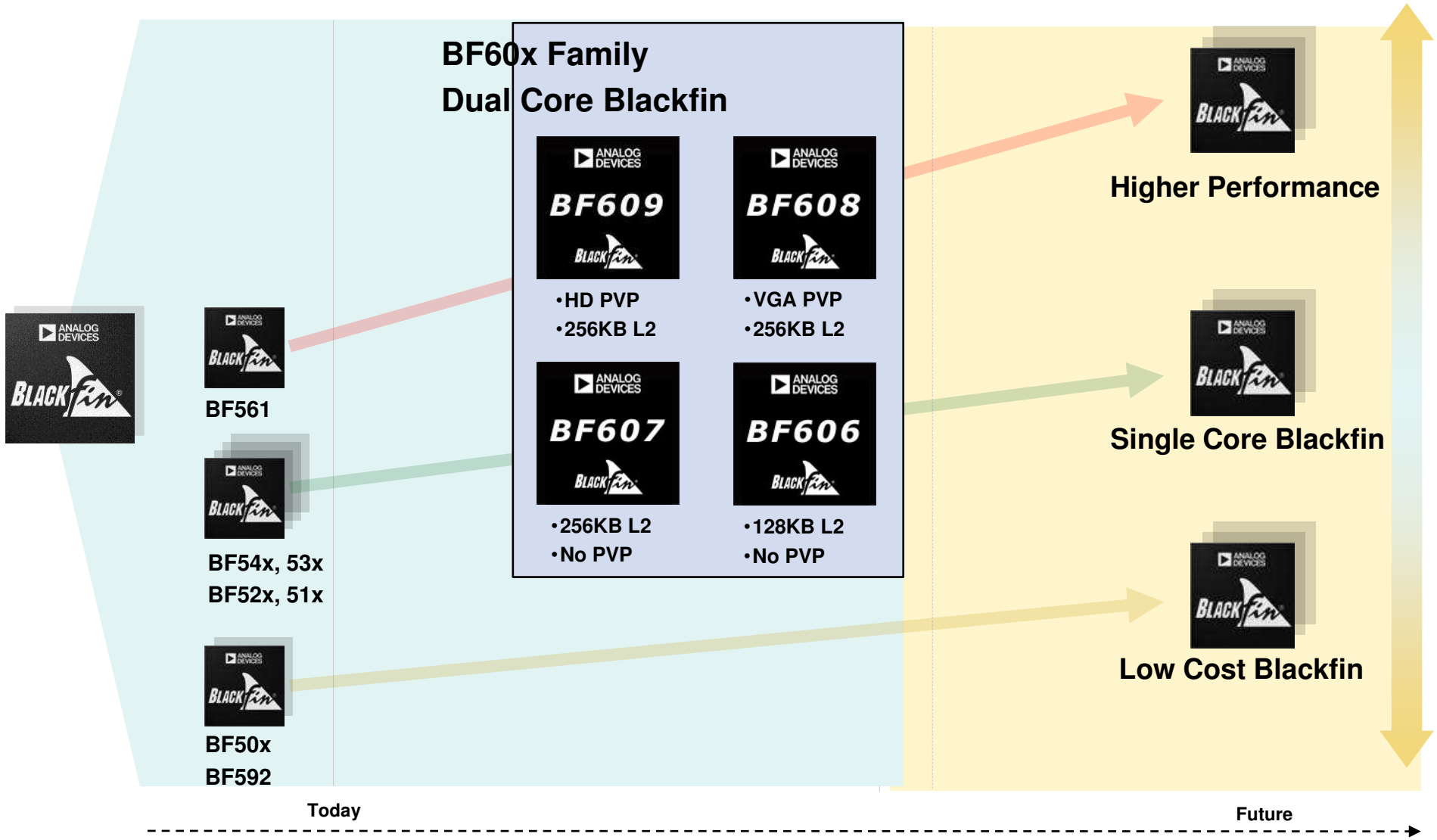
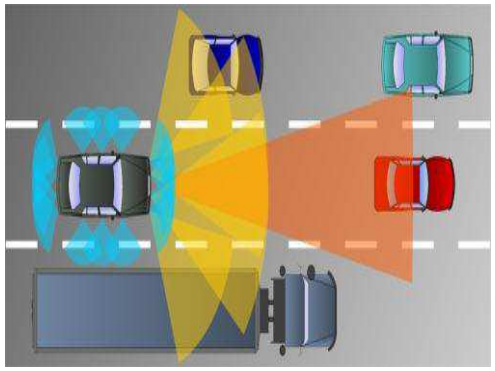
Analog Devices Blackfin Processor Roadmap



Advanced Driver Assistance Systems(ADAS)

- RAdio Detection And Ranging (RADAR)
  - Object detection system using electromagnetic waves to calculate range, height, direction and/or speed of fixed and moving objects.
- LIght Detection And Ranging (LIDAR)
  - Optical sensing technology that measures properties of scattered light to find range and/or other information about a distant object.



- Vision Processing / Video Recognition
  - Requires a Very High Performance Real Time Digital Signal Processing Solution
    - ✓ Pre-crash Warning and/or Avoidance
    - ✓ Lane Departure Warning (LDW)
    - ✓ Traffic Sign Recognition (TSR)
    - ✓ General object classification, tracking & verification

  - ➔ Customer & Market Driven DSP Requirements
    - ✓ Real Time @ 30FPS at 1280x960 Pixels/Frame Performance
      - ➔ 37 Megapixels / Second Real Time ADAS Analytics
      - ➔ Many Parallel and Serial Concurrent Operations / Pixel
      - ➔ BILLIONS of Operations / Sec or GOPS
    - ✓ Low Power, Low Cost, and Low Bandwidth Constraints

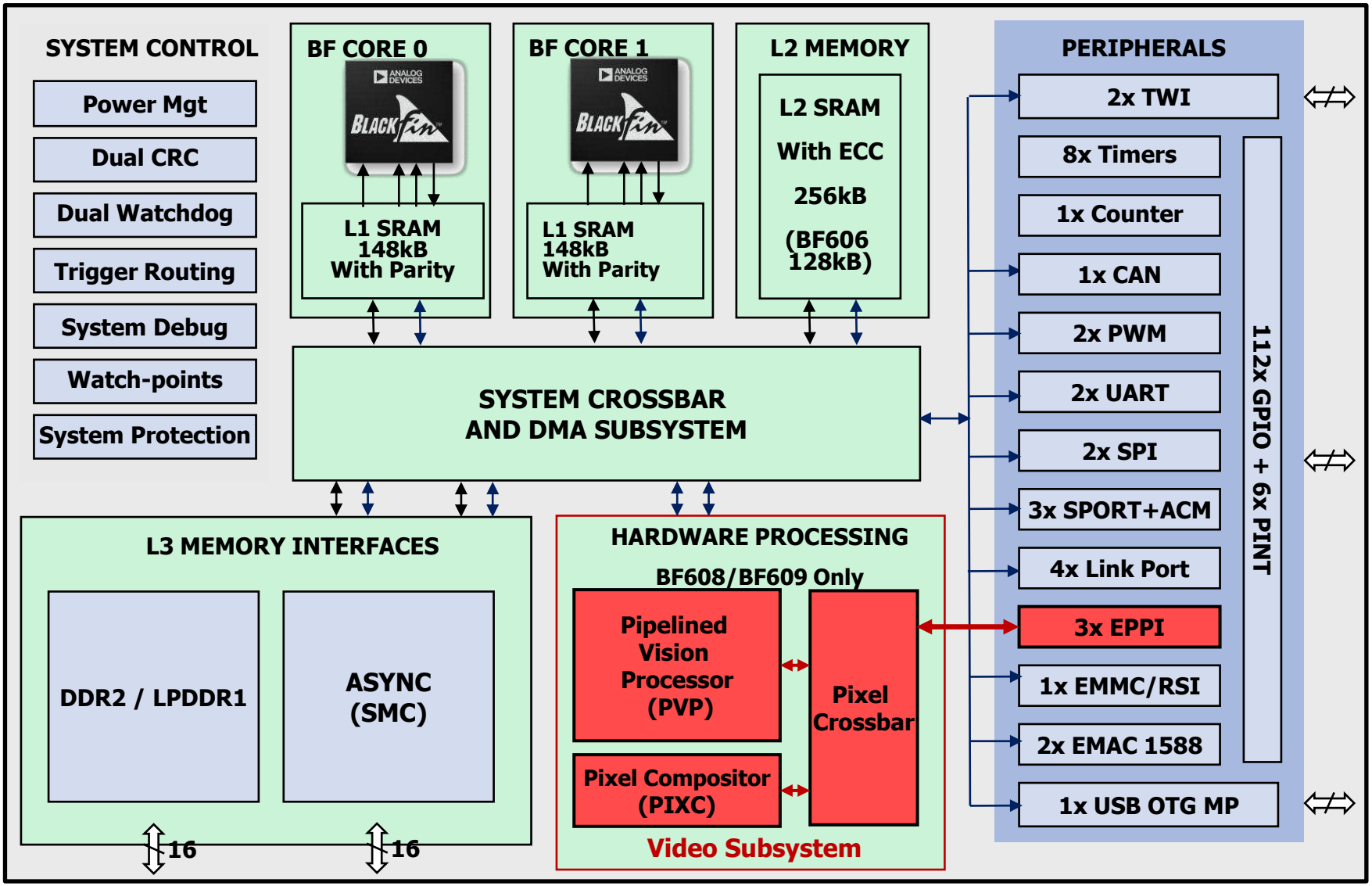
ADSP-BF609 Blackfin Highlights (1)

- **New Pipelined function-level Vision Processor (PVP) for embedded vision applications**
  - **Supports multiple concurrent analytics functions at low price with low power consumption**
    - With our new dedicated function level vision processor, broad adoption of sophisticated, multi-function analytics can now be feasibly deployed into all levels of embedded vision applications
- **Highest performance Blackfin Instruction-level processing**
  - 1GHz of programmable Blackfin instruction level processor performance across two cores
  - Large on-chip memory : 4.3Mbit SRAM & highly efficient system bandwidth

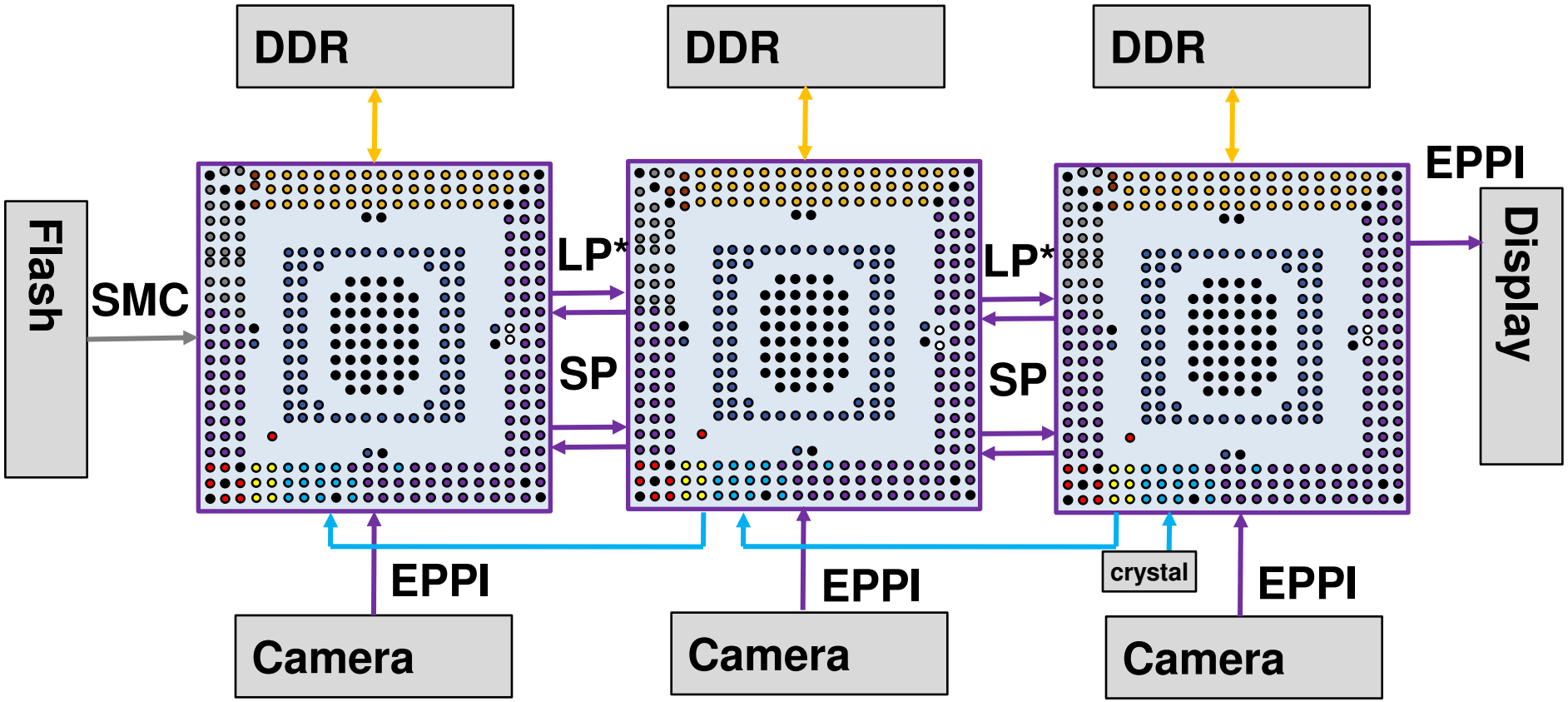
ADSP-BF609 Blackfin Highlights (2)

- **Feature rich peripheral set & connectivity options**
  - Memory interfaces: DDR2, LPDDR, RSI **(Removable Storage Interface for MMC, SD, SDIO, and CE-ATA)**
  - Connectivity: USB2.0, Ethernet, 5 types of serial interfaces, ePPI Video Interface for seamless CMOS sensors and LCD connectivity and control
  - Link ports for high speed multiprocessing and inter-chip communication
- **Integration for safety oriented applications**
  - Memory parity, ECC, system protection unit for detecting/recovering from faults
- **Delivering lowest power per function**
  - Typical power consumption at 25C for the BF609 is 400mW

BF609 Block Diagram



BF609 is Optimized for Many-way Multi-processing With Efficient Inter- chip Communication and Control



* or unidirectional 16-bit PPI

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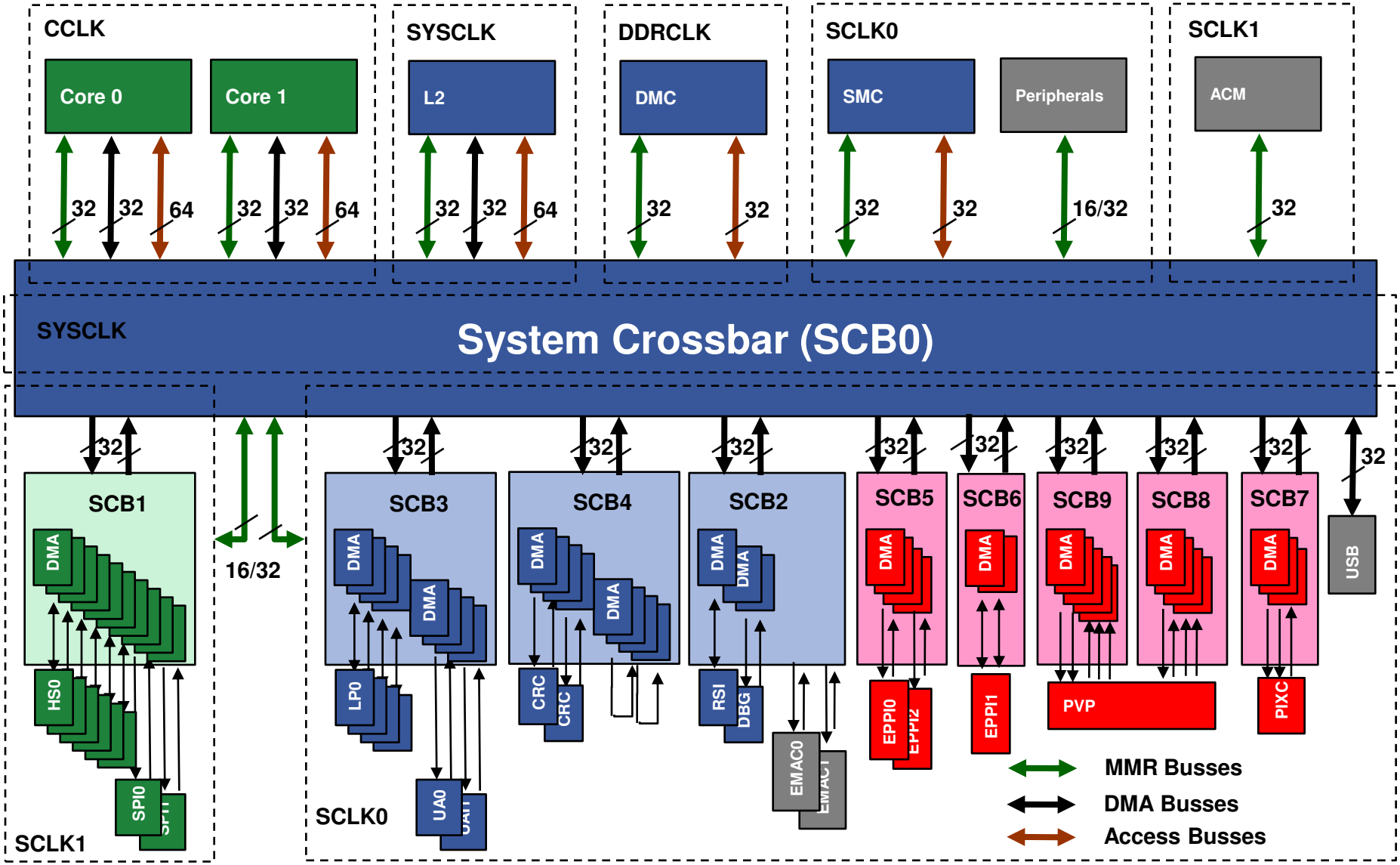
BF609's Masters, Slaves, And Interconnect



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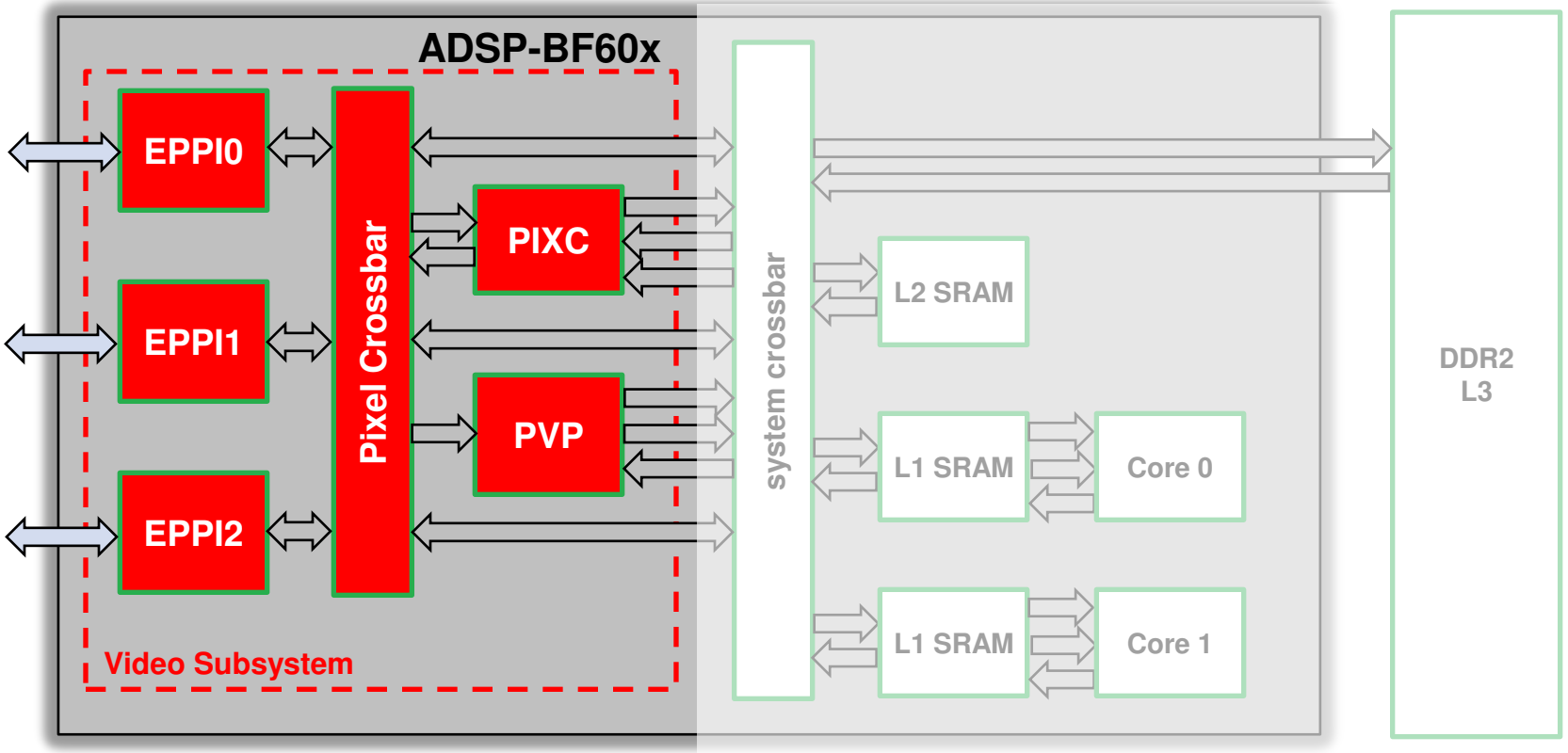
BF609 Video Subsystem & Interconnect



- BF60x Introduces a new Video Subsystem(VSS) architecture and interconnect:
  - 3 Enhanced Parallel Peripheral Interfaces (EPPI);
  - Pipelined Vision Processor (PVP);
  - Pixel Compositor (PIXC);
  - Pixel Crossbar

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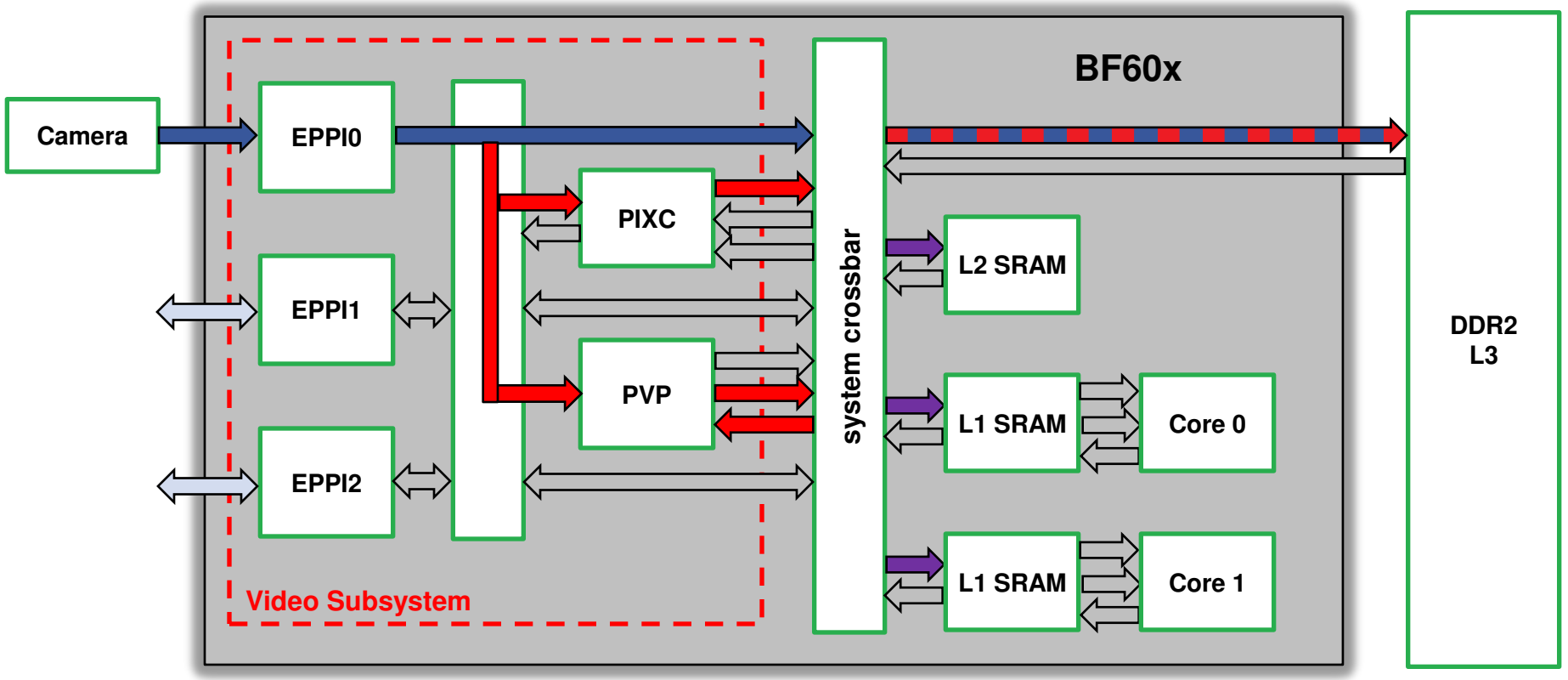
Video Subsystem Vision Processing Datapath



- Data is processed / analyzed before it goes to memory
  - Traffic does not load system bandwidth / power / EMI
- Raw PPI data can go to memories in parallel
  - Data broadcasted to DMA, PIXC and PVP;
  - Multiple data pathes distribute to L1 / L2 / L3 memories

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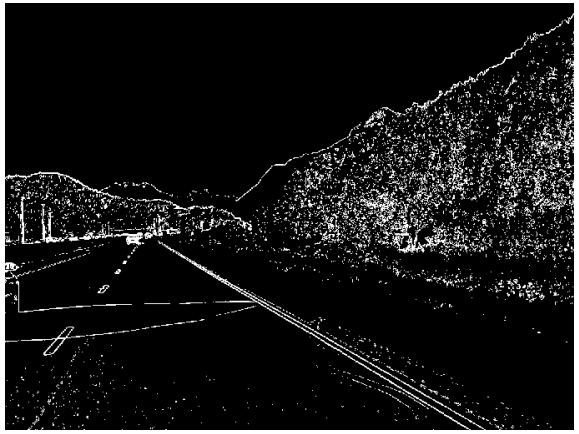
Pipelined Vision Processor(PVP) Overview

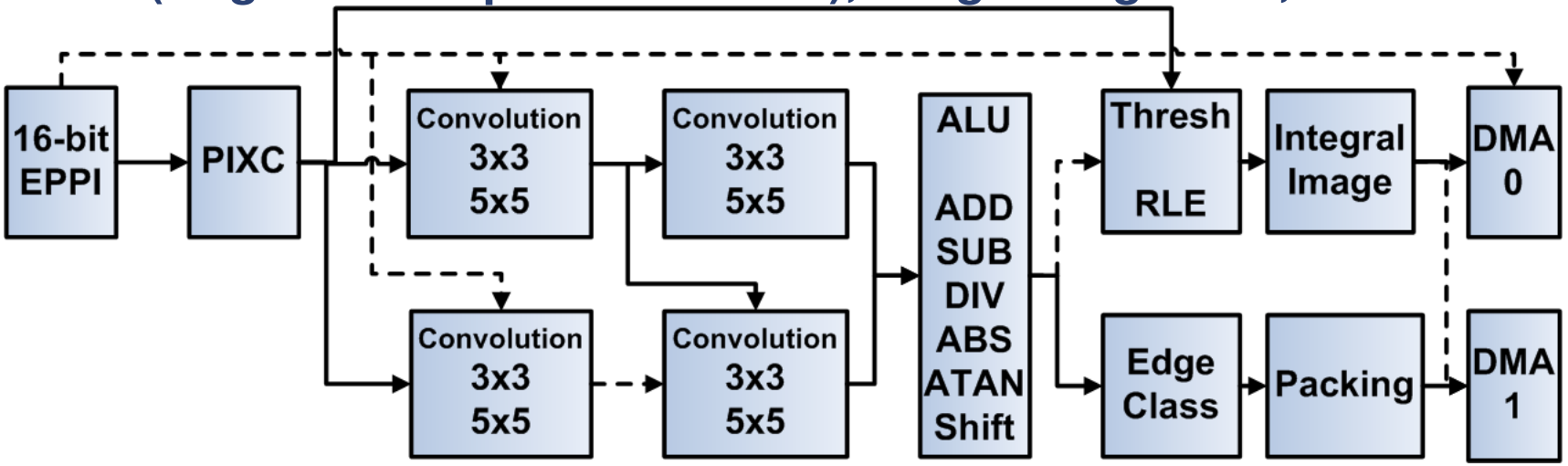
- The PVP computes more than 25 billion operations per second of vision processing while consuming little power and utilizing limited memory bandwidth
  - Used in Advanced Driver Assistance, Robotic and Machine Vision Systems, as well as other adjacent vision/imaging applications
- PVP provides application performance across the following major areas:
  - Object Detection
  - Object Classification and Tracking
  - Object Verification
- PVP works in conjunction with the high performance instruction level programmable Blackfin DSP cores
- PVP reduces required off-chip bandwidth by windowing and pre filtering input data



Example
Canny or Sobel Edge Detection

Pipelined Vision Processor(PVP) Key Features, Pixel Data Path Flexibility & Function Level Processing Capabilities

- Optimal bandwidth reduced pixel datapaths
- Function level processing with highly configurable datapath
- Enables many computationally complex vision applications
- Allows for concurrent support of multiple applications
- Supported Image size (frame rate 30 fps): 1280x960, 1024x768, 640x480
- Supported Pixel-width: up to 16bits
- PVP Supports Vision Function Level Processing: Sobel filter & Canny filter(Convolution), Histogram, ARCTAN and Absolute Value(Angle and amplitude vectors), Image integration, Pixel



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Pipelined Vision Processor (PVP) Key Function Level Processing Blocks (1)

- **2D Convolution Blocks**
  - Supports 1*1, 3*3, 5*5 configurations up to 16-bit input, 16-bit coefficient (updateable line by line)
  - Internal 37-bit Acc & Barrel shift
  - Scaled to 32-bit result
  - PVP Initialization via zero filled lines or duplication of the first/last line per frame

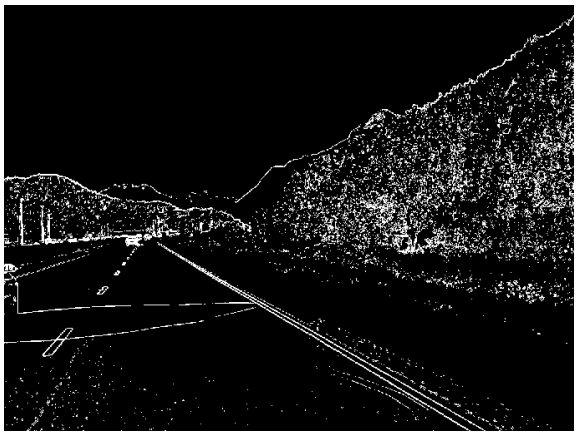
- **ALU/Cartesian to Polar Block**
  - Input two data-streams at 32-bit
  - Output two 16-bit streams or one 32-bit stream
  - Math operations supported (signed/unsigned)
    - ADD, SUB, 32-bit multiply, 32-bit divide, Accumulation (xx bit)
    - Shift (logic, arithmetic), XOR, Masking, Inversion, Arctan, Absolute value (x2+y2)

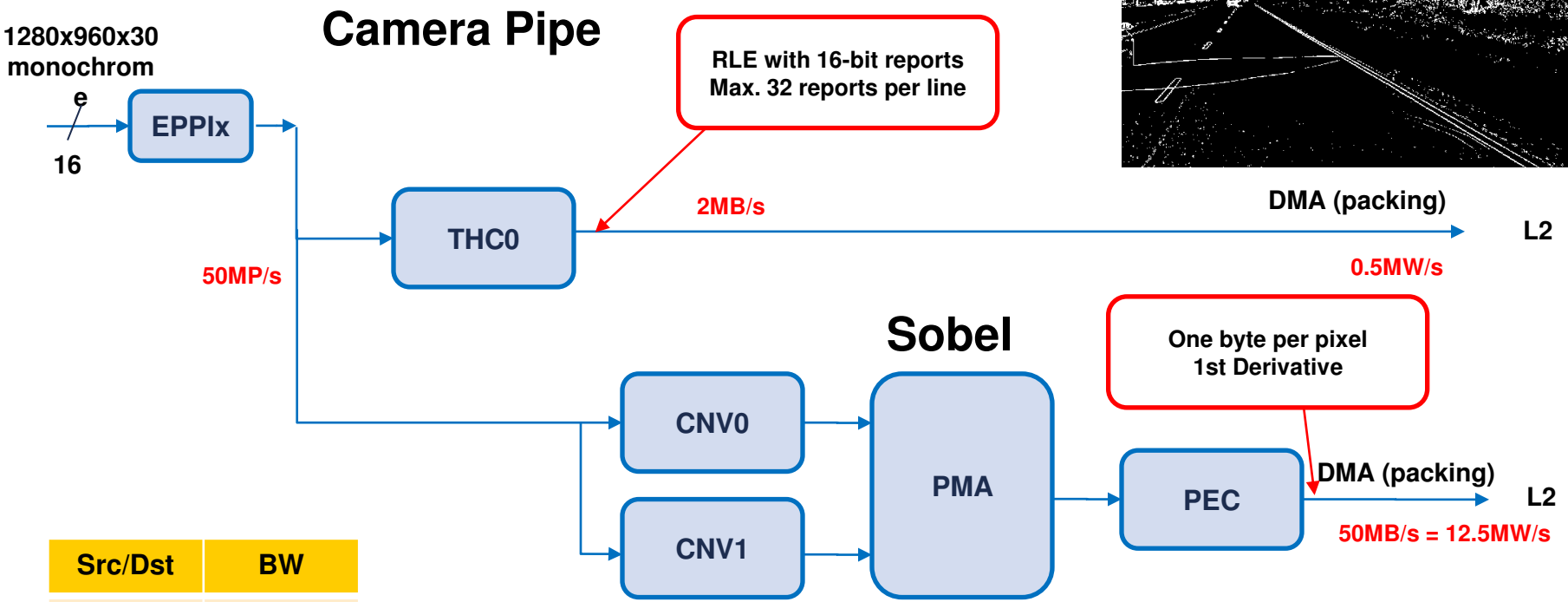
Pipelined Vision Processor (PVP)
Key Function Level Processing Blocks (2)

- **Edge Classification/Packing Block**
  - Covers edge enhancement performing non-linear filtering in a pixel neighborhood, edge classification based on orientation, sub-pixel position interpolation
  - Packs the class, vertical/horizontal sub-pixel position into one byte per pixel

- **Threshold/Integral Image Block**
  - 16 x 32-bit threshold function (output => 4bits classification, RLC, rounding up to nearest threshold, finds max. value)
  - Rudimentary histogram function (16 x 32-bit histogram counter, starts relative to the start of frame/line)

ADAS Use Case: HD HBLB + LDW (PEC)





Src/Dst	BW
L3	0 MB/s
L2	52 MB/s
L1	0 MB/s

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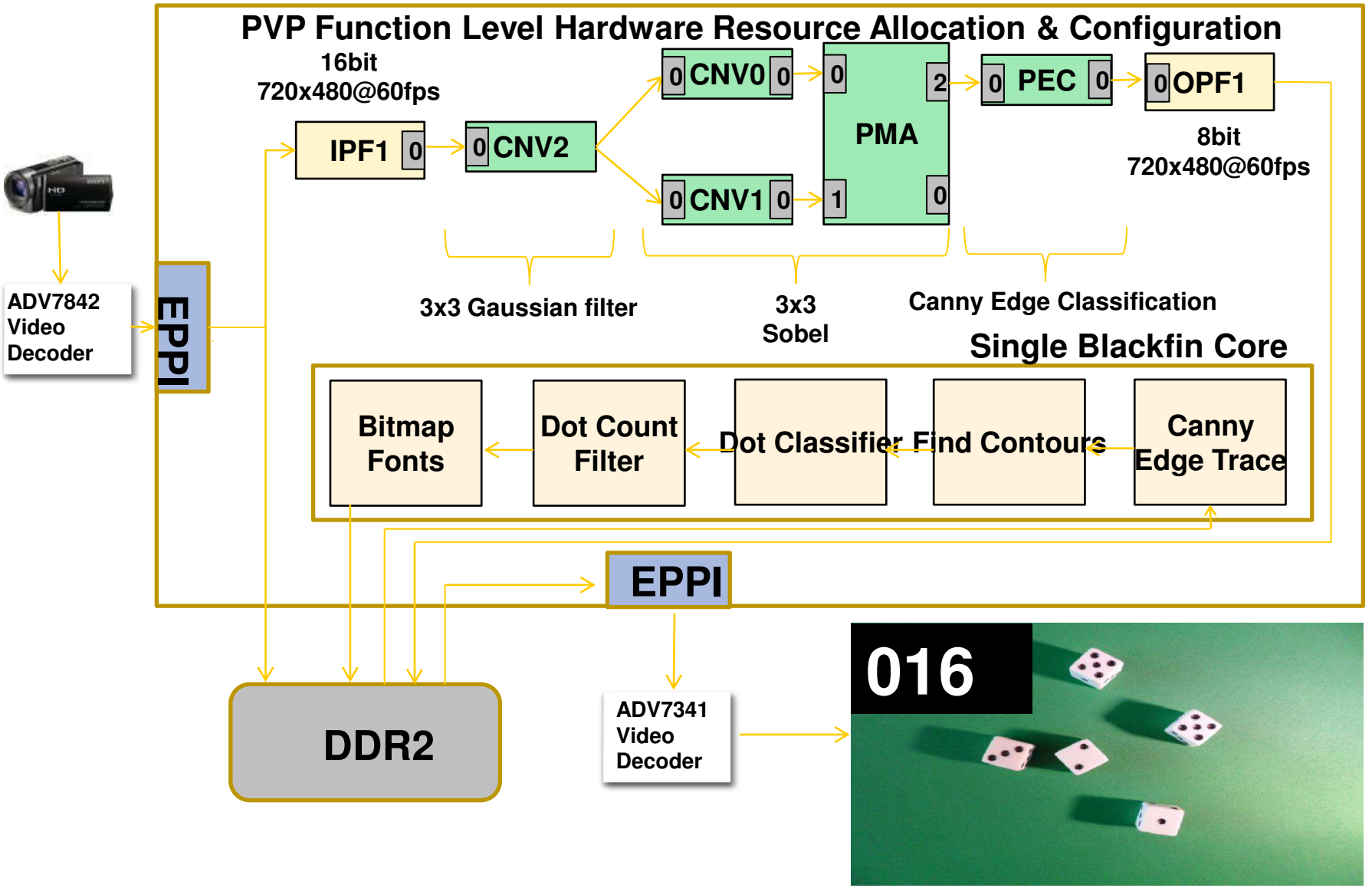
Machine Vision Use Case: Dice Dot Counting



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High Performance, Parallelism Lower Frequency & Low Power

- **TSMC 65nm GP High Performance Process**
  - 25 MAC ~ 50KGates
  - 5 MAC ~ 25KGates

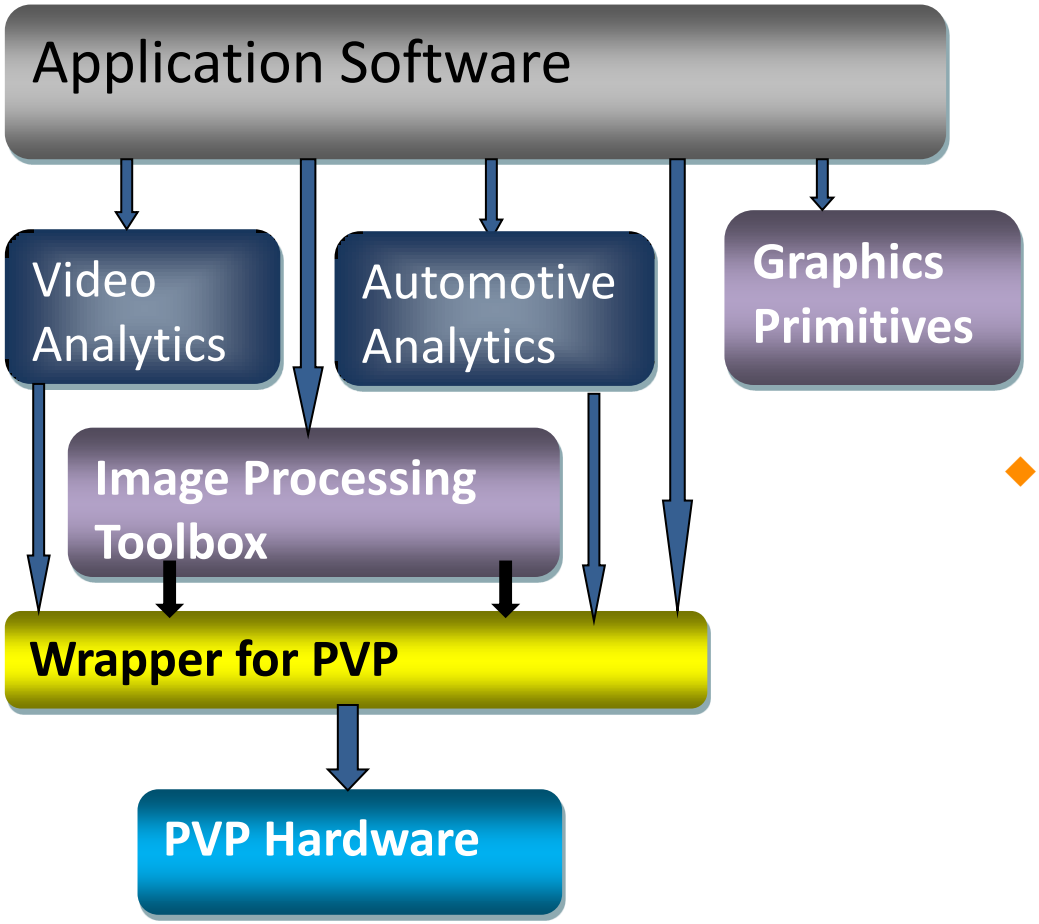
Convolution Architecture		Power Dissipation		
Number of MACs	Clock Speed (MHz)	Leakage (mW)	Dynamic (mW)	Total (mW)
25 MACs	50	11.3	9.5	**20.7**
5 MACs	250	9.4	17.3	**26.7**

- **TSMC 65nm LP Low Power Process**
  - 25 MAC ~ 55KGates

Convolution Architecture		Power Dissipation		
Number of MACs	Clock Speed (MHz)	Leakage (mW)	Dynamic (mW)	Total (mW)
25 MACs	50	0.2	13.6	**13.8**

- 5 GMACs @ 55mW and ZERO incremental BW due to extensive pipelining at multiple levels of the architecture and optimized function level processing
- 11 mW per GMAC

Video/Image Analysis: Software Architecture



- Blackfin Image Processing Toolbox is a collection of hundreds of optimized functions for image analysis & manipulation.
  - Few examples are Histogram operations, morphological operations, 2D convolutions
- Video Analytics Toolbox is a set of high level functions that are focused on solving Intelligent Video Surveillance applications.
  - Current release supports foreground Object/Blob detection
  - Uses Image Processing Toolbox functions

Representative Image Processing, Automotive & Industrial Analytics Toolbox Functionality Available Today (Includes Hardware Mapping as Appropriate)

- Color Conversion
- Image Statistical Tools
- ADAS Modules
- Object & Feature Recognition
- Image Filtering
- Shape-structure Analysis &Computational Geometry
- Geometric Transformations
- Camera Calibration

Tradeoffs, Take-aways, & Conclusions (1)

- An appropriate architectural solution can best be derived from a detailed understanding of market and technical requirements acquired through close customer collaboration and extensive end product technical domain knowledge
  - The pipelined vision processor was architected and defined through customer collaboration coupled with general vision and imaging technical hardware and software domain expertise
- Hardware/Software/IP partitioning is very important and ultimately determines solution power, performance, and cost
  - Choosing to perform appropriate required functions in software on one or more symmetrical or asymmetrical instruction level processors provides many advantages including flexibility
  - Partitioning highly computationally complex imaging or vision processing into the appropriate hardware functional IP blocks will generally lead to a cost optimized, low power, and reduced memory bandwidth solution
  - Optimizing pixel datapaths and flow in an imaging or vision focused SOC is very important when defining a low cost and power solution

Tradeoffs, Take-aways, & Conclusions (2)

- Many systems on chip architectures will continue to require functionality and IP driven by multiple markets and many applications
  - The BF60x SOC was architected and defined to meet the requirements across multiple markets(e.g. automotive ADAS and industrial vision) and across many applications(e.g. lane departure warning, traffic sign recognition, and barcode reading)
- Trade offs involving instruction level processors, function level processors, dedicated internally developed IP, and 3rd party IP must be weighed carefully in order to arrive at the most optimal SOC architecture and general definition
  - The BF609 contains instruction level digital signal processors, a function level processor which is comprised partly of dedicated internally developed vision focused IP, and 3rd party IP
  - The selection, partitioning, and definition of these SOC components is vital to meeting challenging customer and industry competitive requirements
- Architecting and defining a highly efficient crossbar interconnect and DDR memory controller IP is critical to ensure that the system meets all of the bandwidth and latency requirements across many demanding masters
  - Arbitration and prioritization optimization throughout the entire data path from master to slave is paramount to satisfying all master requirements when executing highly computationally complex vision applications

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- Email
  - Robert.Bushey@analog.com
- www.analog.com/BlackfinModules
  - Vision Analytics Toolbox(VAT)
  - Image Processing Toolbox(IPTBX)
  - ADAS Vision Analytics Toolbox(AVAT)
  - 2D Graphics Libraries(BF2DGL)
- www.analog.com/Blackfin
  - Blackfin Processors & SOCs
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