



Xilinx Zynq-7000 EPP

An Extensible Processing Platform Family

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Agenda

- **Xilinx Series 7 Highlights**
- **Zynq-7000 EPP Architecture & Silicon**
- **Zynq-7000 Software & Applications**
- **Summary**

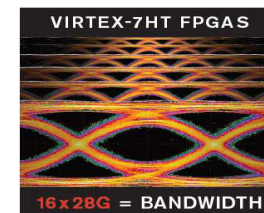
Xilinx 7 Series Highlights

- **7 Series silicon devices**
 - 28 nm Technology, TSMC HPL process
 - 50% reduction in power over 40 nm devices
- **3 FPGA Fabrics**
 - Artix = Low cost, low power FPGA (“1W FPGA”)
 - Kintex = Density & performance FPGA (“Market Sweet spot”)
 - Virtex = Highest density and performance FPGA
 (“More than Moore”)
- **‘More than Moore’ density increase**
 - Up to 2M logic cells
 - Using Stacked Silicon Interconnect Technology (SSIT)
- **Improved GT bandwidth**
 - GT bandwidth increased to 28 GHz
- **Zynq Embedded Processing Platform (EPP)**



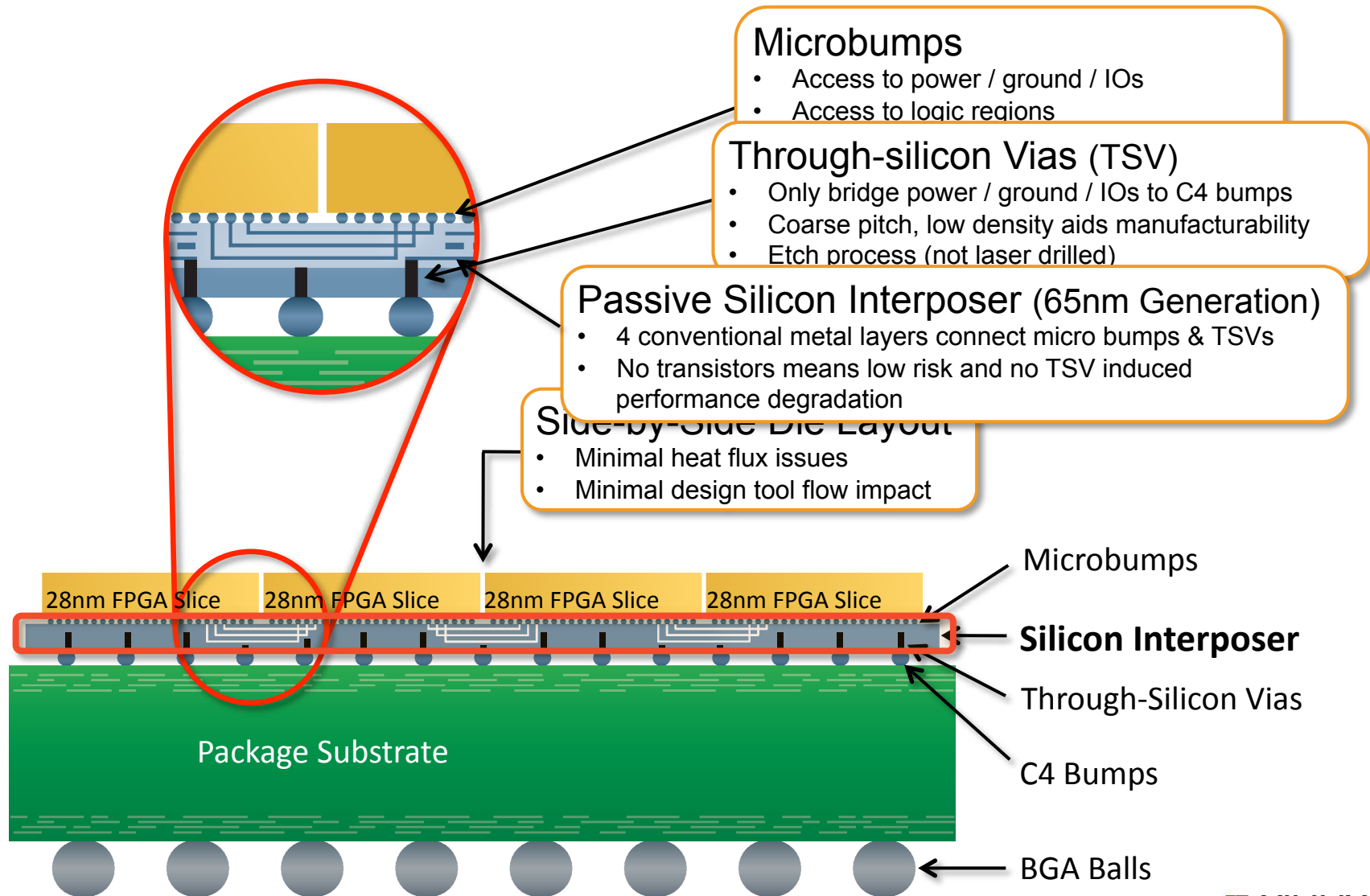
Design Green by Xilinx

ARTIX⁷
KINTEX⁷
VIRTEX⁷



More Than Moore

Xilinx Stacked Silicon Interconnect Technology



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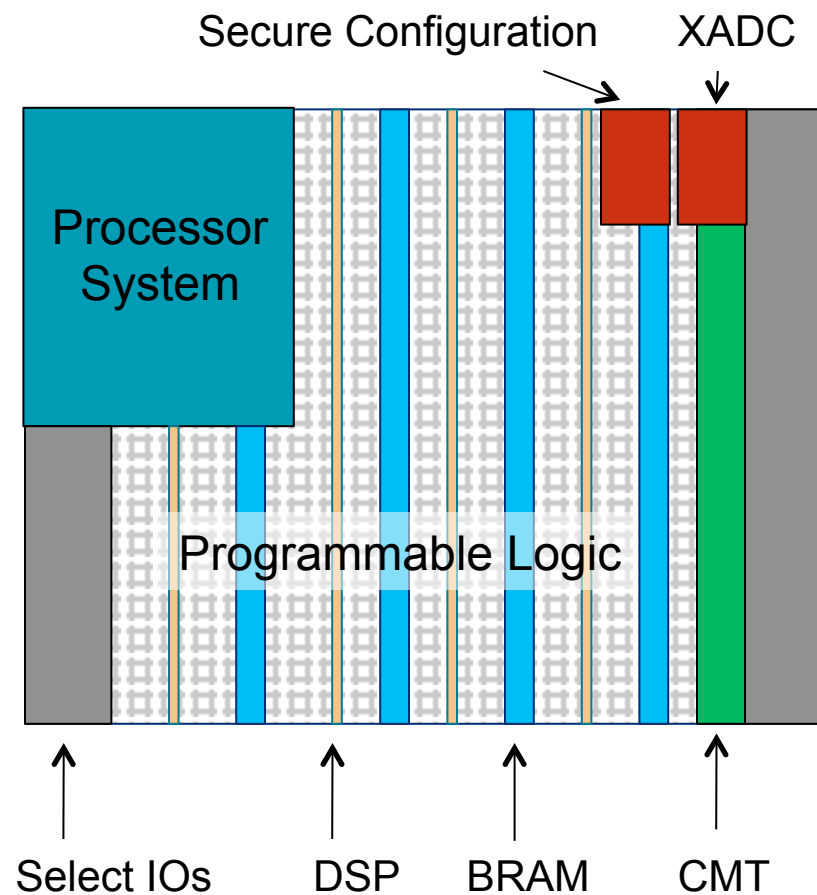
Zynq-7020 Device

Processor System (PS)

- ARM Cortex-A9 MPcore
- Standard Peripherals
- 32-bit DDR3 / LPDDR2 controller
- 54 Multi-Use IOs
- 73 DDR IOs

Programmable Logic (PL)

- 85 K Logic Cells
- 106K FFs
- 140 32-Kb Block RAM
- 220 DSP Blocks
- Dual 12-bit ADC
- Secure configuration engine
- 4 Clock Management Tiles
- 200 Select IO (1.2-3.3V)



Zynq-7000 Device Family

	Zynq-7000 EPP Devices	Z-7010	Z-7020	Z-7030	Z-7040
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™			
	Processor Extensions	NEON™ & Single / Double Precision Floating Point			
	Max Frequency	800MHz			
	Memory	L1 Cache 32KB I / D, L2 Cache 512KB, on-chip Memory 256KB			
	External Memory Support	DDR3, DDR2, LPDDR2, 2x QSPI, NAND, NOR			
	Peripherals	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
Programmable Logic	Approximate ASIC Gates	~430K (30k LC)	~1.3M (85k LC)	~1.9M (125k LC)	~3.5M (235k LC)
	Extensible Block RAM	240KB	560KB	1,060KB	1,860KB
	Peak DSP Performance (Symmetric FIR)	58 GMACS	158 GMACS	480 GMACS	912 GMACS
	PCI Express® (Root Complex or Endpoint)	-	-	Gen2 x4	Gen2 x8
	Agile Mixed Signal (XADC)	-	-	2x 12bit 1Msps A/D Converter	
I/O	Processor System IO	-	-	130	-
	Multi Standards 3.3V IO	100	200	100	200
	Multi Standards High Performance 1.8V IO	-	-	150	150
	Multi Gigabit Transceivers	-	-	4	12

Zynq-7000 Processor System (PS)

- **Dual Core Cortex ARM A9**

- NEON, 512 KB L2 cache
- 256 KB On-Chip-Memory (OCM)

- **DDR Interface**

- DDR3 Performance
- High BW utilization

- **Config & Legacy Memory I/F**

- Quad-SPI, NOR, NAND

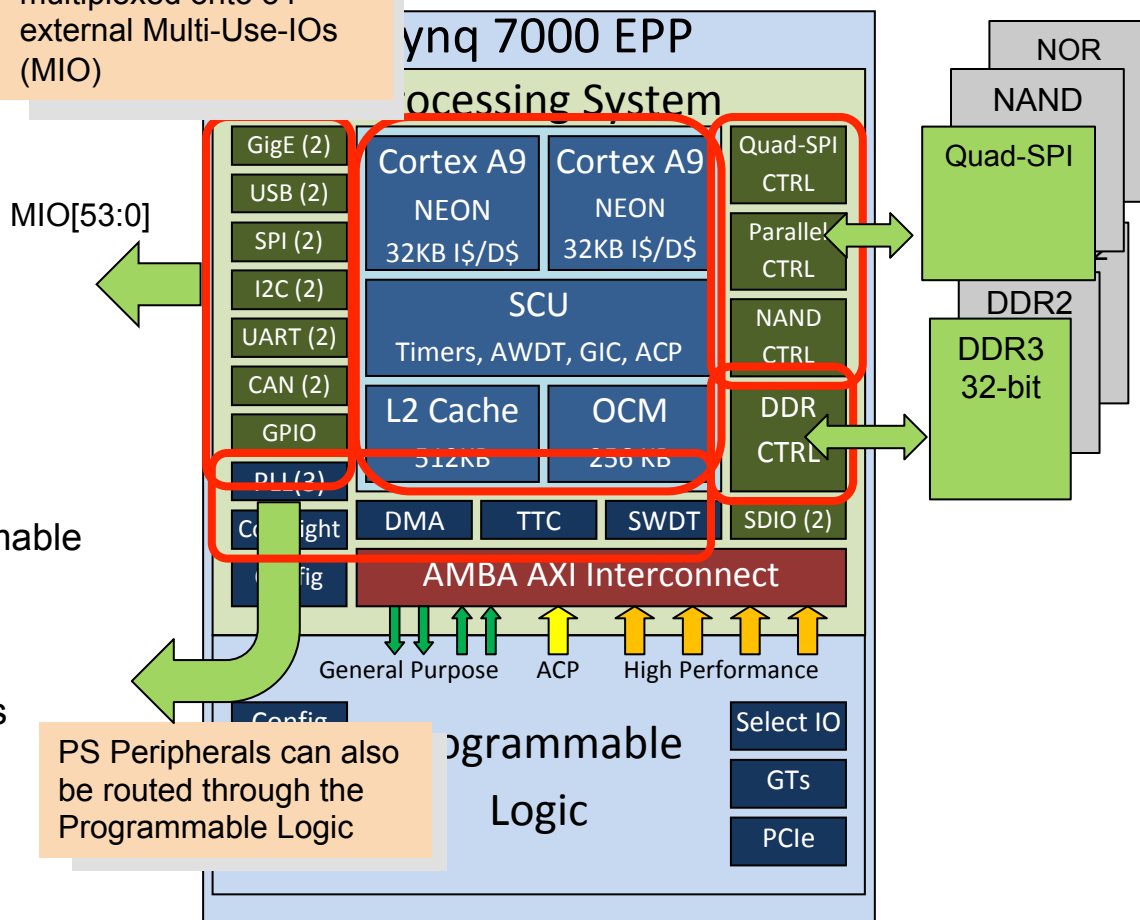
- **Standard Peripherals – GigE ...**

- Available to PS IO or to Programmable Logic

- **System Level Peripherals**

- Clock generation, Counter Timers
- 8 Channel DMA controller
- Coresight Debugging

PS Peripherals can be multiplexed onto 54 external Multi-Use-I/Os (MIO)



Zynq-7000 Programmable Logic (PL)

Programmable Logic Resources

- 30K – 235 K Logic Cells
- Dedicated 36 K-bit BRAMs, DSP, CMT
- XADC dual channel 12-bit ADC
- Up to 12 GTs with PCIe hard core
- Up to 300 Select IOs

Programmable Logic AXI Interfaces

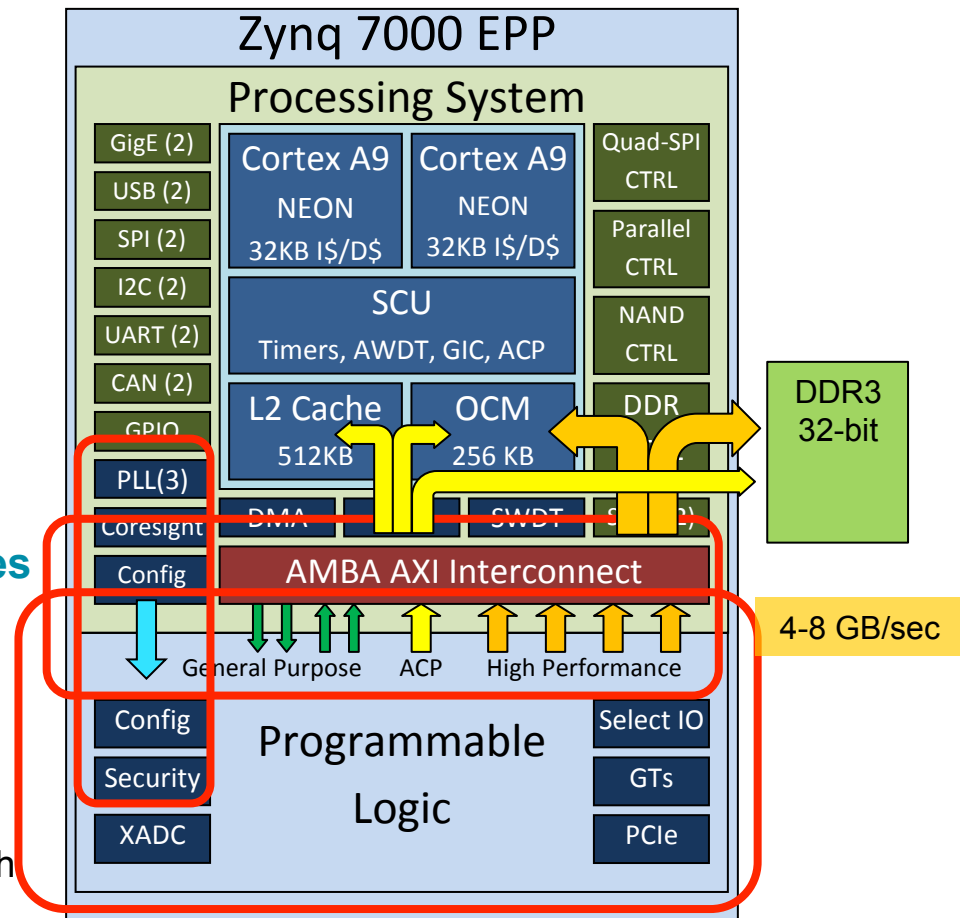
- Multiple 32/64 bit AXI interfaces to PL
- Accelerator Coherency Port (ACP) with access to caches

Programmable Logic System Interfaces

- Interrupts, DMA control
- Debug

High Performance PL Configuration

- Security Decryption Engine
- Under 200 ms configuration time from flash
- Debugging interfaces



Customizing Zynq

Tools for the Programmable Logic System Builder

■ Clocking

- Flexible clock sources (PS or PL)
- Simple clock interfaces

■ Memory and Peripheral access

- PL access to all memory: Caches, OCM, DDR
- 2 dedicated DDR ports ensure bandwidth
- PL access to all peripherals in PS

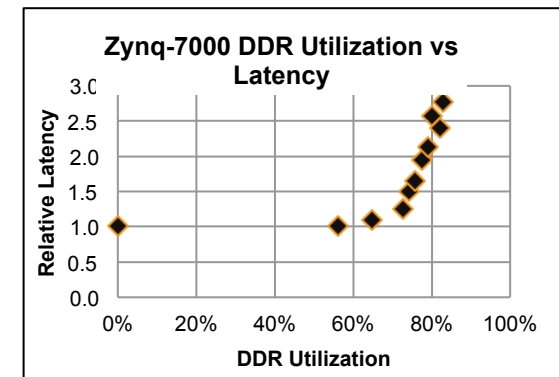
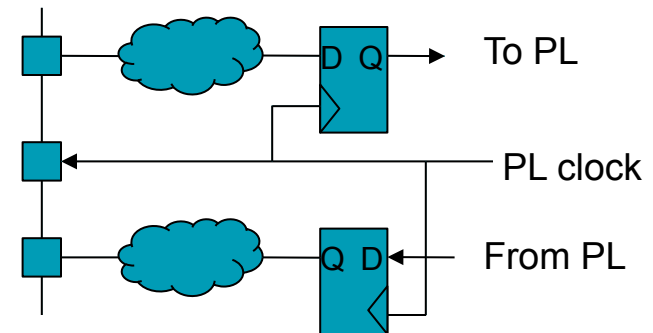
■ Interconnect

- AXI Interconnect IP available from Xilinx
- Optimized for FPGA implementation

■ Debug and Misc.

- Bidirectional cross-triggers (Coresight and Chipscope)
- 16 general purpose interrupts from PL to PS

Simple Clock Interfaces

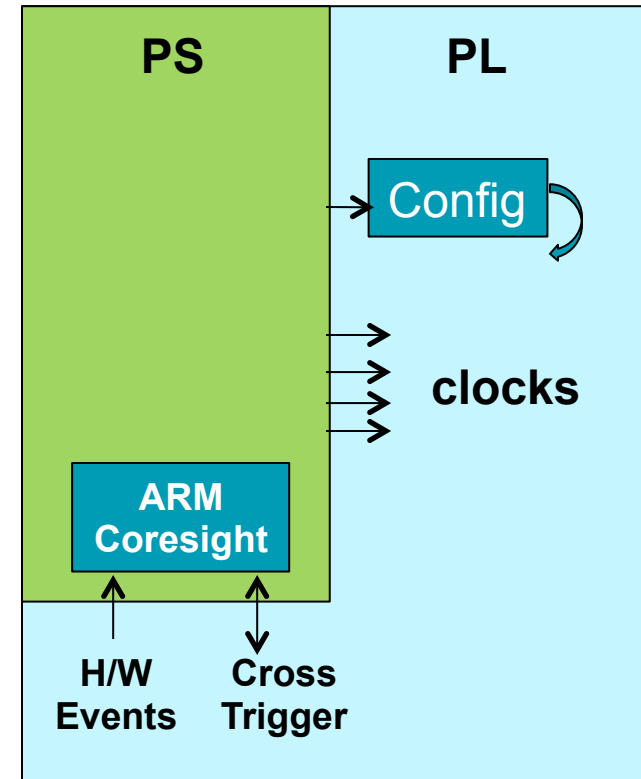


SW managed Programmable Logic (PL)

Linux based, “remote controlled”, programmable logic

SW user experience: SoC with integrated PL

- Configure PL (full and partial)
- Start/stop & single step clocks
- Setup & update HW triggers
- Monitor HW performance counters
- Observe & sync to PL hardware events



Zynq-7000 Power Saving Features

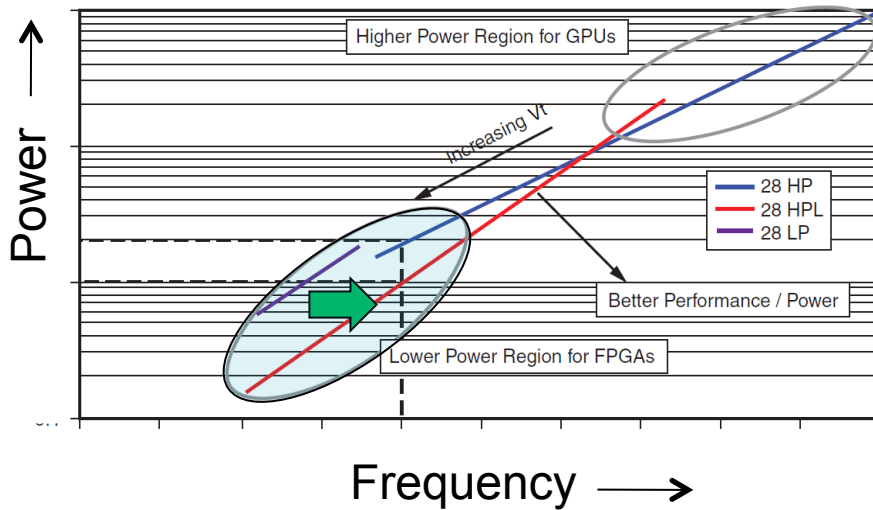
- **Low power 1.0V HPL 28 nm process silicon technology**
- **Programmable Logic can be powered off and on as needed**
 - 40-90% reduction in static power depending on device
 - Very fast configuration times when loaded from DRAM
- **Low power ARM Cortex-A9 MP**
 - Incorporates clock gating and power-down modes
- **Support for LPDDR2 devices**
 - Ultra low power self refresh
- **Peripherals shutdown**



Design Green by Xilinx

Engineering Insights

Process Selection Criteria

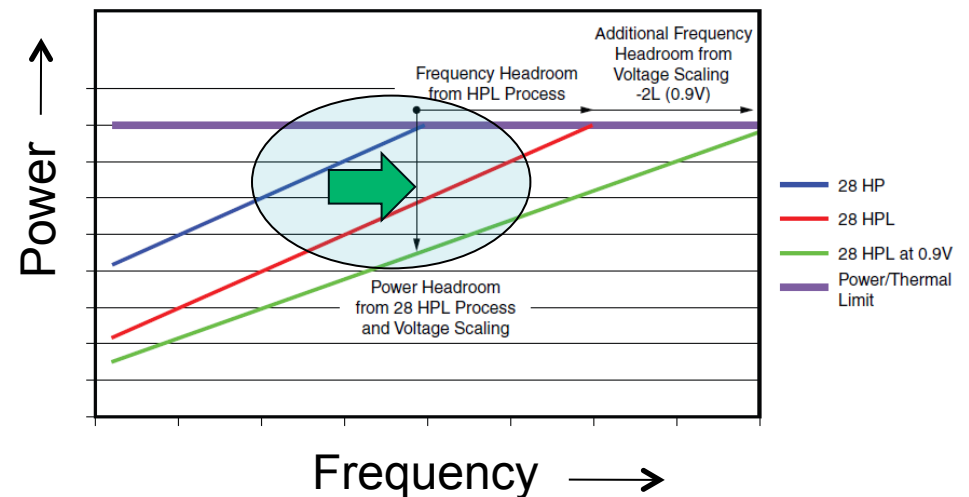


Process Considerations:

- **28 HP: Highest Performance HKMG Process** (but must be able to afford power; e.g. GPU)
- **28 HPL: Low power HKMG process** (shifts down HP power / performance range)
- **28 LP: No HKMG low power process** (cheaper than HPL, but less performance)

Xilinx' Reasons for Selecting HPL:

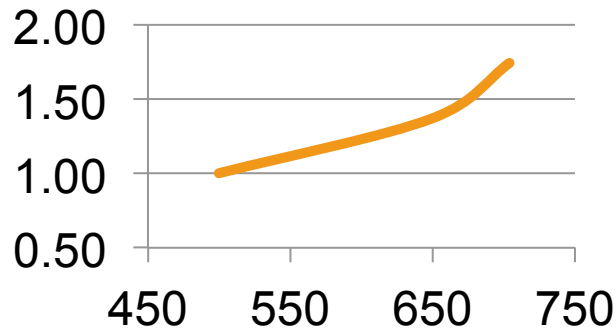
- **Higher performance than LP** (at same power level)
- **Higher performance vs HP at FPGA TDP** (or lower power at same performance)



Engineering Insights

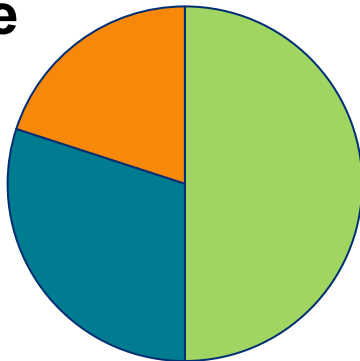
Finding The Frequency Sweet Spot (within the HPL Process)

Normalized Power vs. Frequency



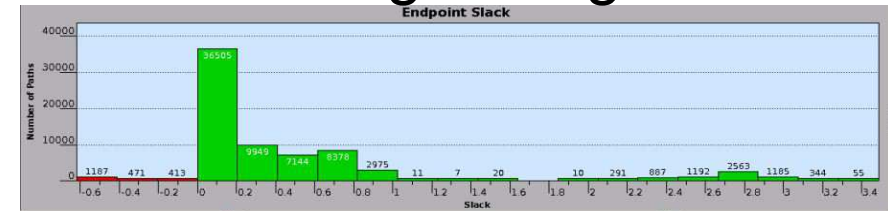
Vt usage

- High Vt
- Med Vt
- Low Vt

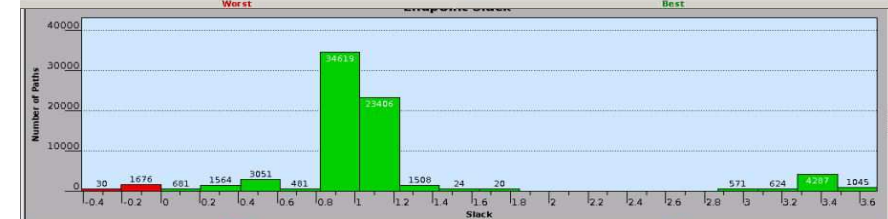


Timing Histograms

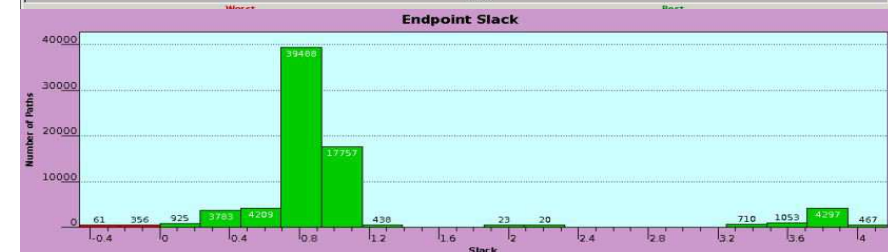
Worst Setup
-40c



Hold

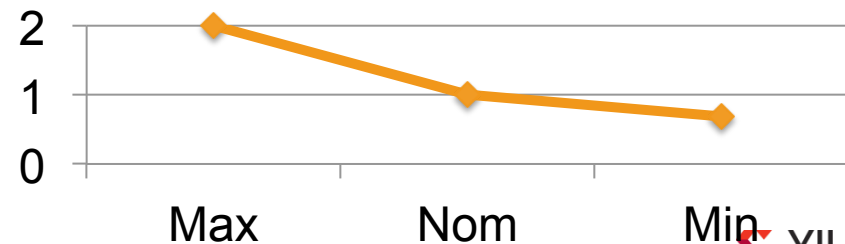


Typical



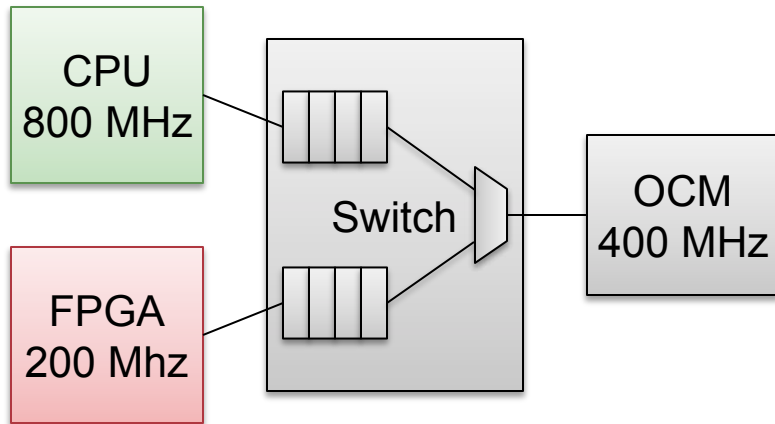
Normalized Path Delay

Delay Variation



Engineering Insights

Configuring Interconnect



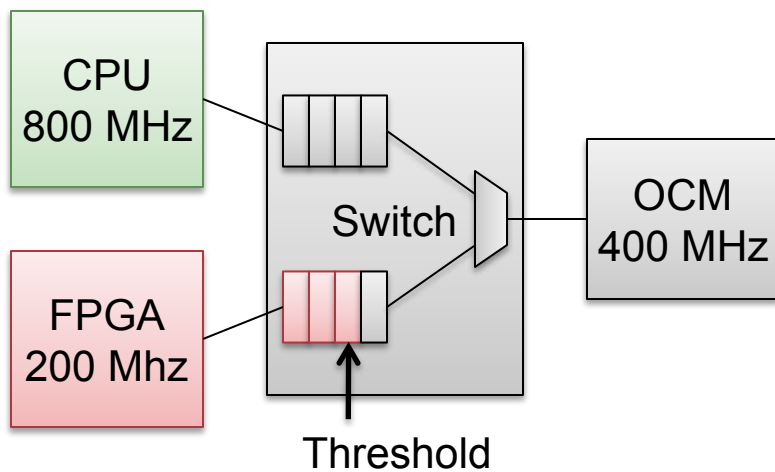
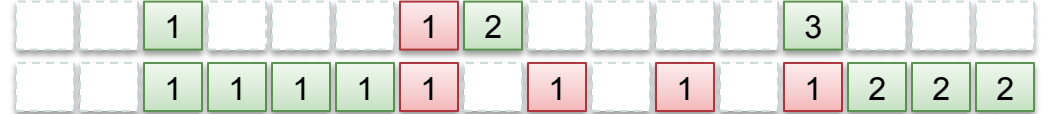
CPU:



FPGA:



OCM:



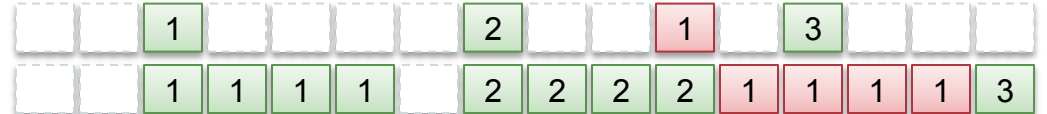
CPU:



FPGA:



OCM:



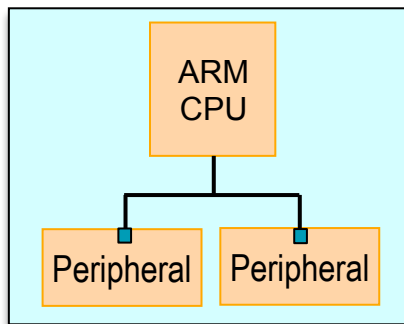
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Zynq-7000 Use Cases

#1

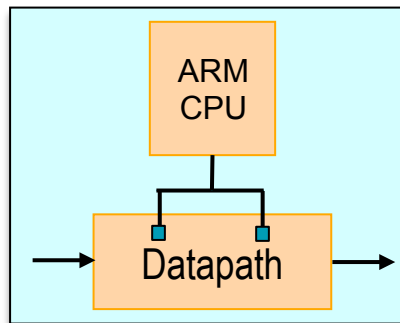
Embedded Control



Ex: Motor Control

#2

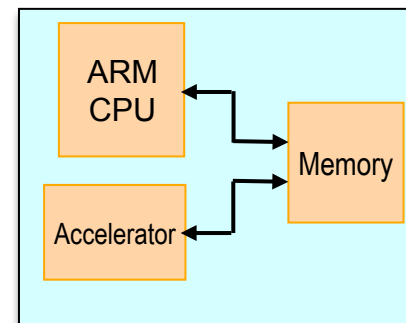
Fabric Datapath



Ex: Static Video Stream

#3

SW Acceleration



Ex: Interactive Image Processing

Use Case #1

Access peripheral configuration registers

Use Case #2

Access datapath configuration registers

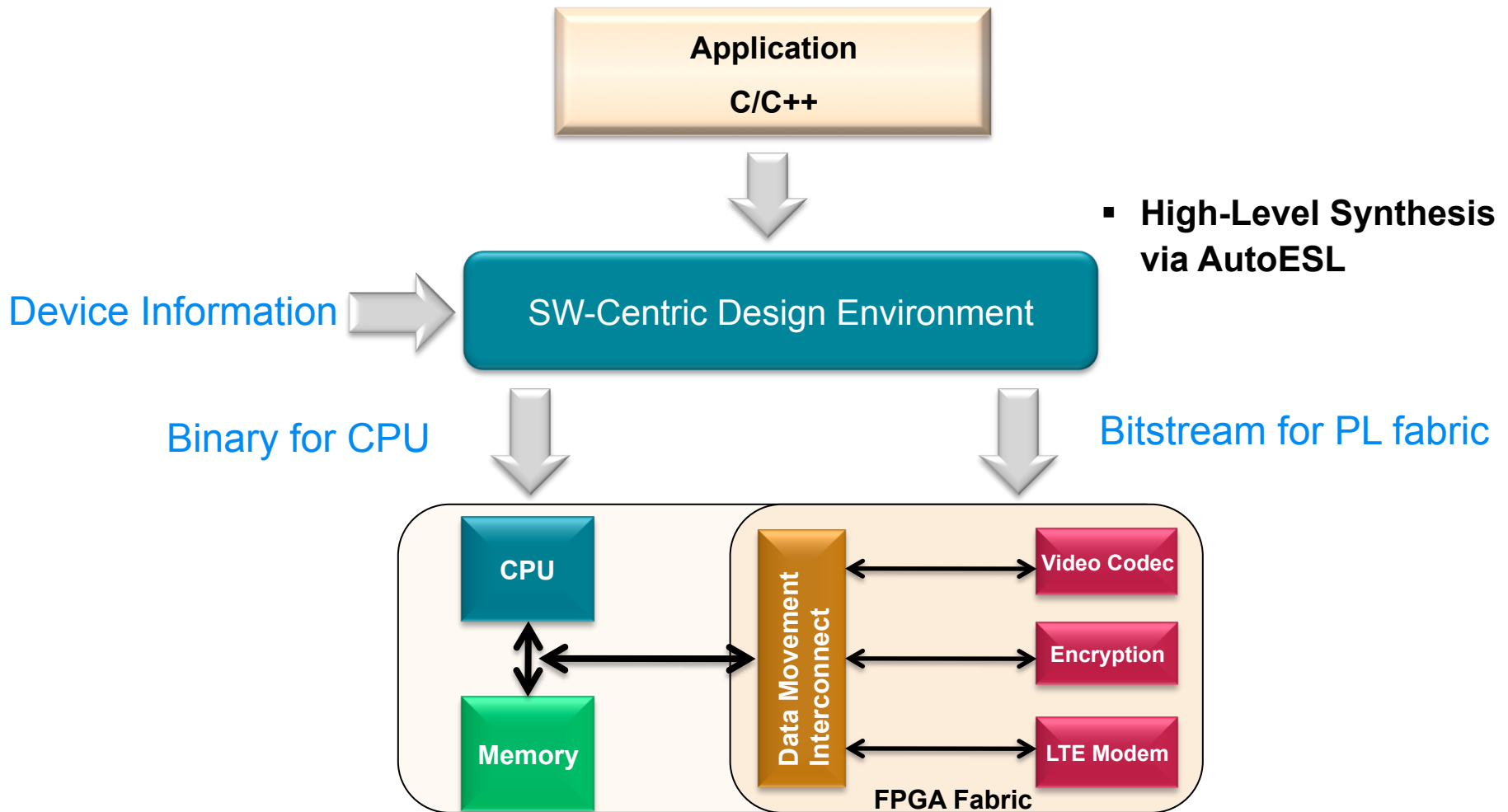
Access datapath memory (coefficient tables)

Use Case #3

Low latency/high bandwidth shared work spaces

Move data between SW and HW domains

Application Programming Using Only C

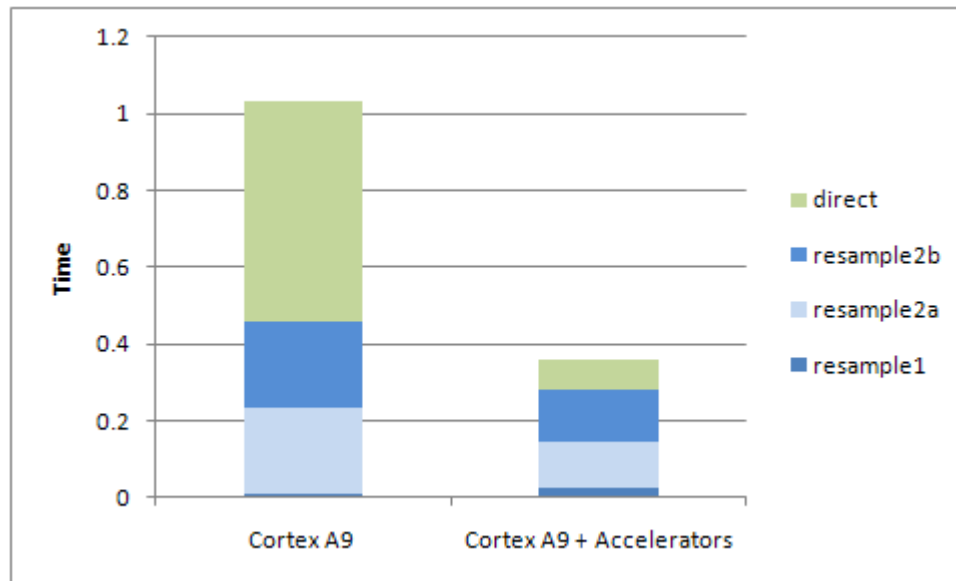


AutoESL Generated Accelerators

C-Based, High-Level Synthesis Tools at Xilinx

Application Example:

Back Projection Algorithm (recreate CT scan images from samples)



gprof

Locate SW hot spot function(s) on ARM

AutoESL

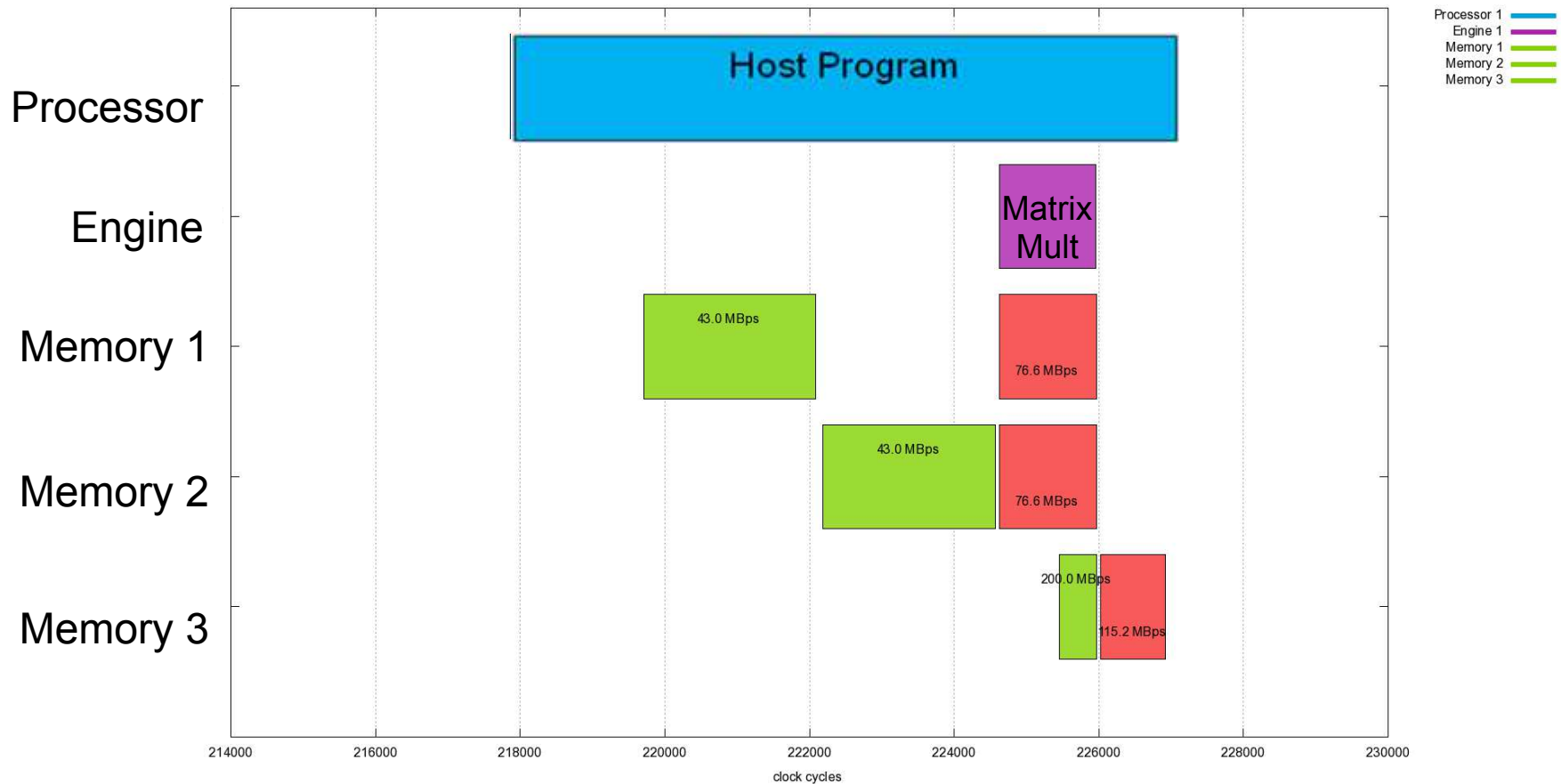
Synthesize hot spot function(s) to HW/PL

- **52 Floating Point Operators @ 200Mhz**
- **Fits in lowest cost Zynq 7010 device**
- **3X Performance vs SW only**

Engineering Insights

Data Movement Gotchas

Event Traces of 16x16 Matrix Multiplier Design #1 Running on PEEP

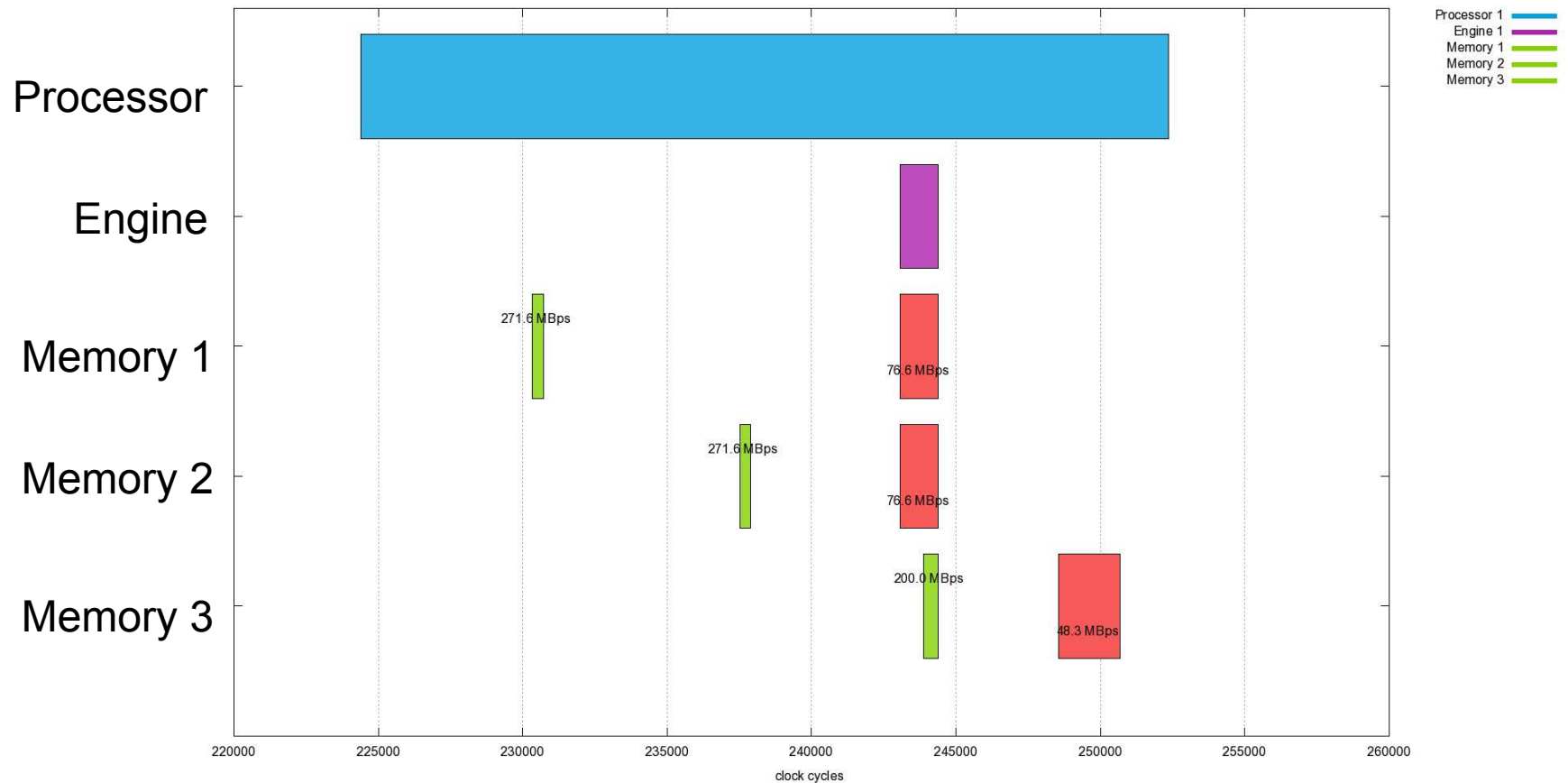


- Using CPU Programmed IO
- IO dominates accelerator compute time

Engineering Insights

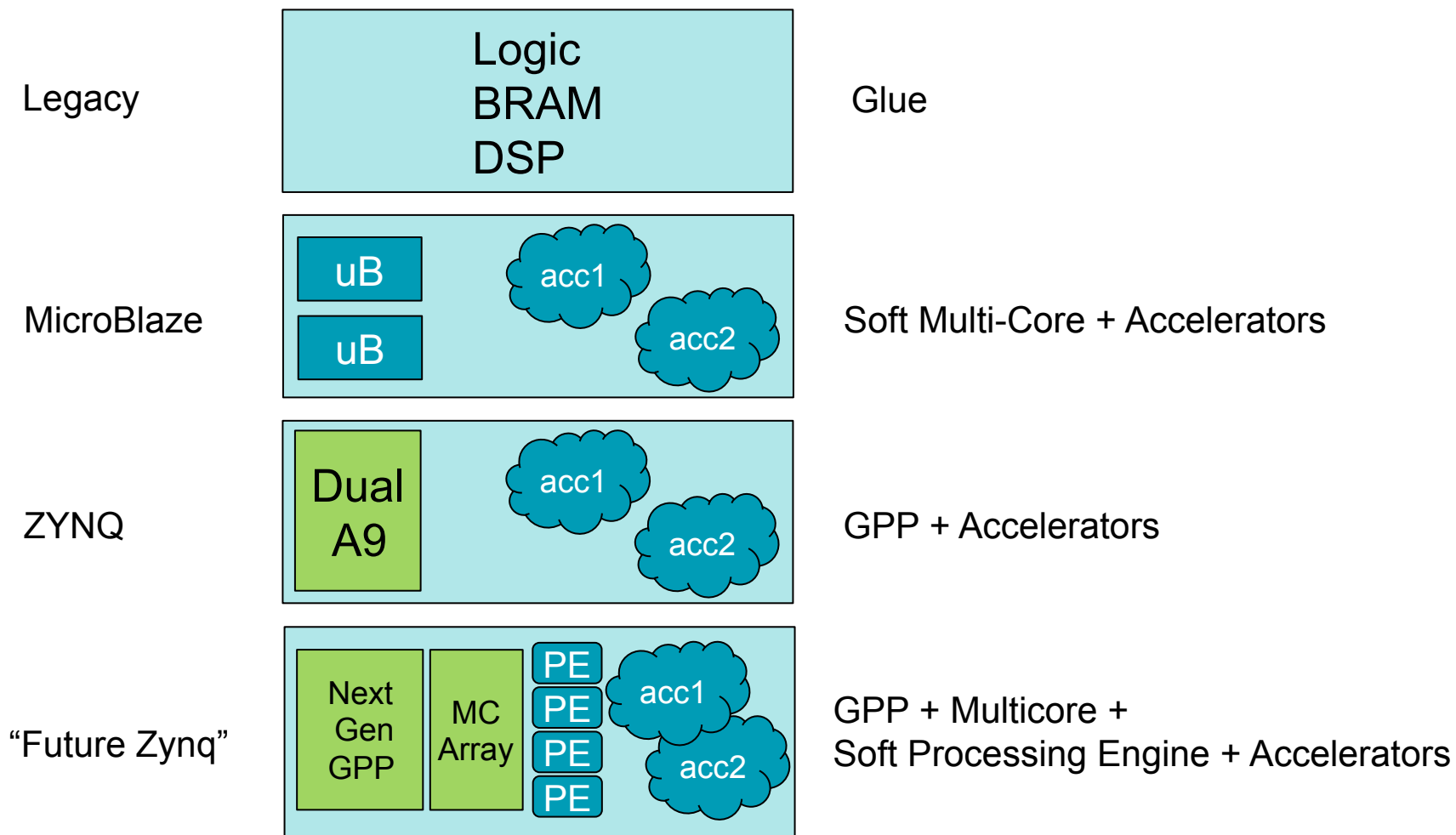
Data Movement Gotchas

Event Traces of 16x16 Matrix Multiplier Design



- Using DMA
- DMA setup time dominates (white space between green bars)

Xilinx Evolution Towards Multicore



Multicore programming models being ported to Zynq

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Summary

- **Zynq SoC Device Family**
with Integrated Programmable Logic
- **\$15 Price Point* / 28nm Fab Process**
- **Microcontroller and Accelerator Use Models**
- **Industry Standard Tools**
(ARM Ecosystem, Android, ISE)
- **Emerging Tools (AutoESL, Multicore)**
- **Emulation platforms in use for prototyping**
- **Available 1H 2012**



Android on Zynq emulation board

Source: iVeia LLC

* High volume price for smallest device and package, slowest speed grade