Fully Integrated Switched-Capacitor DC-DC Conversion

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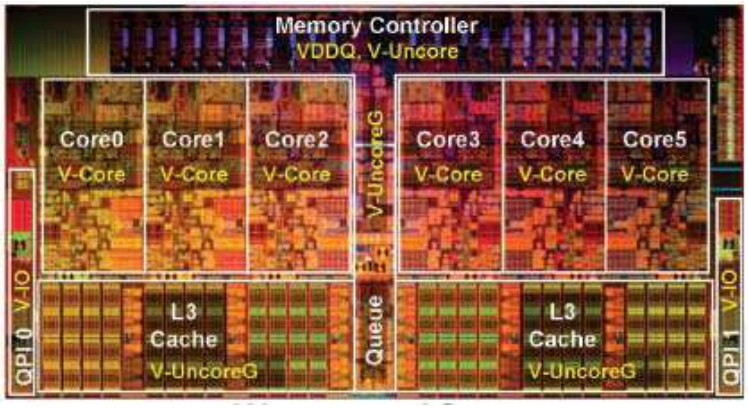
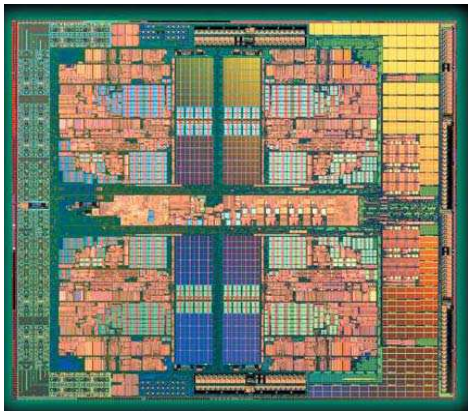
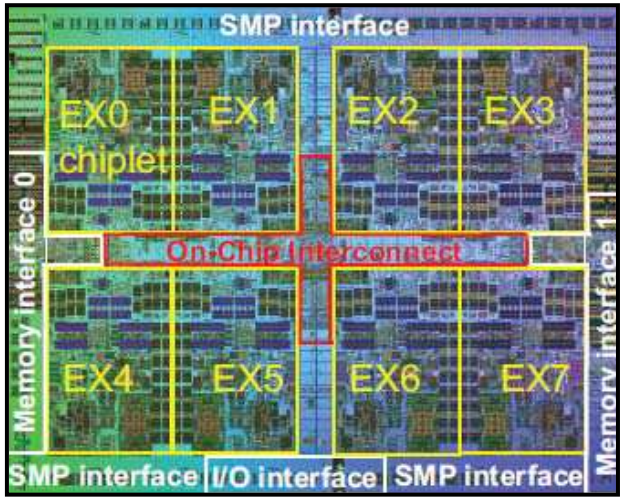
Multi-Core Chips Are Here



Intel Westmere



AMD Phenom

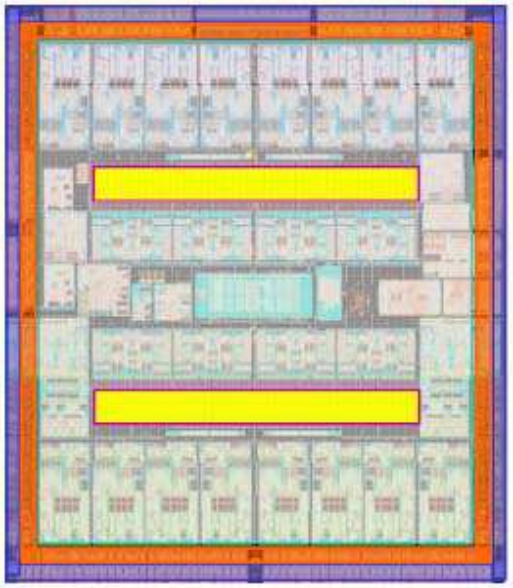


IBM POWER7

Sun Rainbow Falls

Multi-Supply Chips?

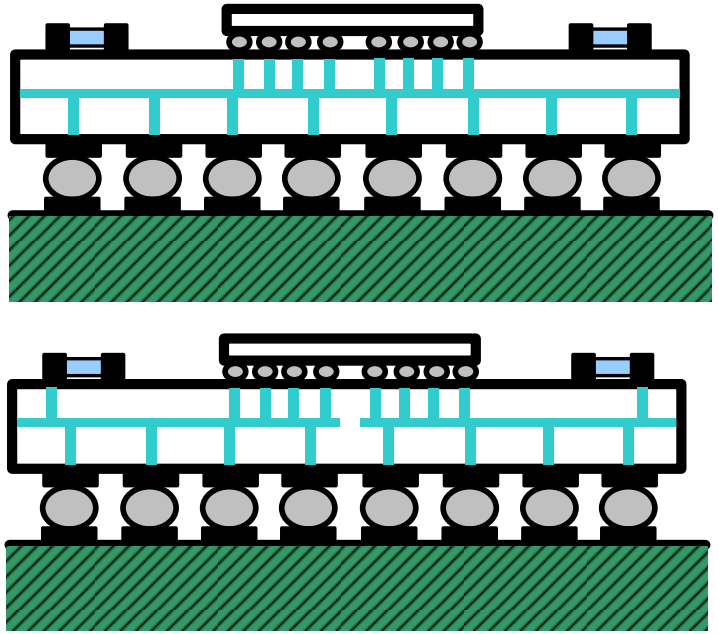
- **Separate supply voltages clearly desirable**
  - Power management, compensate variability, etc.
- **But, true multi-supply adoption slow**
  - Except for power gating

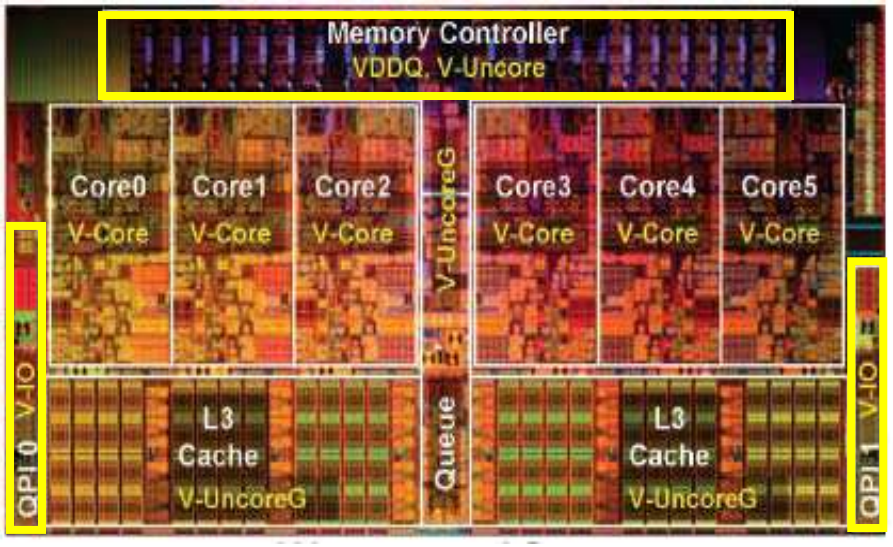


Shin, ISSCC 2010

- **Why not use multiple external converters?**

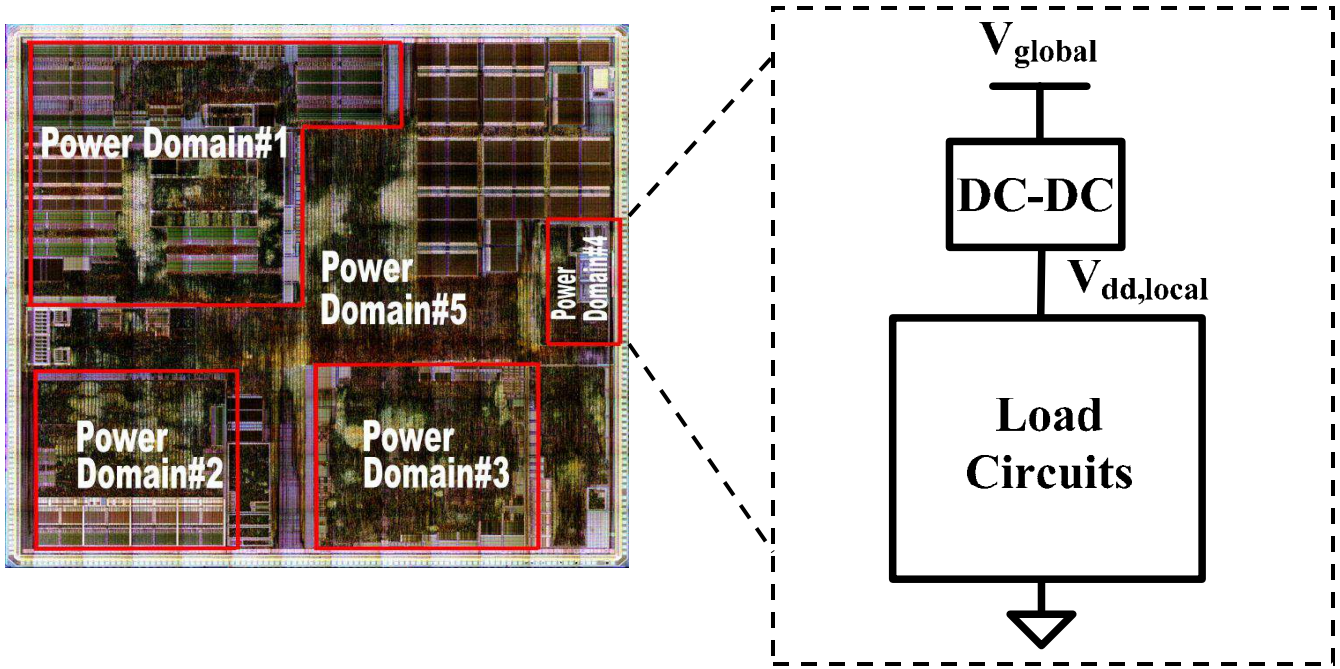
Supply Impedance and Split Planes





- **Supply impedance requirement extremely low**
  - 1V, 100A part → 1mΩ
- **Split power planes bad for impedance**
  - Load and decap isolation
  - Reason I/O's often placed on edges even with flip-chip

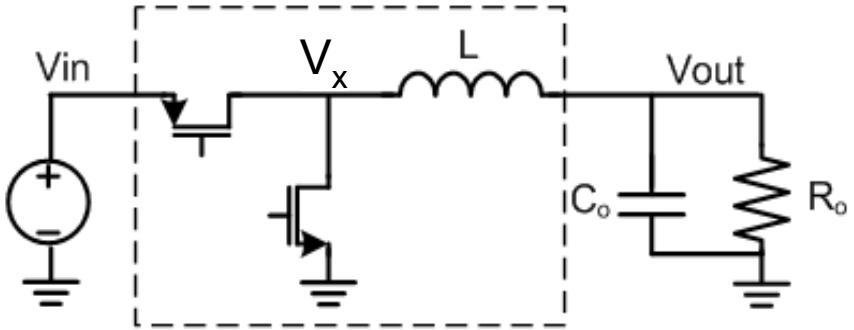
On-Die Voltage Conversion

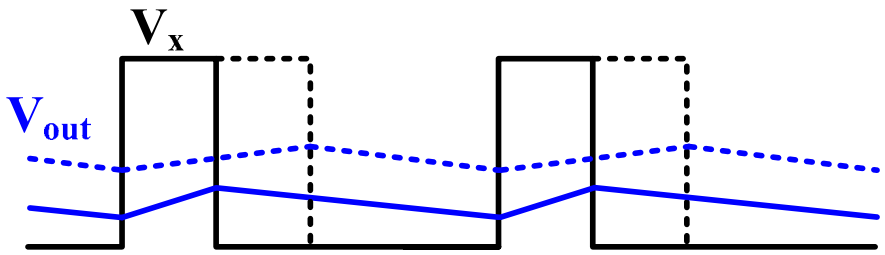


- **Enables single, low-impedance global input voltage**
- **Key challenge: fully integrated DC-DC**
  - Energy storage must be integrated on-die too

Switching Converter Options

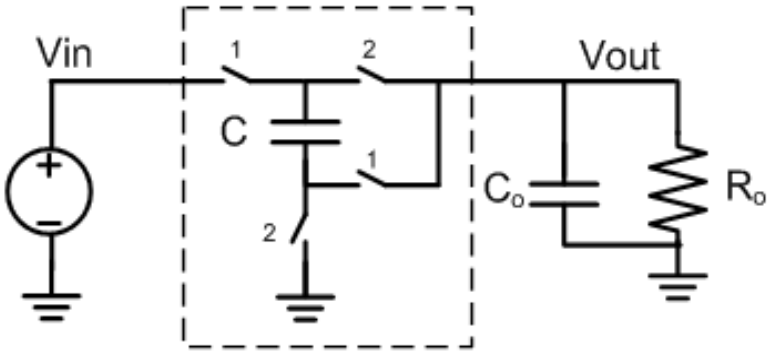
Inductor:

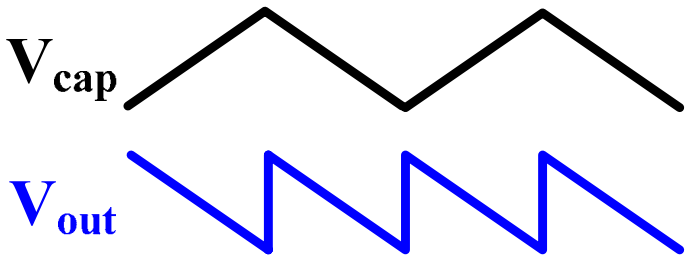




- Conversion ratio set by duty cycle
- Very popular for off-chip converters

Capacitor:

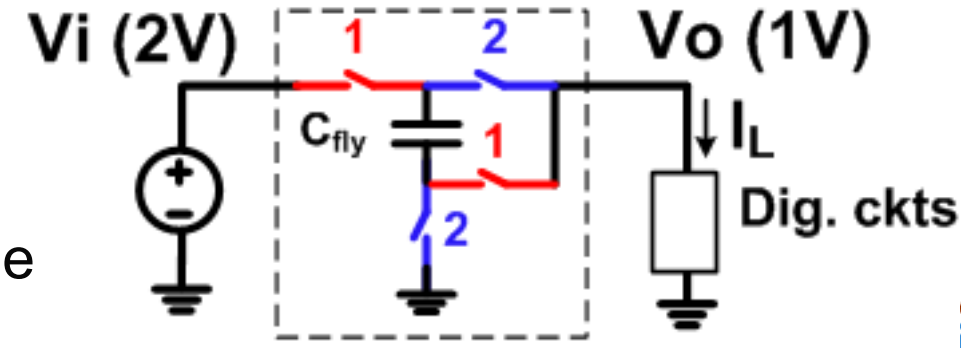




- Conversion ratio set by topology
- Many perceived disadvantages

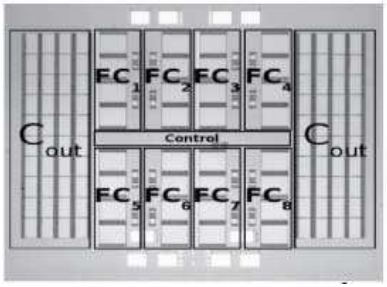
So Why Switched-Capacitor (SC)?

- **Key motivation: integration with <u>low cost</u>**
  - Dense, high-quality capacitance widely available
  - (Development of on-die magnetics can be leveraged for SC converters too)



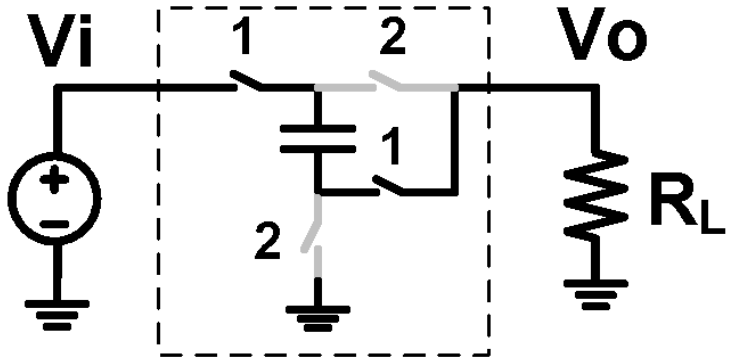
- **Integrated SC design can mitigate perceived downsides**
  - Component count no longer critical
- **What is achievable efficiency, power density?**

Selected Previous Designs

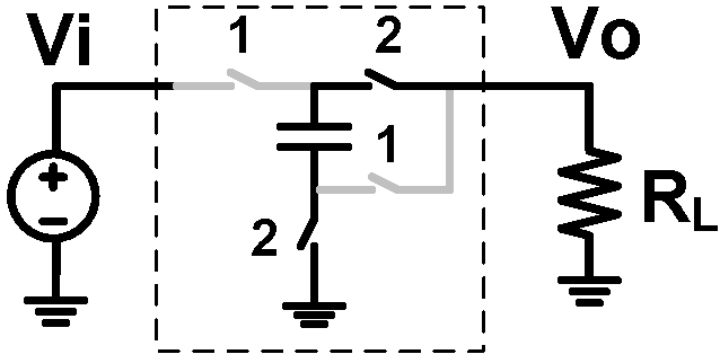
Work	Breussegem, VLSI 09	Somasekhar, VLSI 09
Technology	130nm Bulk	32nm Bulk
Topology	2/1 step-up	2/1 step-up
Interleaved Phases	16	32
Converter Area (mm^2)	2.25	6.678×10^{-3}
Power density @ η_{max}	0.002 W/mm^2	1.123 W/mm^2
Efficiency (η_{max})	82%	60%
		

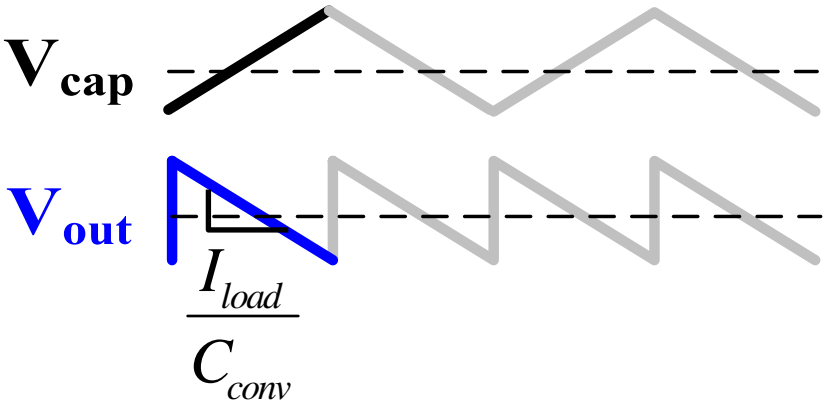
Review: SC Basics

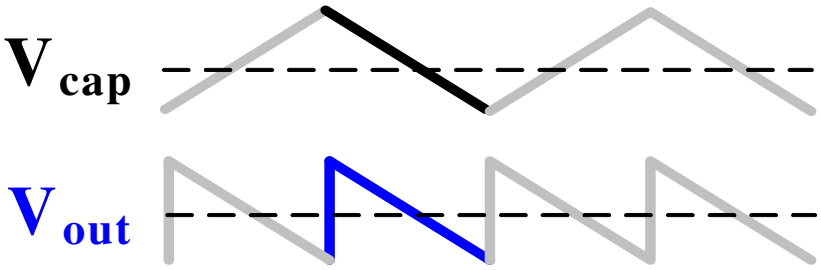
Phase 1:



Phase 2:

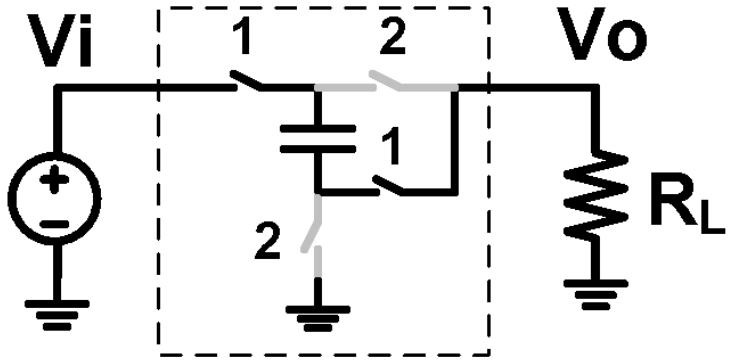




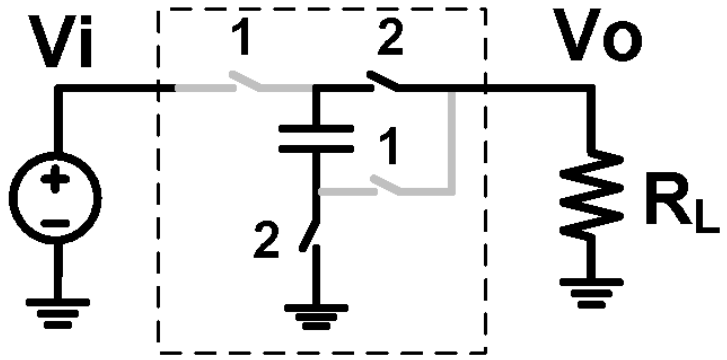


Switched Capacitor (SC) Basics

Phase 1:

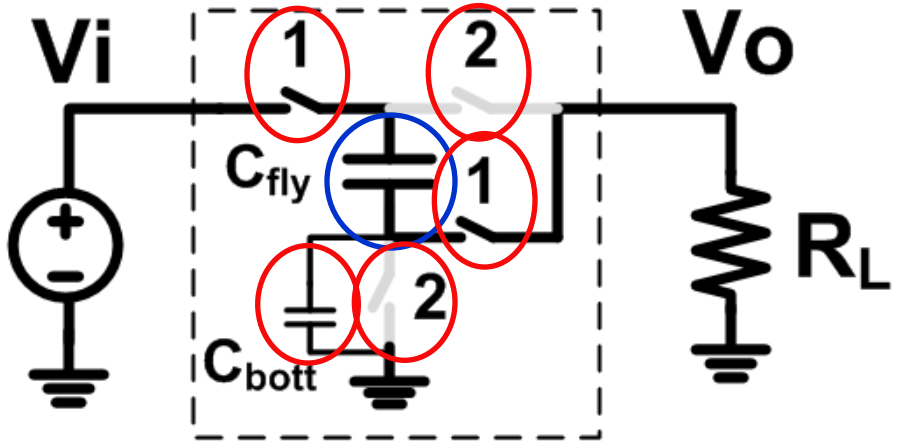


Phase 2:



- Conversion ratio set by topology
- Works in other direction too
  - Step-up: reverse V_i, V_o

SC Converter Loss Mechanisms

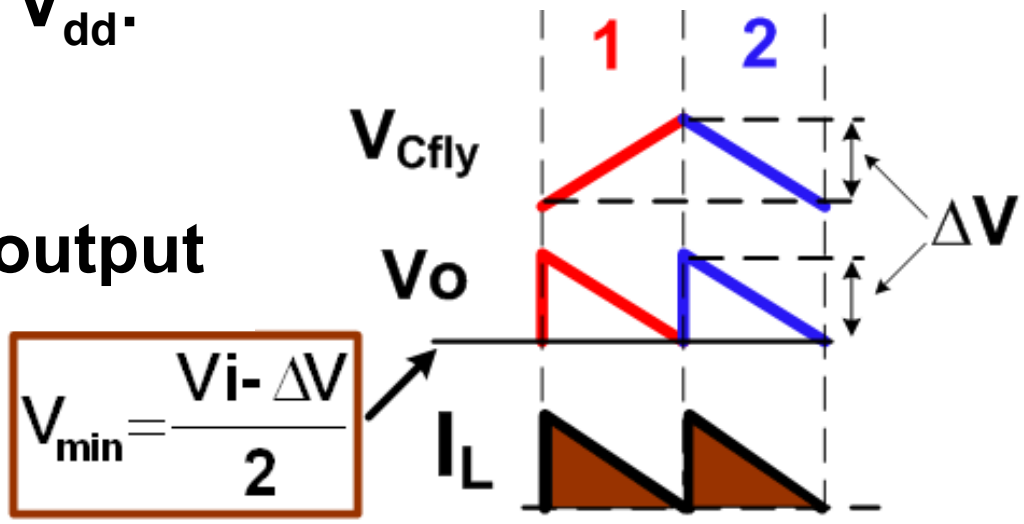


- **Intrinsic loss**
  - Fundamental to converter operation
- **Switch/parasitic loss**
  - Non-idealities of the capacitor(s) and switches

SC Converter Loss with Digital Loads

- **Gate delay depends on V_{dd}:**
  - Performance set by V_{min}
- **SC converter effective output resistance (for V_{min}):**

$$R_{eff,Csw} = \frac{1}{M_{conv,cap} C_{conv} f_{sw}}$$



- **But, load also draws "extra" current when $V_{dd} > V_{min}$**
  - This power is wasted since it doesn't improve performance
- **Ripple leads to extra loss:**

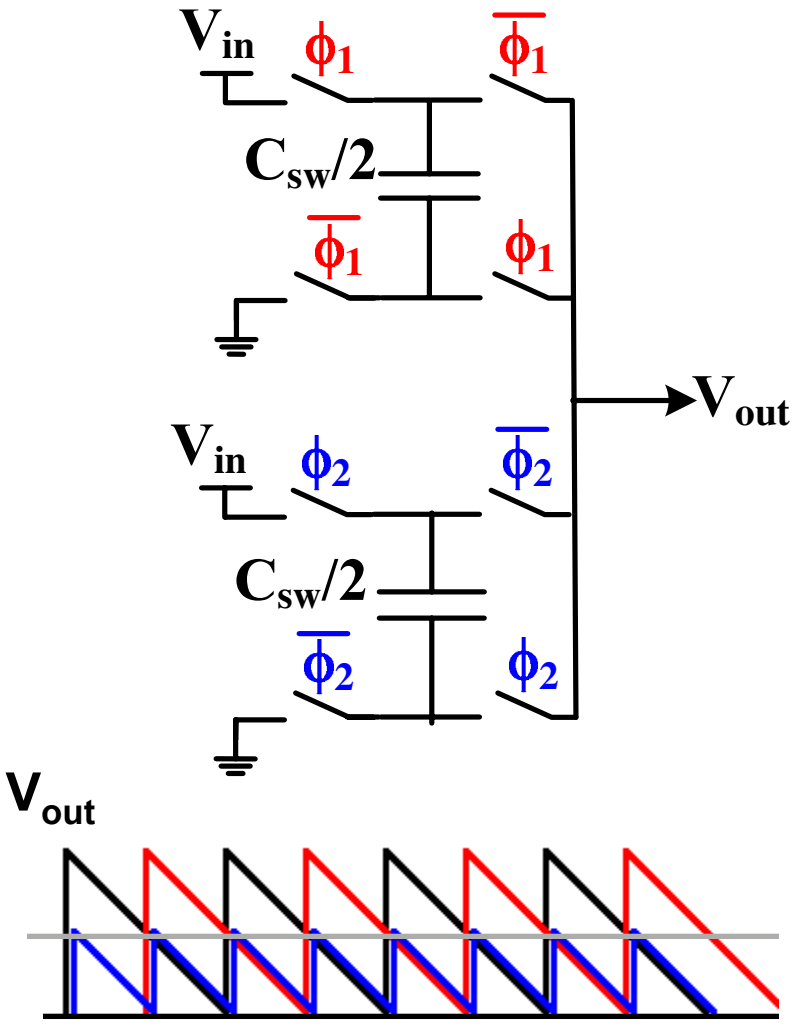
$$P_{Reff} = \frac{2 I_{load}^2}{M_{conv,cap} C_{conv} f_{sw}}$$

Interleaving

- **Good news: interleaving reduces ripple**
  - But leaves V_{min} unchanged
- **With N_{int} interleaved converters:**

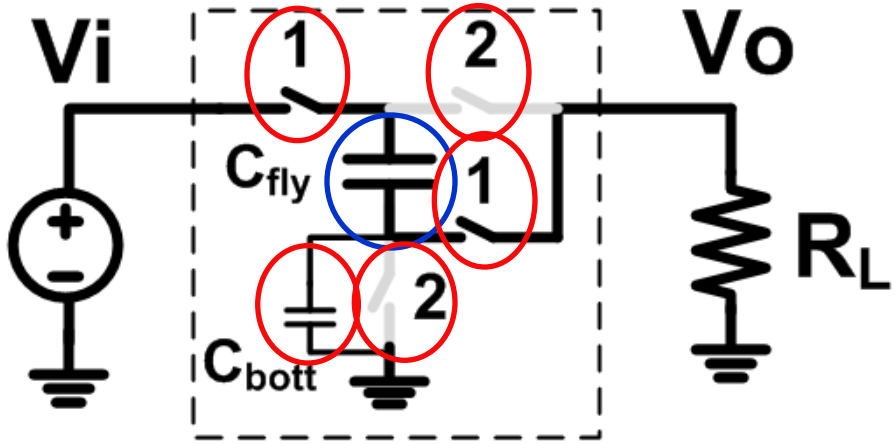
$$P_{Reff} = \left(1 + \frac{1}{N_{\text{int}}}\right) \frac{I_{load}^2}{M_{conv,cap} C_{conv} f_{sw}}$$

- **Ripple minor for ~16+ way interleaving**



D. Ma, "Robust Multiple-Phase Switched-Capacitor DC-DC with Digital Interleaving Regulation Scheme," *ISLPED* 2006.

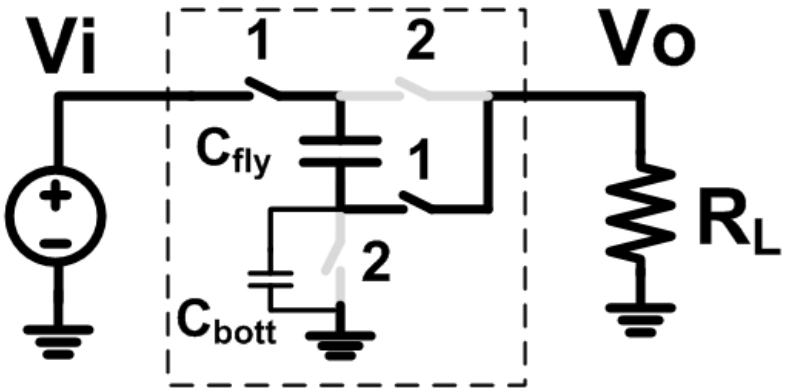
Efficiency Optimization

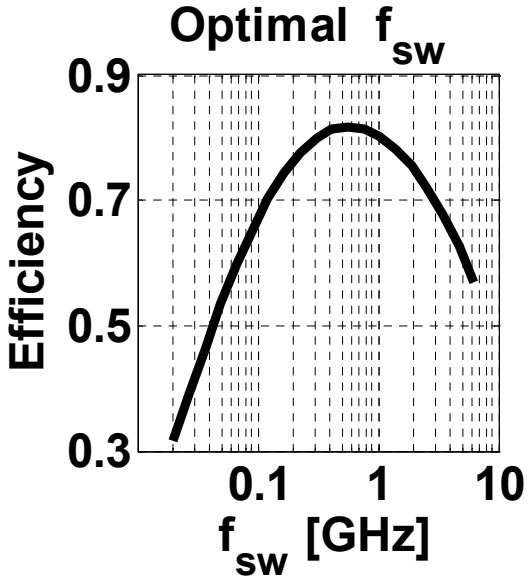


- **Intrinsic loss**
  - Reduced by ↑ C density
  - Reduced by ↑ f_{sw}
- **Switch/parasitic loss**
  - Reduced by ↑ switch f_T
  - Increased by ↑ f_{sw}

- **Efficiency optimization: choose f_{sw} and W_{sw} to balance loss terms**

Loss Terms Detail





Sw.-cap R:

$$P_{Reff} \approx \frac{I_{load}^2}{M_{ccap} C_{conv} f_{sw}}$$

Bottom plate:

$$P_{Cbot} = M_{bott} C_{bot} V_{out}^2 f_{sw}$$

Switch R:

$$P_{Rsw} = \frac{M_{sw} I_{load}^2 R_{on}}{W_{sw}}$$

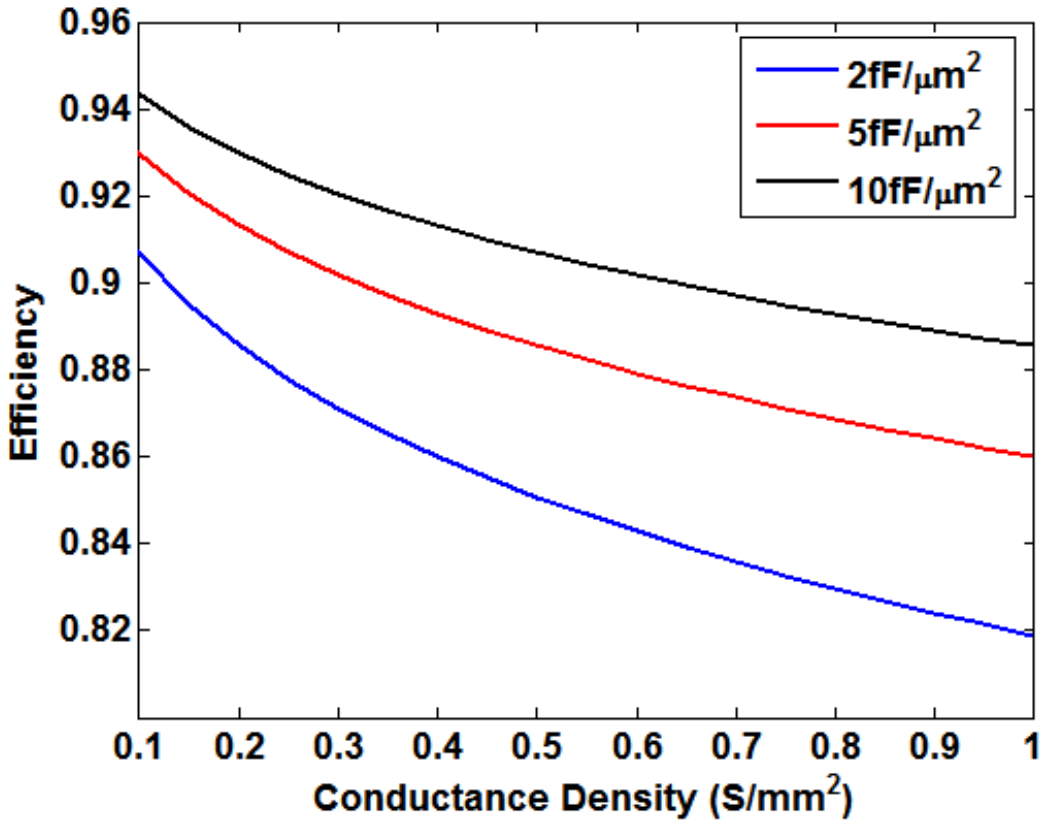
Gate loss:

$$P_{Csw} = W_{sw} C_{sw} V_{sw}^2 f_{sw}$$

Optimized Efficiency

- **Ignoring bottom-plate:**

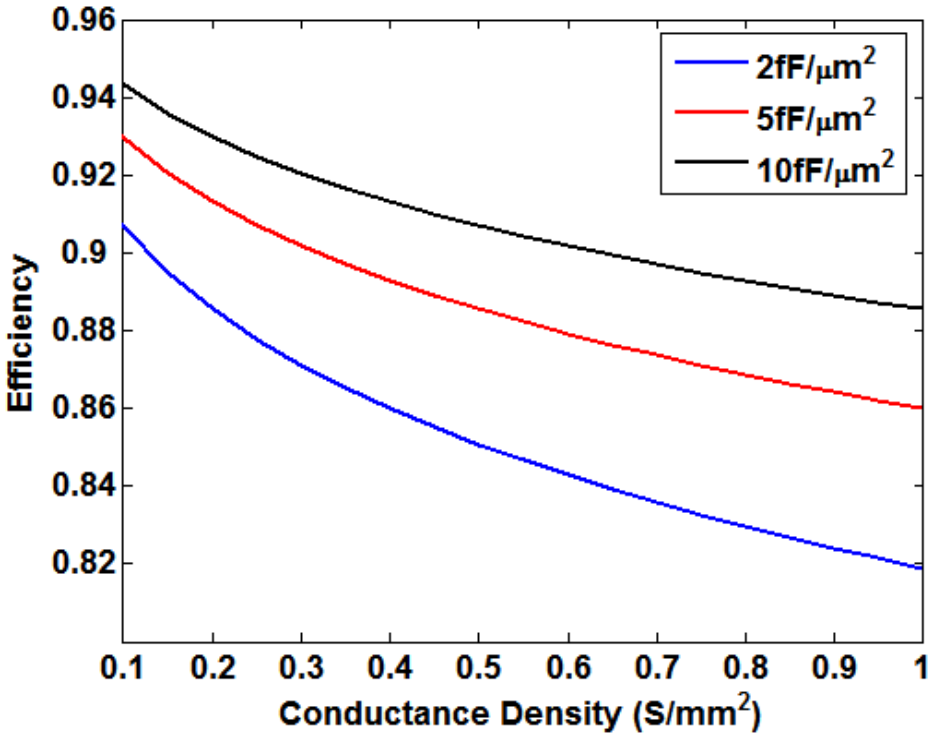
$$\frac{P_{loss}}{P_{load}} = 3 \cdot \sqrt[3]{M_{conv,sw} M_{conv,cap} \frac{V_{sw}^2 R_{on} C_{sw}}{V_{out}^2 R_L C_{conv}}}$$



Optimized Efficiency cont'd

- **Efficiency set by *conductance* density**
  - I.e., (I_{load}/V_{out}) / Conv. Area
  - (Equivalent to power density for given V_{out})

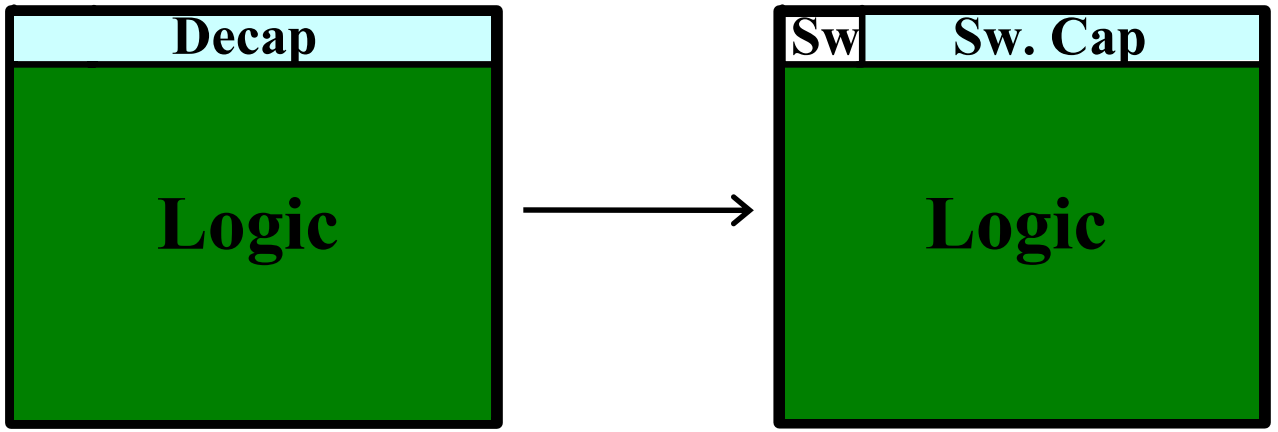
$$\frac{P_{loss}}{P_{load}} = 3 \cdot \sqrt[3]{M_{sw} M_{cap} \frac{V_{sw}^2 R_{on} C_{sw}}{V_{out}^2 R_L C_{conv}}}$$



- **Typical numbers (1V)**
  - Mobile device: ~0.1 S/mm²
  - Processor: ~1 S/mm²

- **Efficiency trades off with converter area overhead.**

Side Note



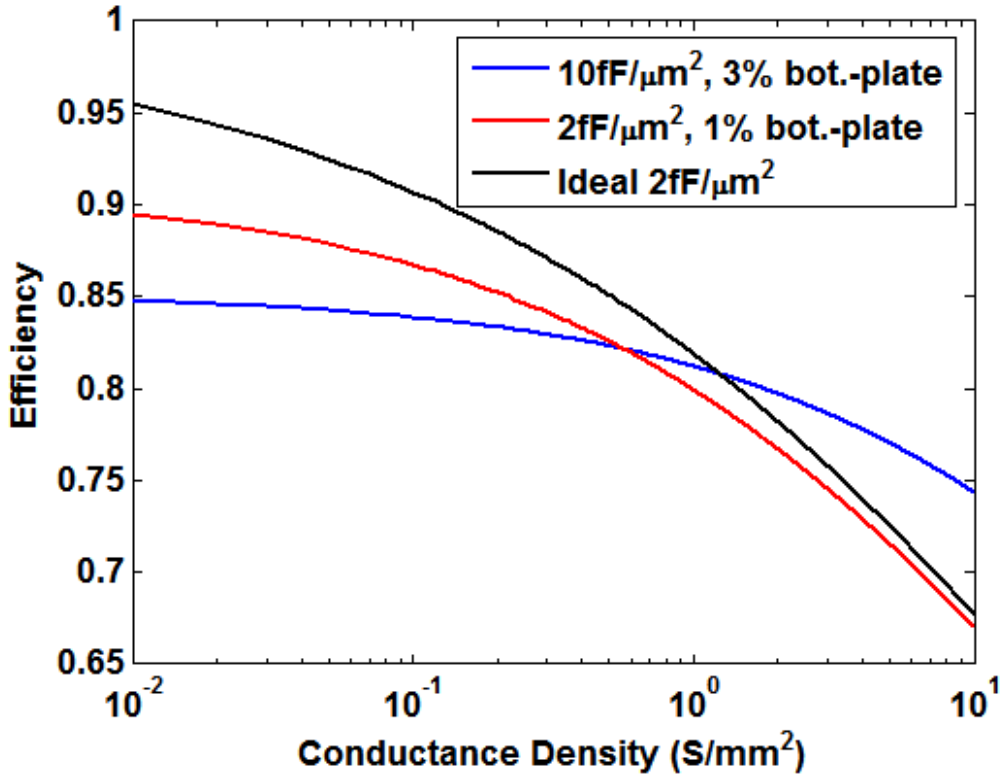
- **Explicit decoupling capacitance usually required for supply integrity**

- **Can largely replace decap with converter**
  - In order to fit, converter needs to deliver ~10X higher density than load

Impact of Bottom-Plate

- With $C_{bot} = k_{bot} C_{conv}$:

$$\frac{P_{loss}}{P_{load}} = 2\sqrt{M_{cap} M_{bott} k_{bot}} + 2\sqrt{\left(M_{sw} \sqrt{\frac{M_{cap}}{M_{bott} k_{bot}}} \right) \frac{V_{sw}^2 R_{on} C_{sw}}{V_{out}^2 R_L C_{conv}}}$$

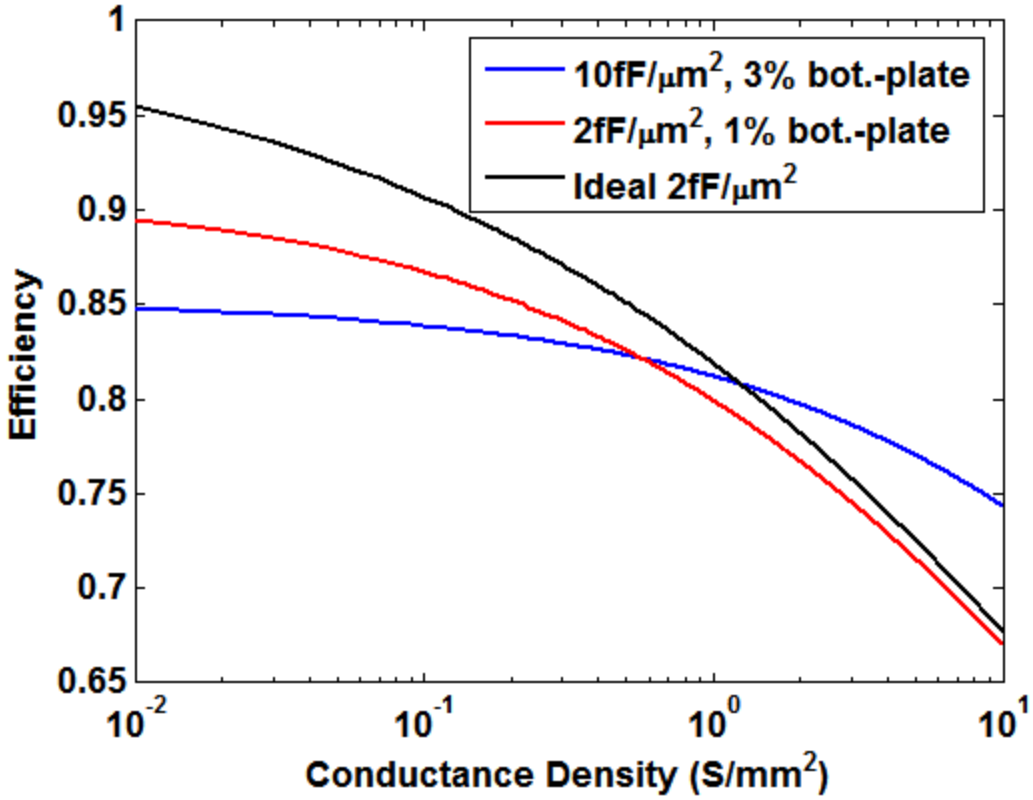


Impact of Bottom-Plate cont'd

- **Bottom plate sets min. loss:**
  - E.g., 2:1 step-down, 1% bottom plate → 10% loss

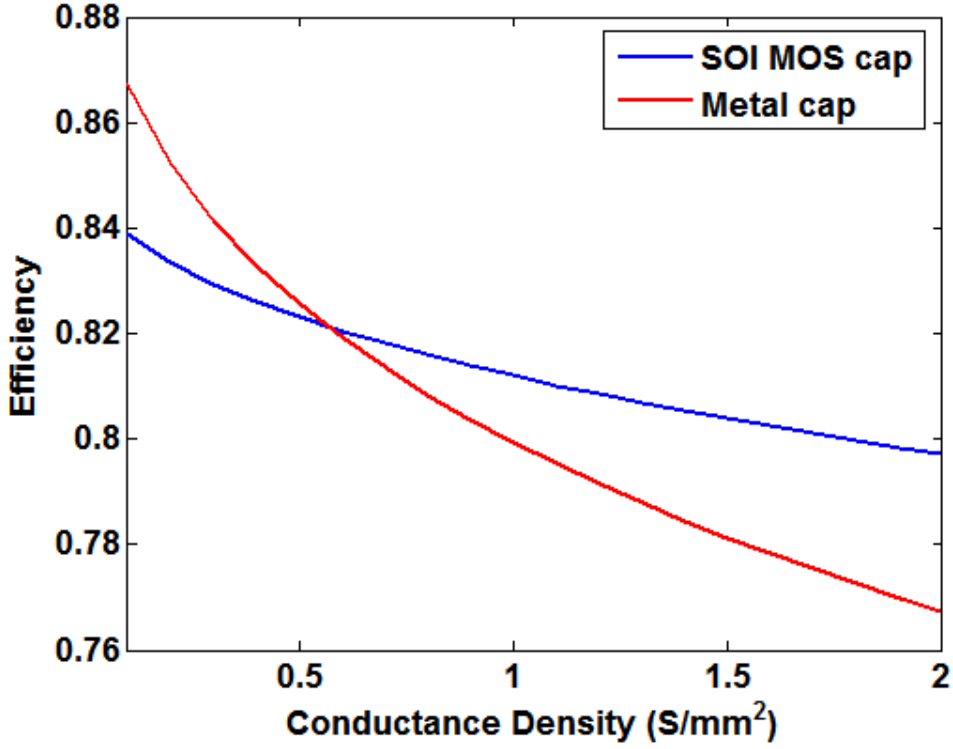
$$P_{loss} / P_{load} \approx 2\sqrt{M_{cap} M_{bott} k_{bot}}$$

- **In the limit of low power density:**
- **Converter area does not affect efficiency**
- **Low parasitics more important than cap. density**



Achievable Performance

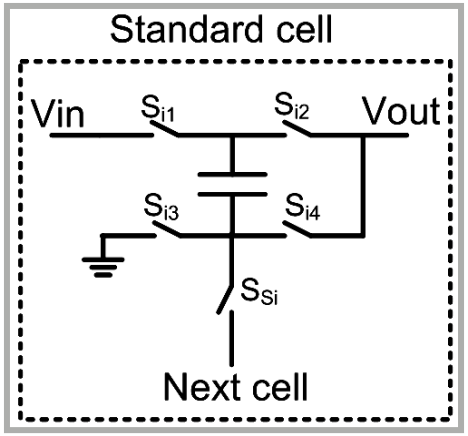
- **45nm, 2:1 converter:**
  - 75% - 80% efficiency at 1W/mm^2
  - Even in standard CMOS
- **Looks promising**
  - Reminder: mobile device ~0.1W/mm^2
  - But, only checked one conversion ratio so far…

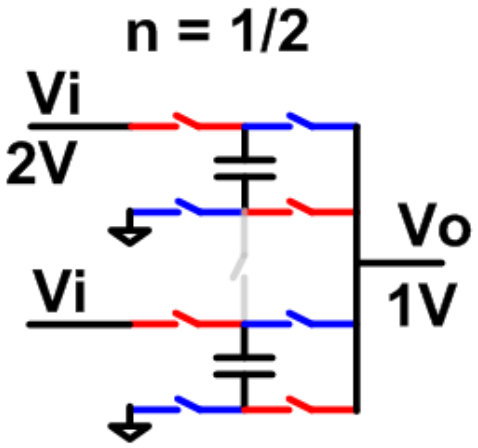


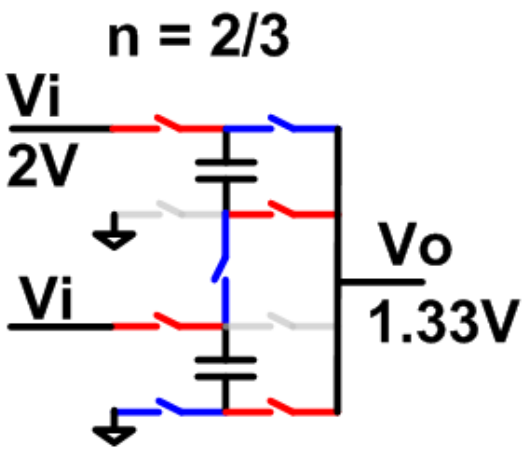
- **How to handle variable voltages?**

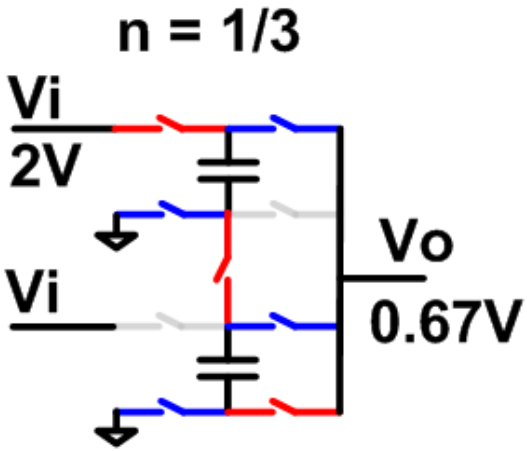
SC "Standard Cell" Converter

- **Integrated capacitors/switches easily partitioned**
- **"Standard cell" configuration sets conversion ratio**



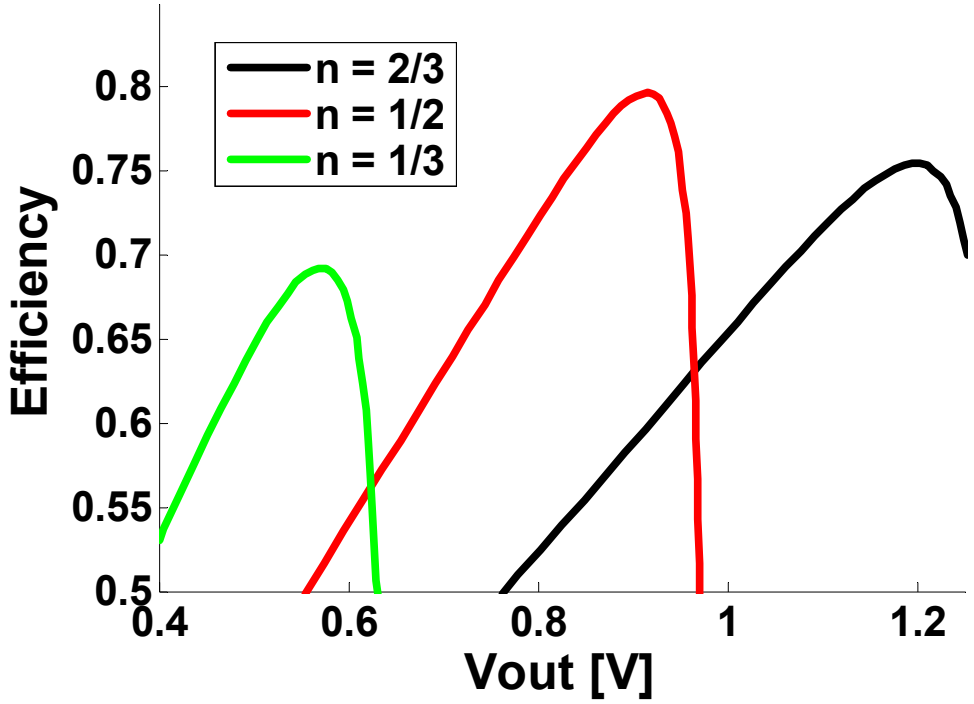






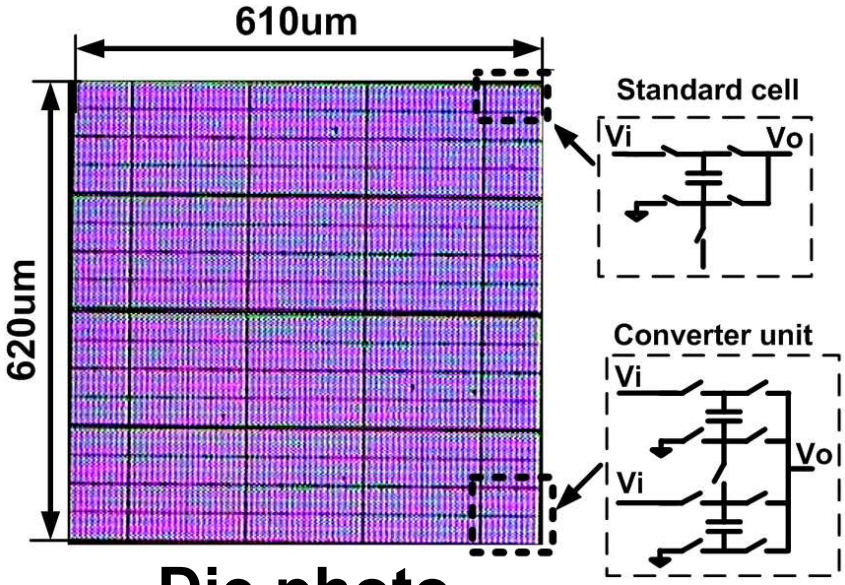
Efficiency vs. Conversion Ratio

- **Change topology, W_{sw}, and f_{sw}**
  - $R_{out} \sim 1/(C f_{sw})$
  - Just like linear regulator
- **Probably need only ~4-5 topologies**
  - Clustered around 2:1
  - Watch out for switch drivers

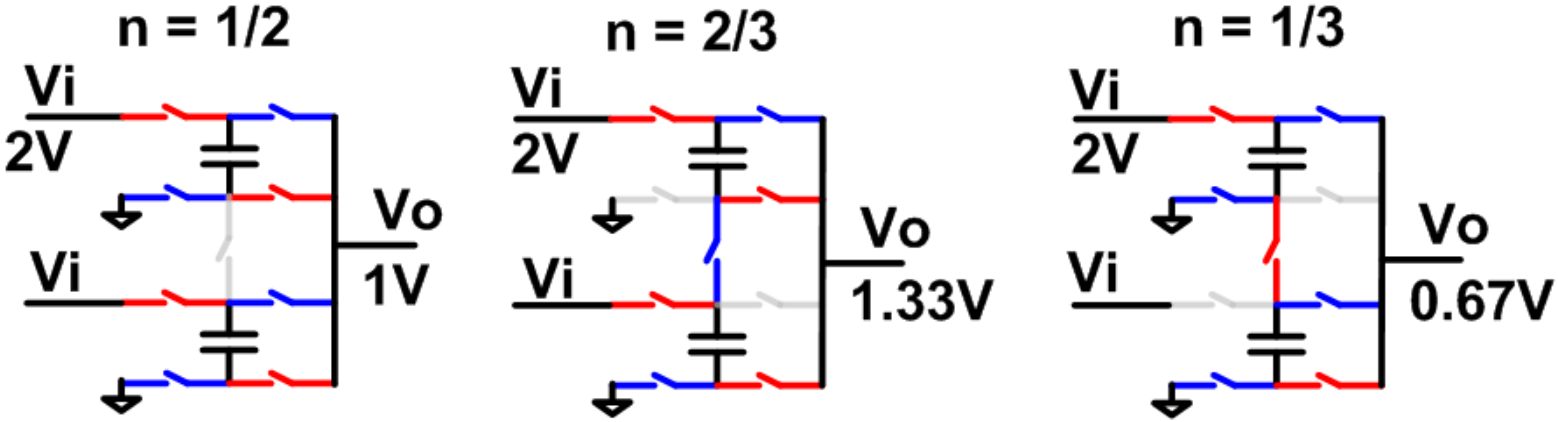


Prototype

- Implemented in 32nm SOI test-chip (w/AMD)
- MOS flying capacitors, 32-way interleaved
- Supports 0.6V ~ 1.2V from 2V input

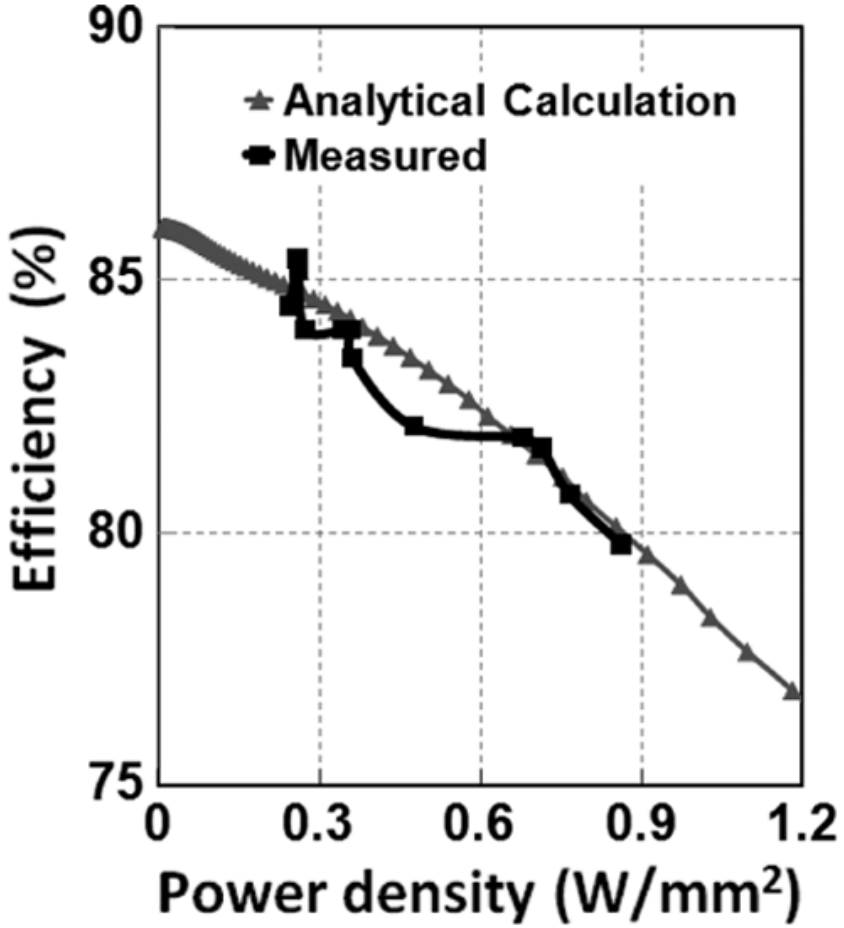


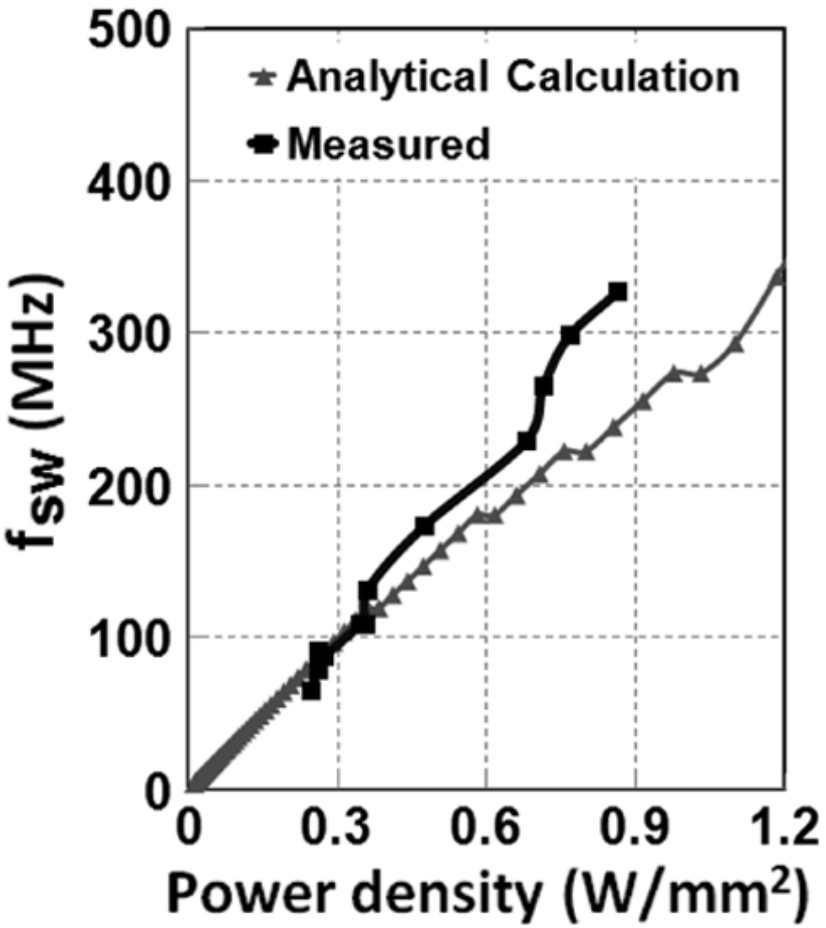
Die photo



H.-P. Le, S. Sanders, and E. Alon, "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters," *JSSC* Sept 2011.

Measured Efficiency vs. Power Density

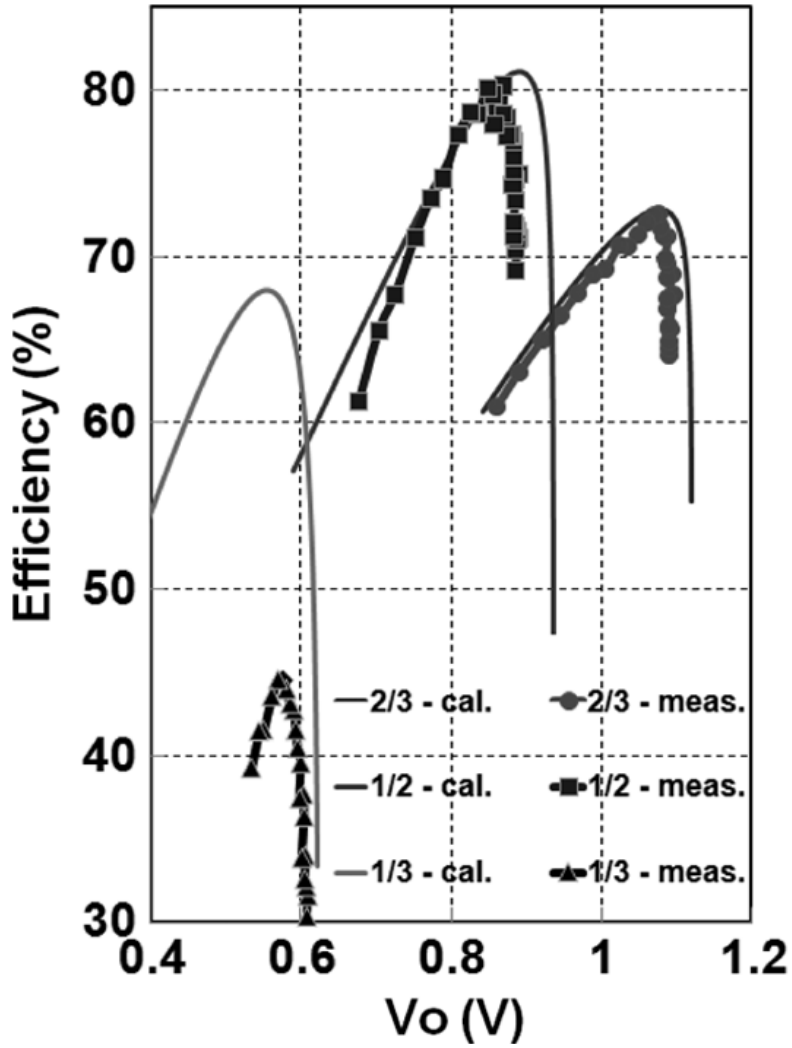




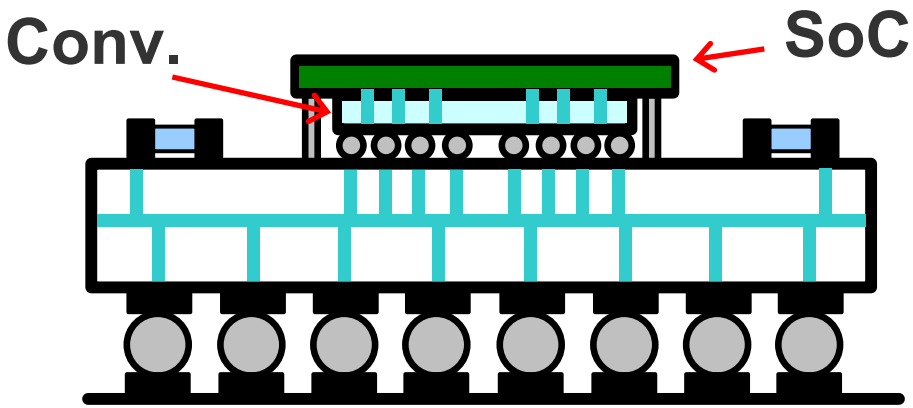
- Measured with n = 1/2 (Vi = 2V, Vo ≈ 0.88V)
- Matches analysis: ~80% efficiency @ 0.86 W/mm²

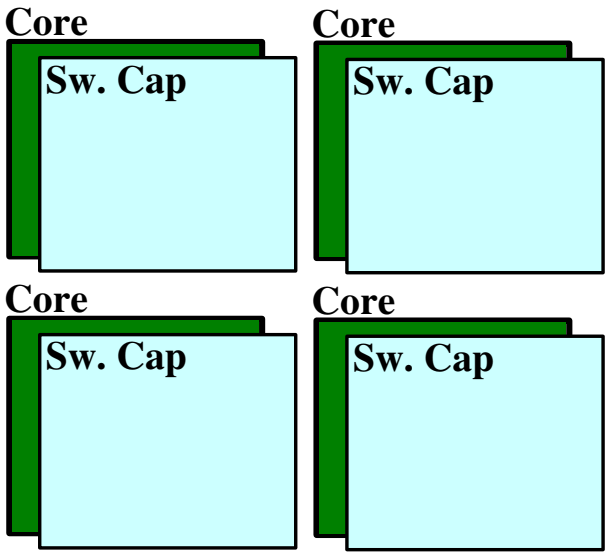
Measured Efficiency vs. Topologies

- **All three topologies functional**
  - (3:1 efficiency limited by breakdown)
- **Efficiency still >70% for 0.75V – 1.15V Vo with 2V Vin**



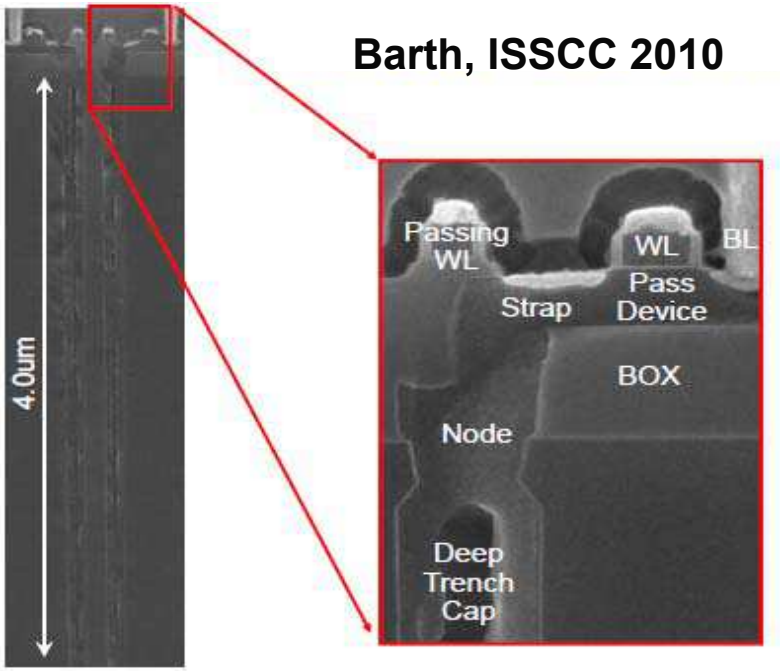
Looking Forward: Leveraging 2.5/3D Integration

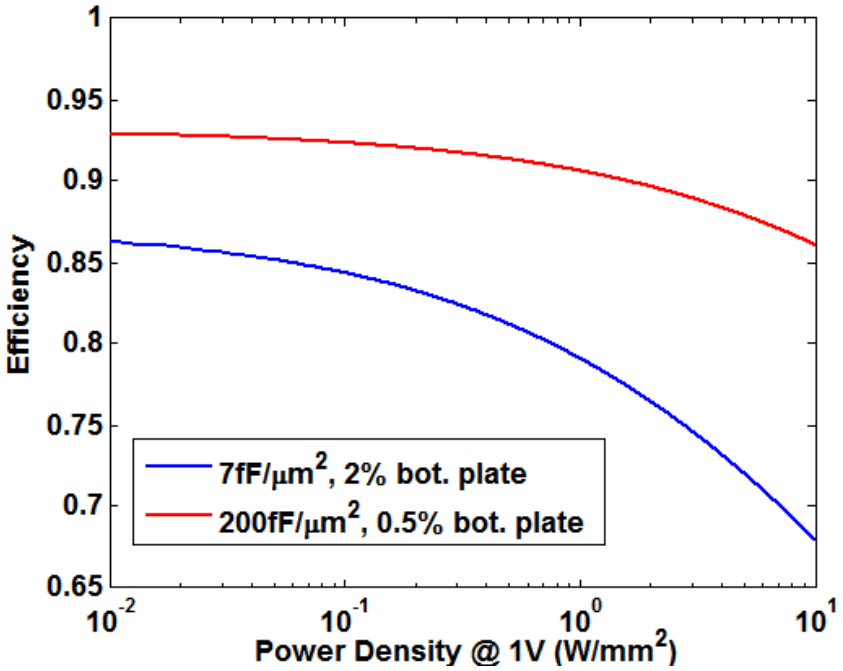




- **Enables converter to use entire area over core**
  - Mitigates efficiency vs. power density tradeoff
- **Converter die can use older, lower-cost technology**
  - While still meeting efficiency & density requirements

Looking Forward: Dense Capacitors





- **Dense capacitors already exist for DRAM/eDRAM**
  - IBM eDRAM 2:1 converter*: 90% efficiency @ 2.3A/mm^2
- **Opportunity to further leverage stacked DRAM**

*L. Chang *et al.*, "A Fully Integrated Switched-Capacitor 2:1 Voltage Converter with Regulation Capability and 90% Efficiency at 2.3A/mm^2," *IEEE Symposium on VLSI Circuits*, Jun. 2010

Summary

- **Clear need for fully-integrated DC-DC converters**
  - Multiple off-chip supplies costly, degrade impedance
- **Switched-capacitor converters in standard CMOS can achieve:**
  - In 2:1: ~**80% efficiency @ 0.86 W/mm^2**
  - **>70% efficiency** for **Vo from ~0.75V to 1.15V** with **Vi = 2V**
- **Low-cost technologies to enable even higher densities, efficiencies already exist**

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