Demonstration of a High Speed 4-Channel Integrated Silicon Photonics WDM Link with Hybrid Silicon Lasers

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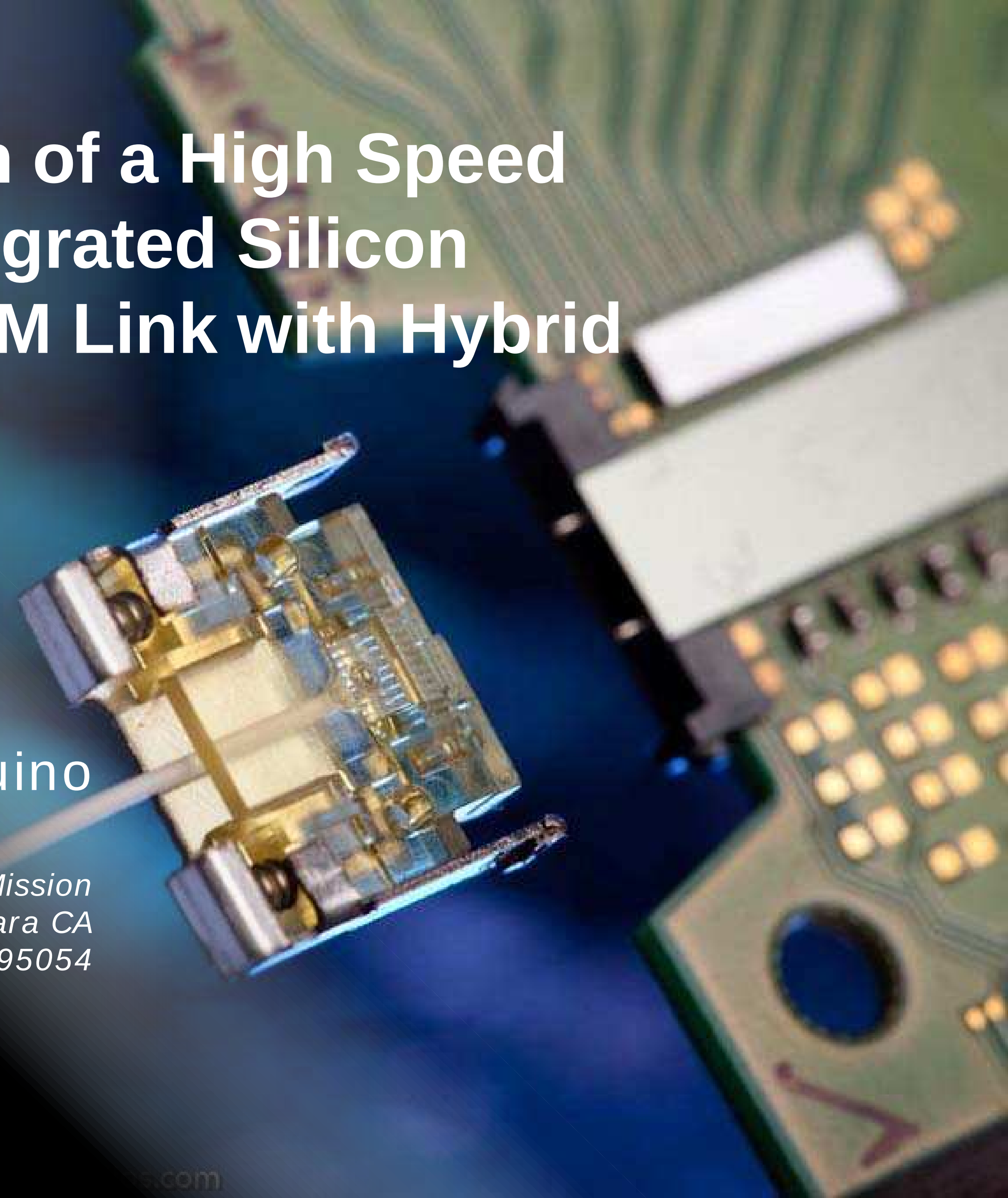

Outline

- Introduction
- Previous Results
- WDM Silicon Photonics Link
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Previous Silicon Photonics Results

Lasers

1^{st} Continuous Wave Silicon Raman Laser (Feb. ‘05)

Hybrid Silicon Laser (Sept. ‘06)

Data Encoders

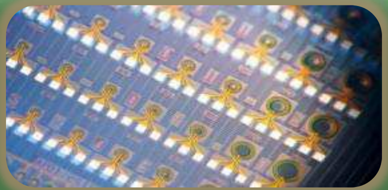
Silicon Modulators
1GHz (Feb ‘04)
10 Gbps (Apr ‘05)
40 Gbps (July ’07)

Basic Light Routing

Waveguides, multiplexers, demultiplexers, couplers…

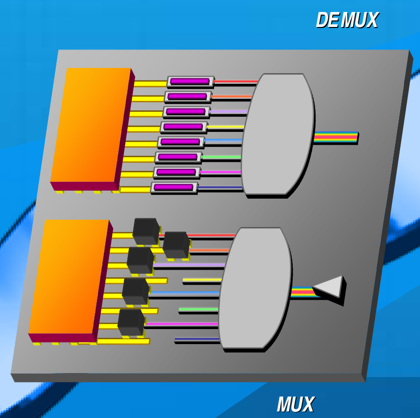
Light detectors

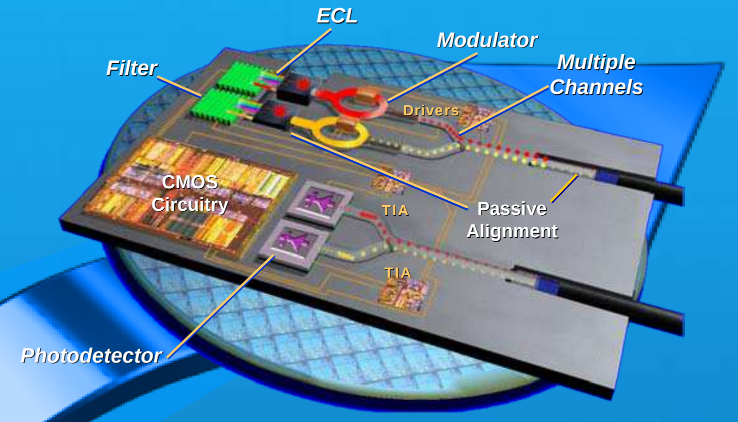
40 Gbps PIN Photodetectors (Aug. ’07)



340 GHz Gain*BW Avalanche Photo-detector (Dec ’08)

Integration Vision





FUTURE
Monolithic?

Level of integration Determined by Application/ cost

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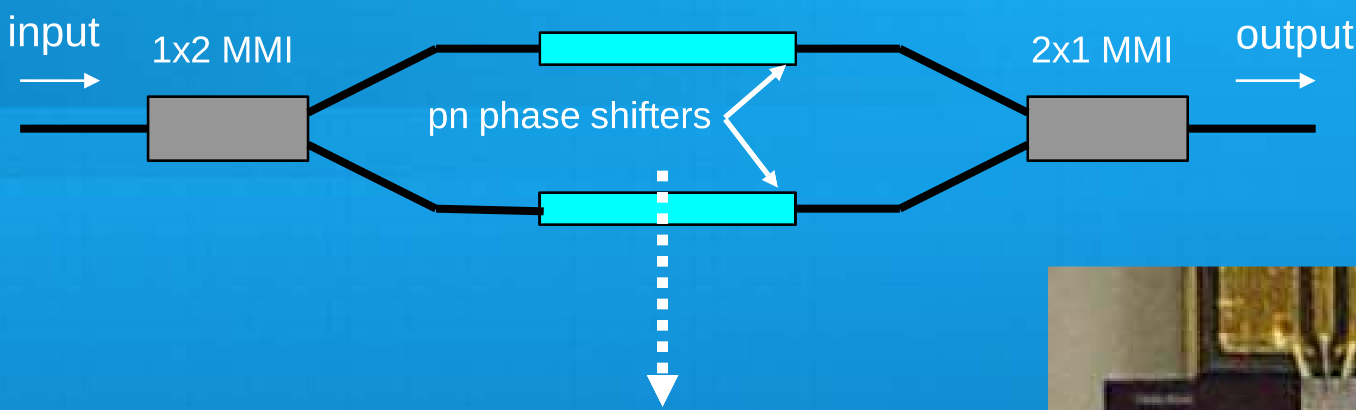
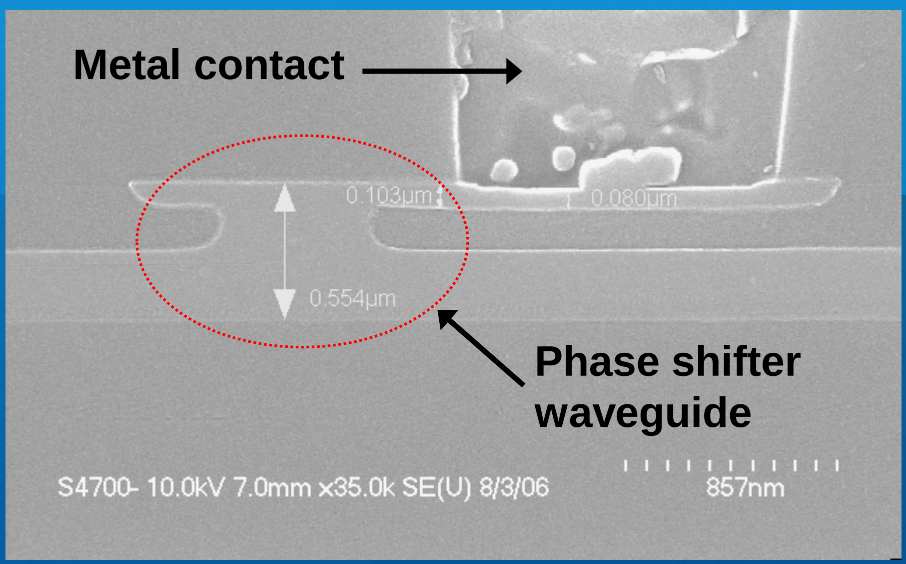
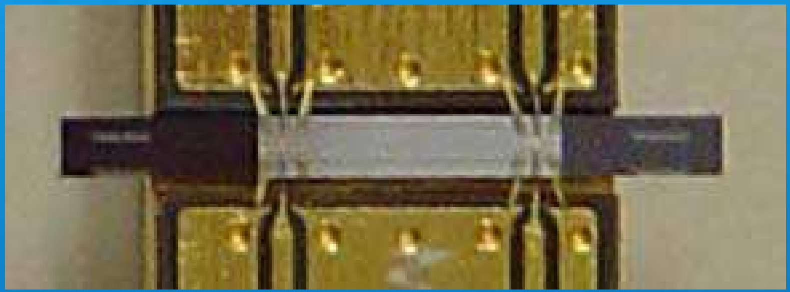
High Speed Silicon Modulator





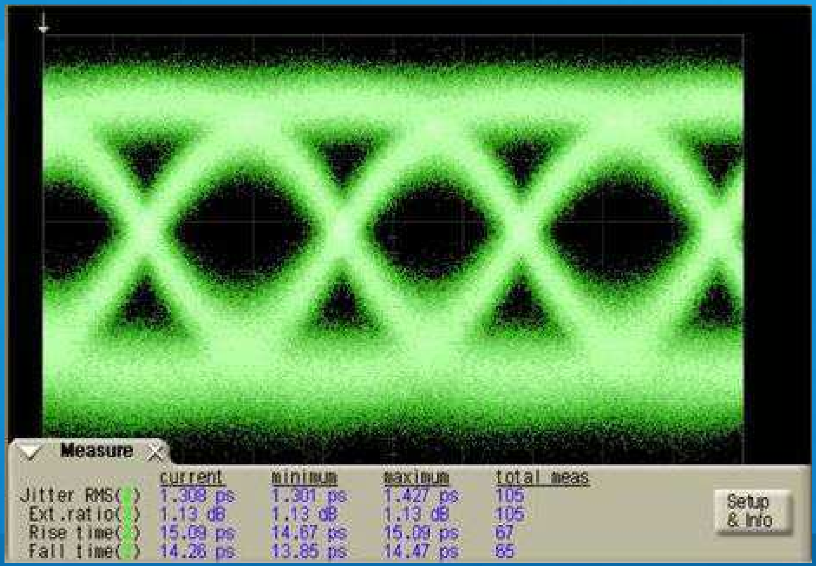
SEM picture of p-n phase shifter

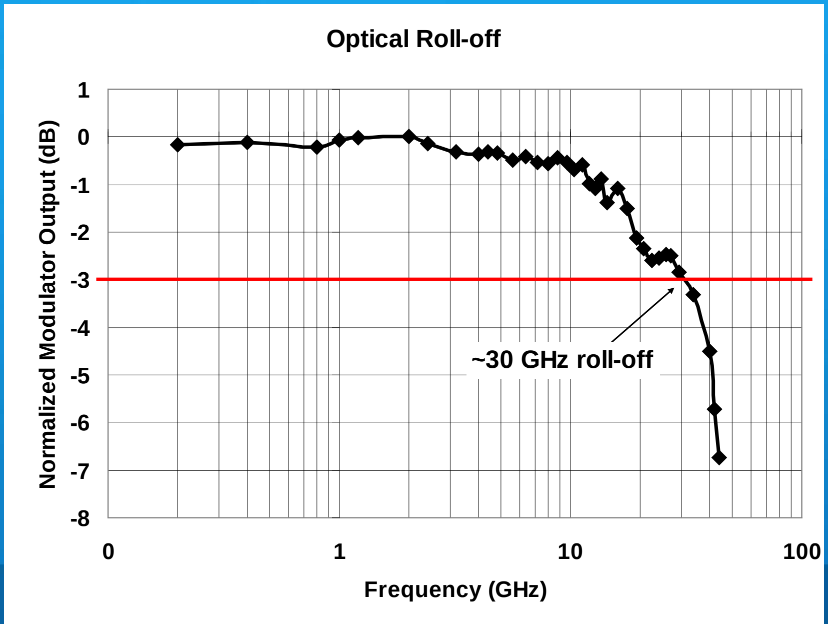


Si modulator on PCB

- Reversed biased pn diode based devices
- Travelling wave electrode designs
- Mach-Zhender configuration
- Stable over temperature and wavelength

40Gbps Data Transmission





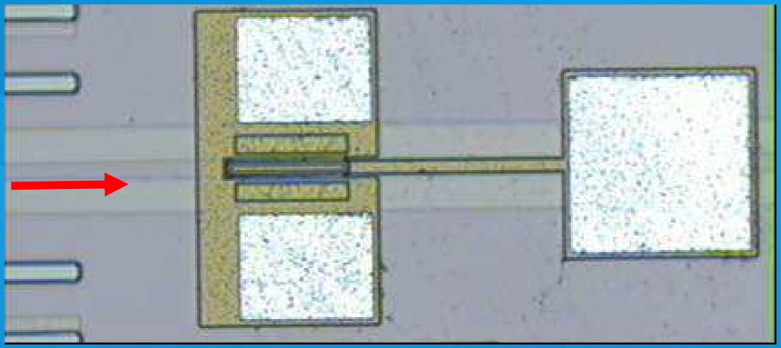
40Gbps Data Transmission

“Eye” diagram from large signal, psuedo-random bit sequence (prbs) testing

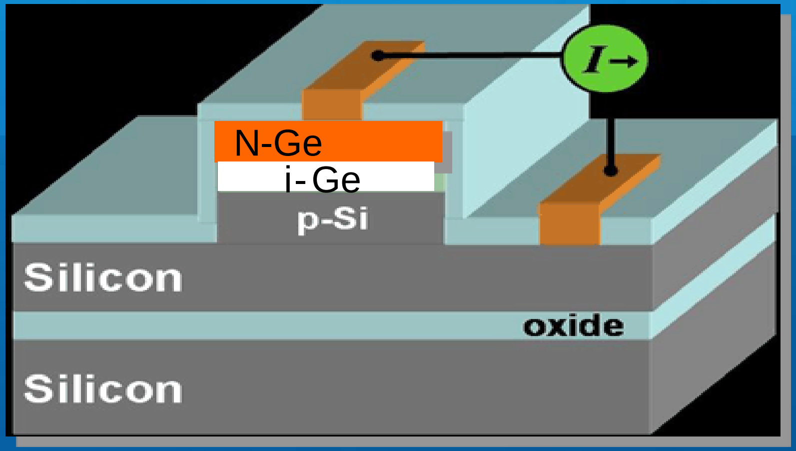
Small Signal Testing
Optical 3 dB roll off ~30 GHz

L. Liao, A. Liu, D. Rubin, J. Basak, Y. Chetrit, H. Nguyen, R. Cohen, N. Izhaky, and M. Paniccia, “40 Gbit/s silicon optical modulator for high-speed applications,” Electron. Lett. Vol. 43, No. 22, 25th October 2007.

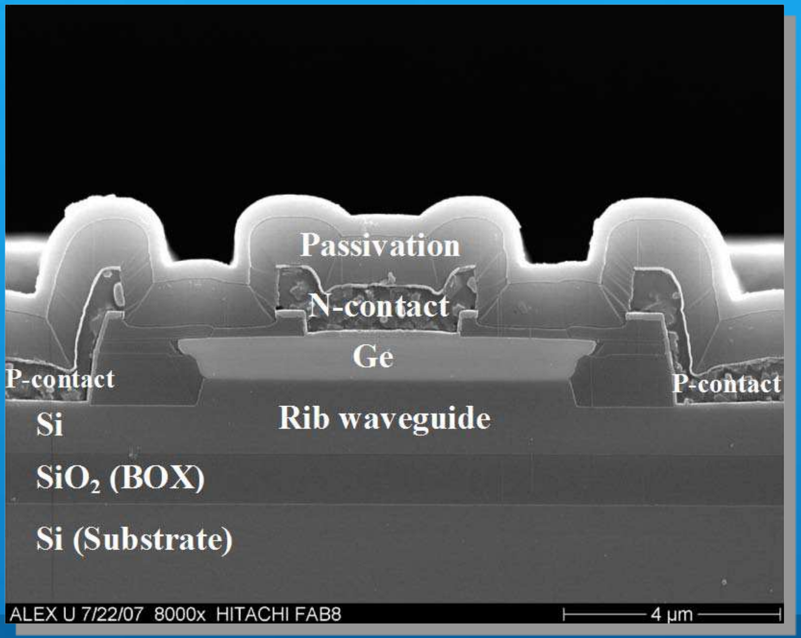
SiGe Waveguide Photodetector Design



Top View



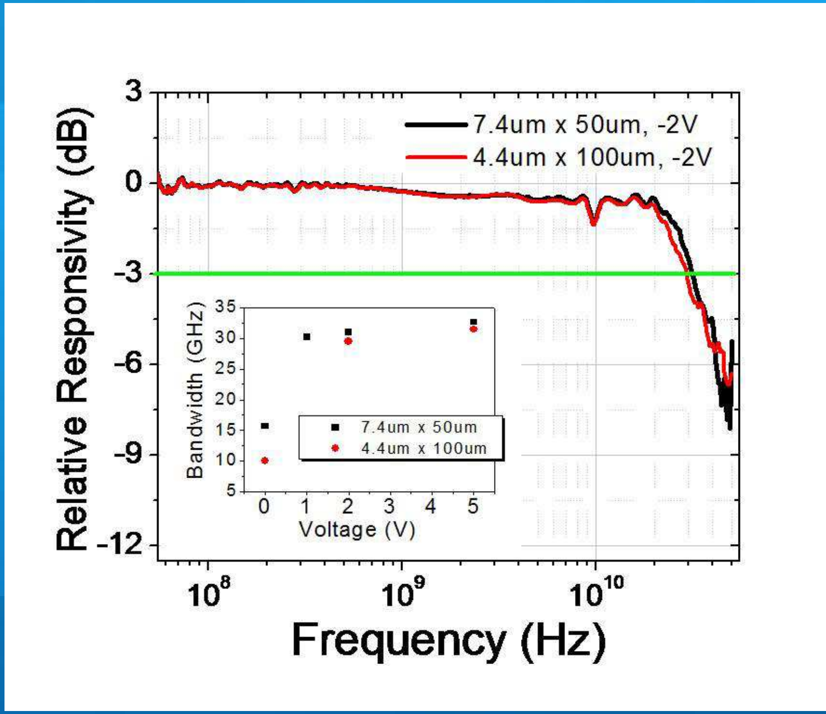
SEM Cross-Section



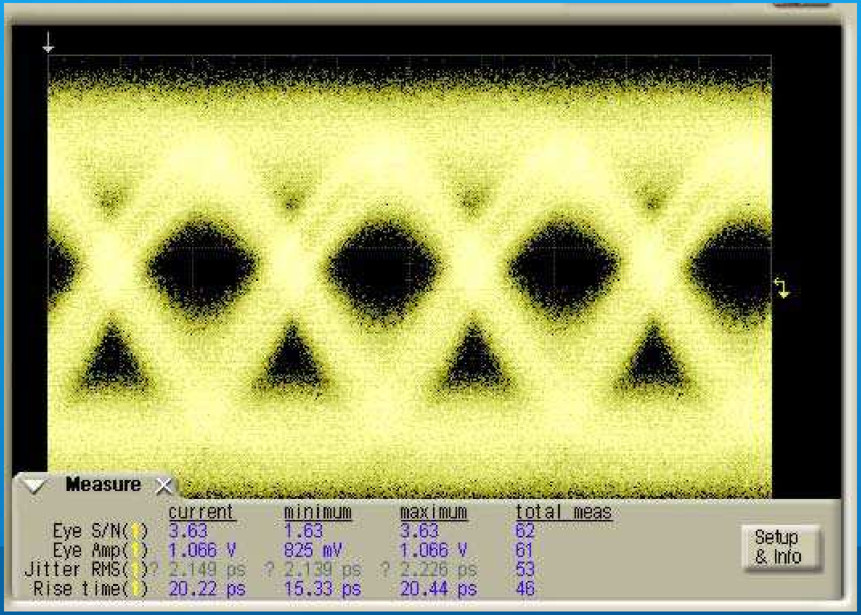
SEM Cross-Section

- Photodetector concepts rely upon the epitaxial growth of Ge on SOI substrate
- Ge absorption scales to ~1600nm

SiGe WG PIN - High Speed Performance



31 GHz Optical Bandwidth



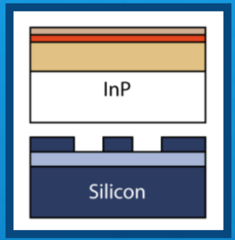
40 Gbps Eye Diagram

95% Quantum Efficiency
Operating at λ ~1.56um
< 200nA of dark current

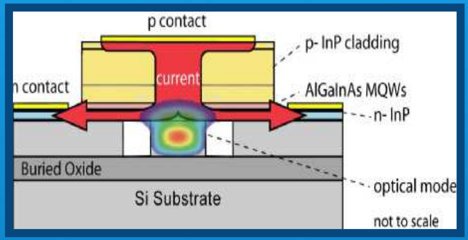
"31 GHz Ge n-i-p waveguide photodetectors on Silicon-on-Insulator substrate"; Tao Yin, Rami Cohen, Mike M. Morse, Gadi Sarid, Yoel Chetrit, Doron Rubin, and Mario J. Paniccia Optics Express, Vol. 15, Issue 21, pp. 13965-13971

Hybrid Silicon Laser
(Developed with UCSB)

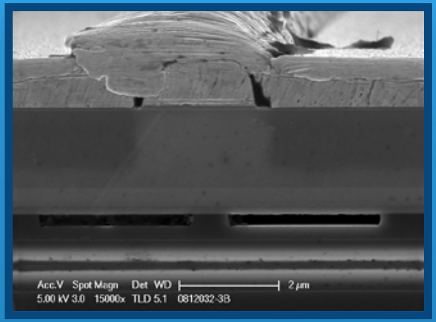
Creating a Silicon-based laser by bonding a III-V material (Indium Phosphide) onto Silicon



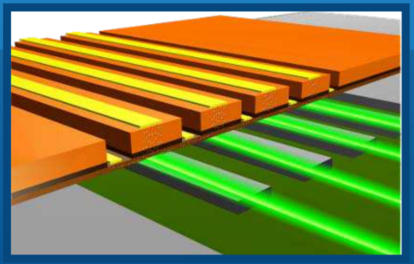
InP bonded to Si



Cross Section of Hybrid Laser



SEM of Cross Section

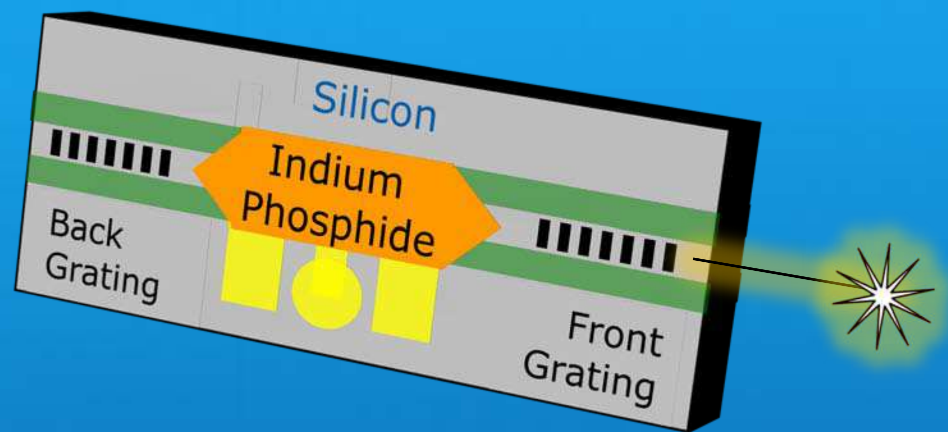


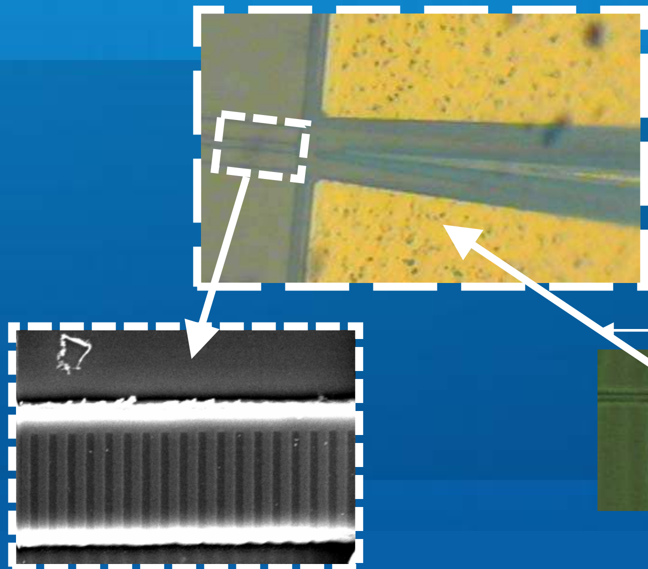
One bond, no alignment needed

- InP emits light when electrically stimulated
- Light bounces back and forth in silicon, and is amplified by the InP based material
- Mirrors are gratings etched into the silicon
  - Grating pitch defines the laser wavelength

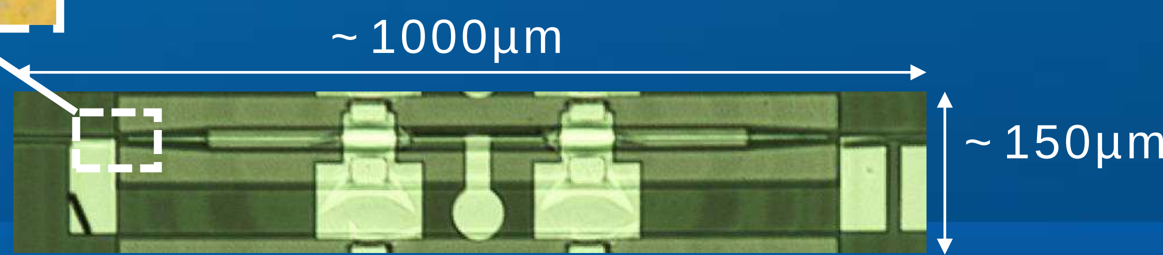
Single Wavelength Hybrid Laser

- Photolithographically defined grating mirrors fabricated in silicon.
- Creating low cost, HVM compatible wavelength-specific laser channels





Typical Device



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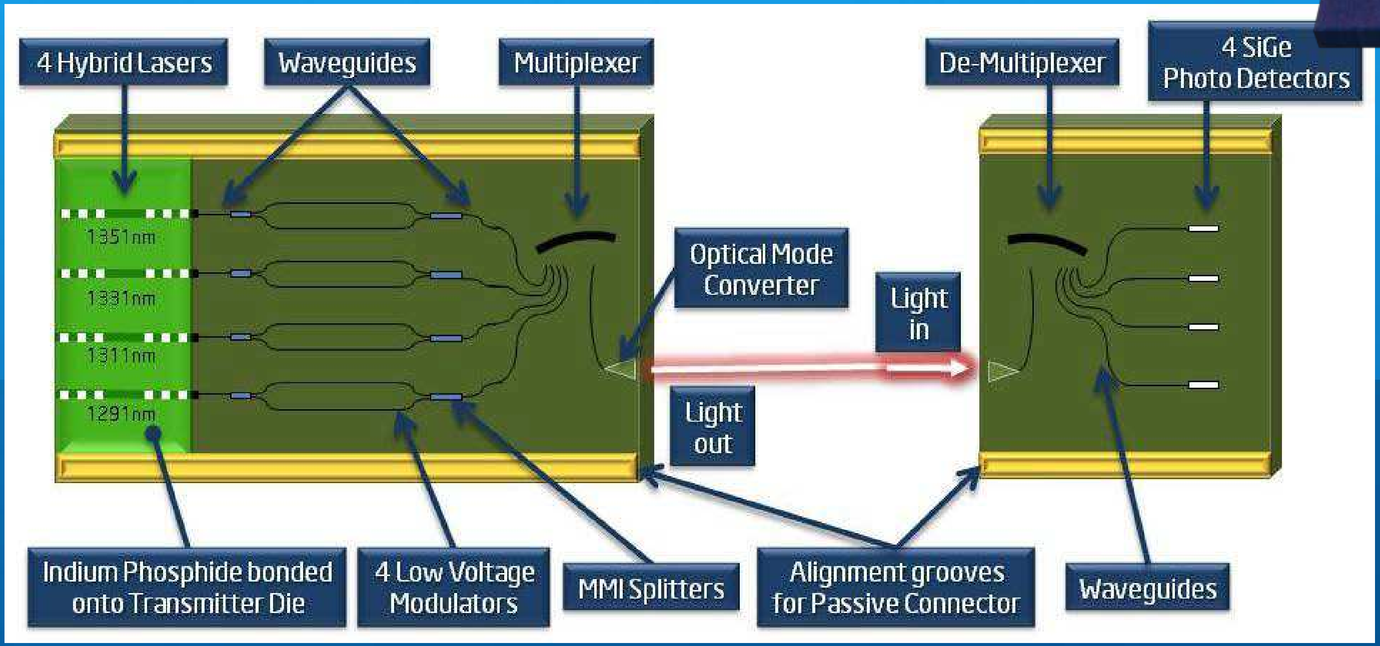
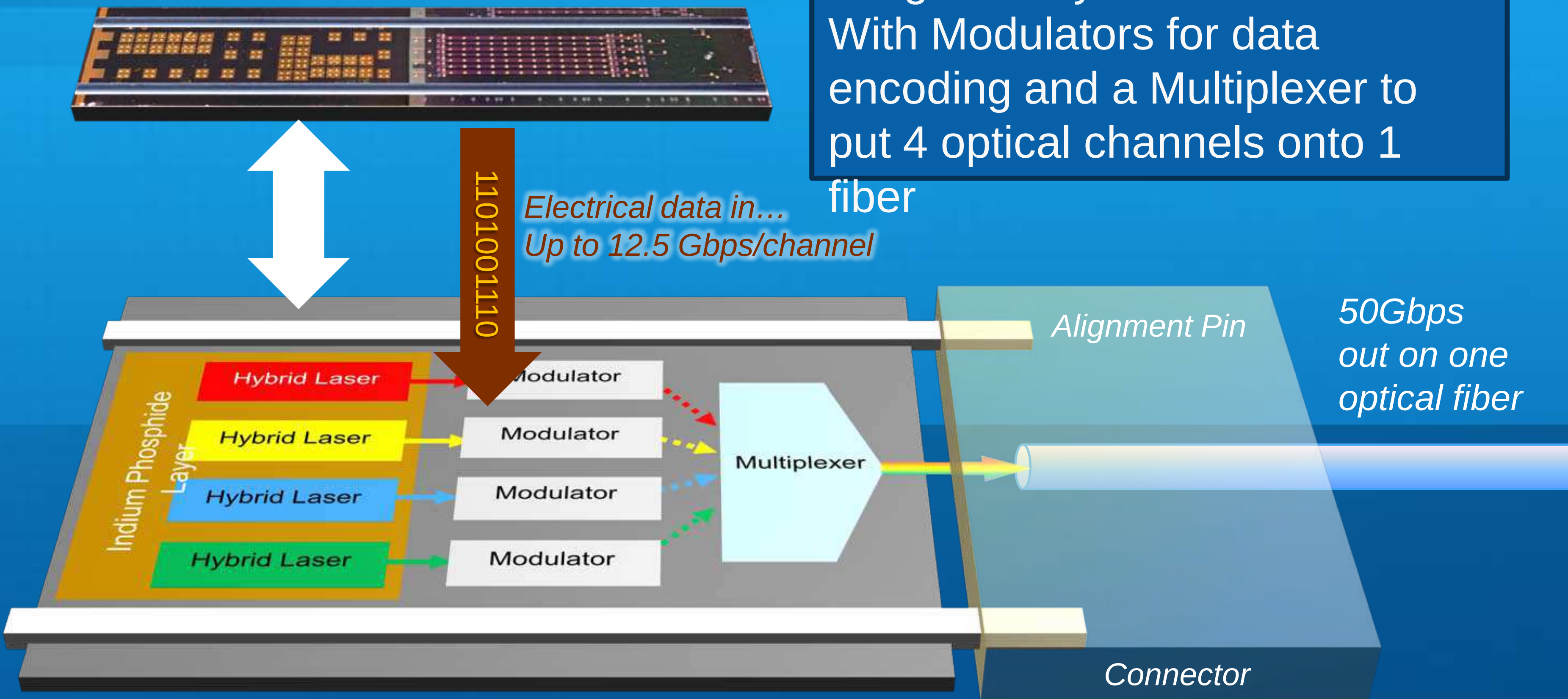
Integrated 4 Channel CWDM Silicon Photonics Architecture



- Silicon Hybrid Laser and Transmitter components integrated on one silicon die
- Receiver components integrated onto a separate silicon die

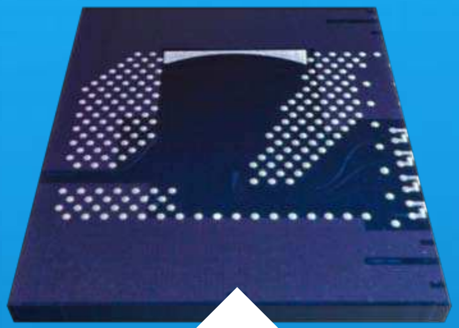
Integrated Transmitter Chip

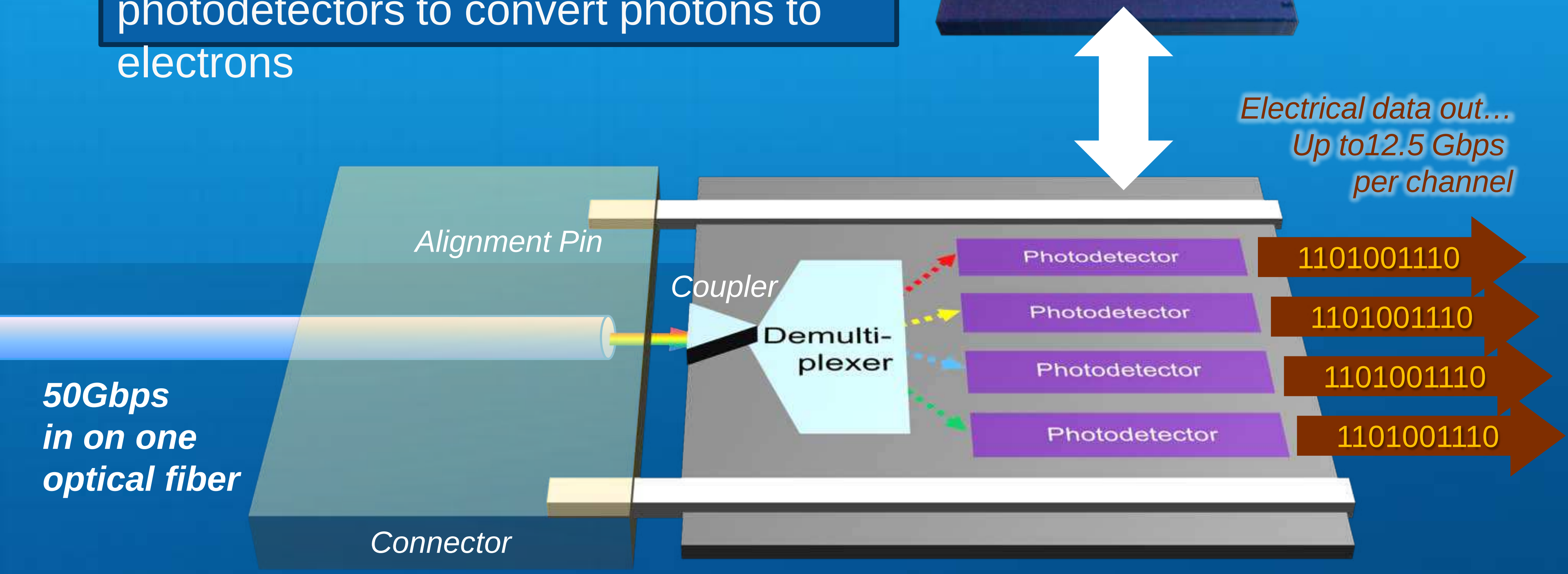
Integrates Hybrid Silicon Lasers With Modulators for data encoding and a Multiplexer to put 4 optical channels onto 1 fiber



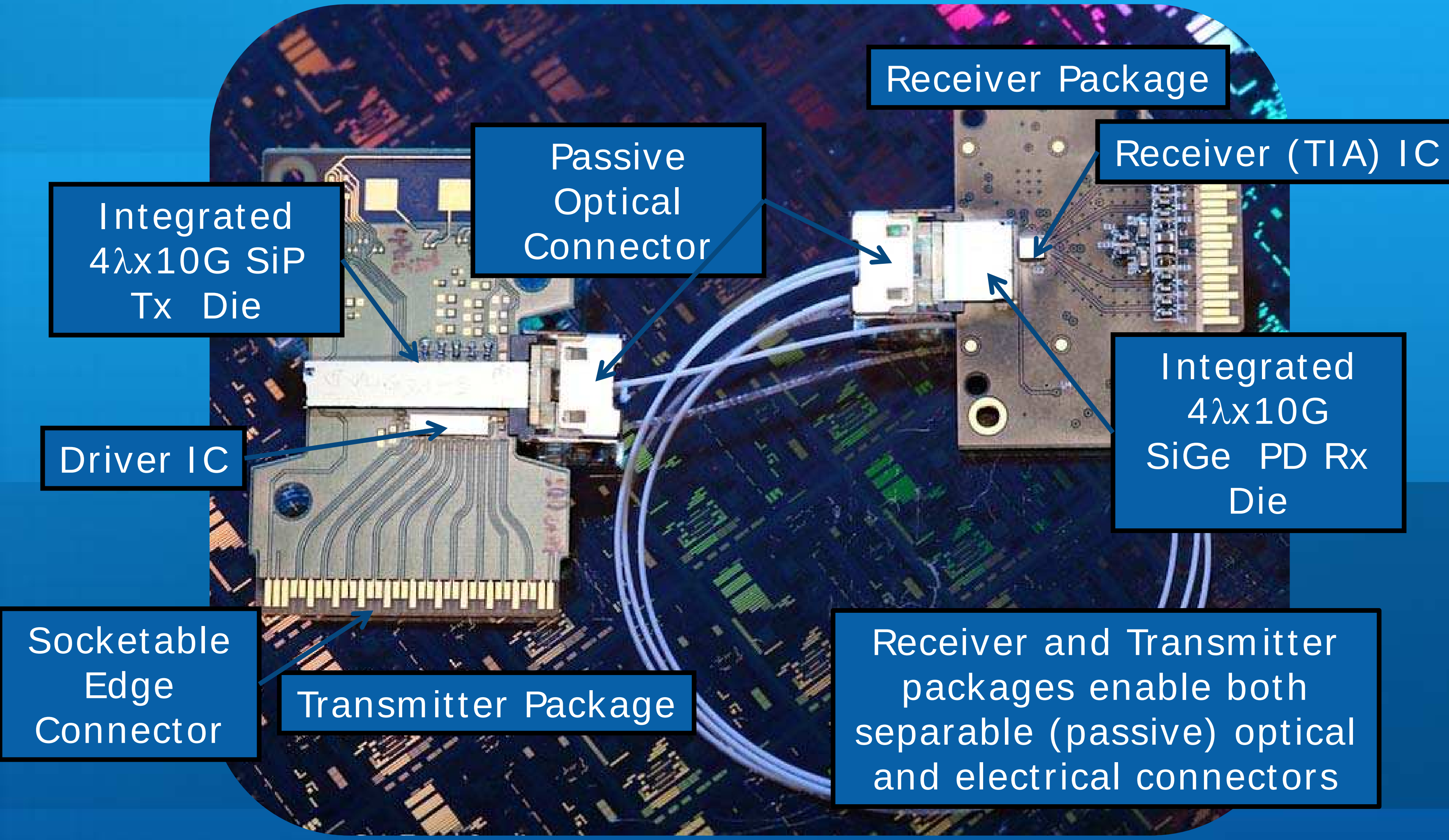
Integrated Receiver Chip

Integrates a coupler to receive incoming light with a demultiplexer to split optical signals and Ge-on-Si photodetectors to convert photons to electrons

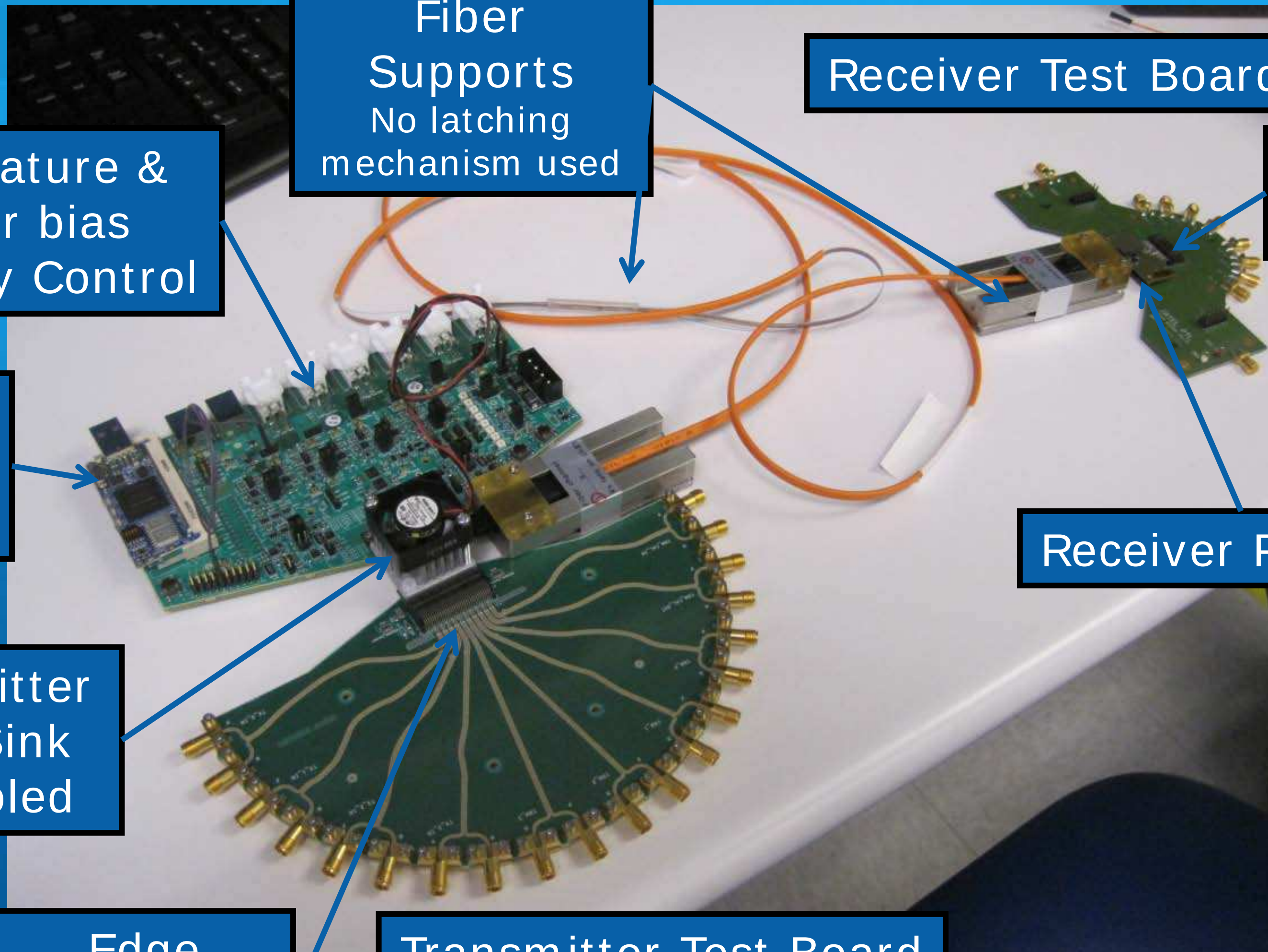




4λx10Gbps SiP Tx & Rx Packages



End to End System Test Setup



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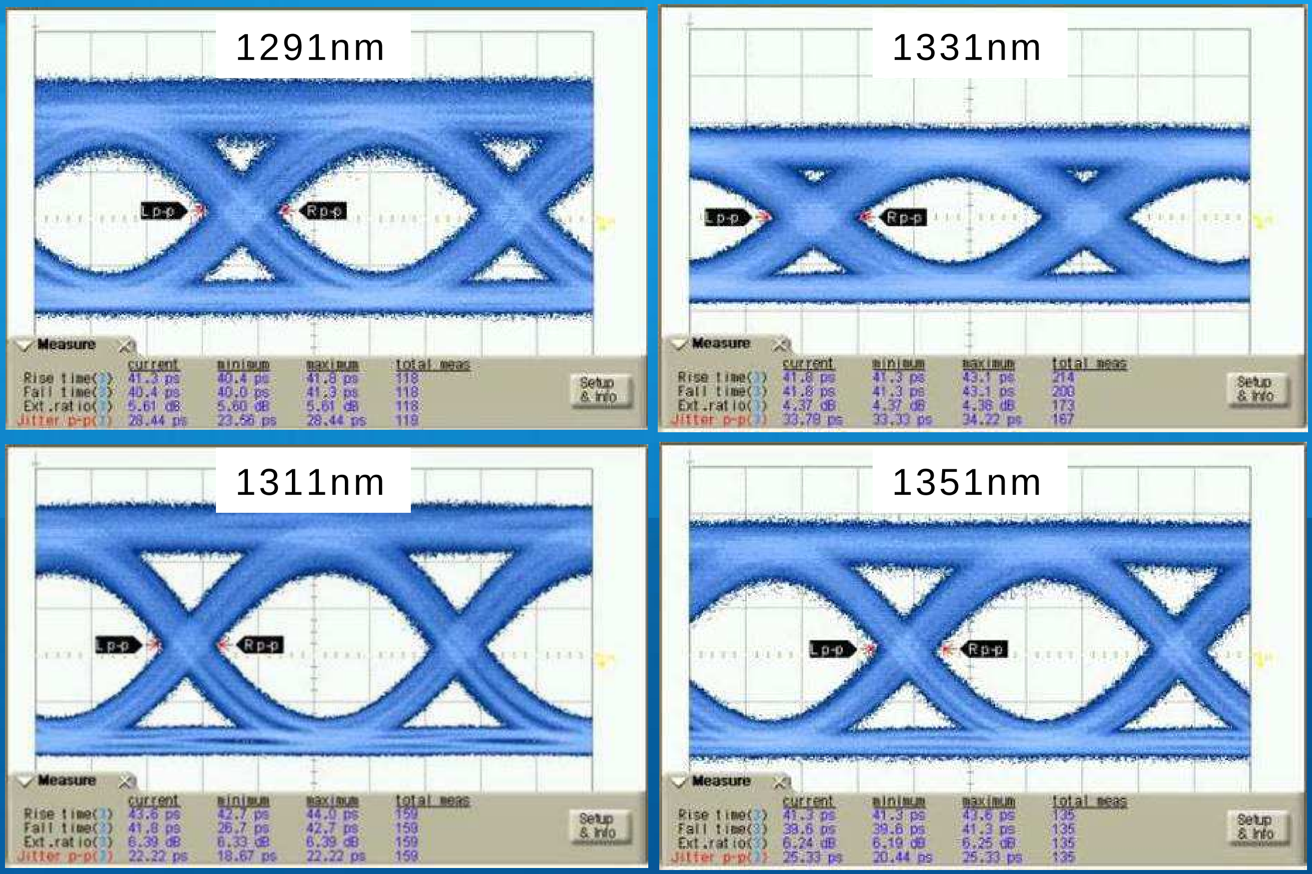
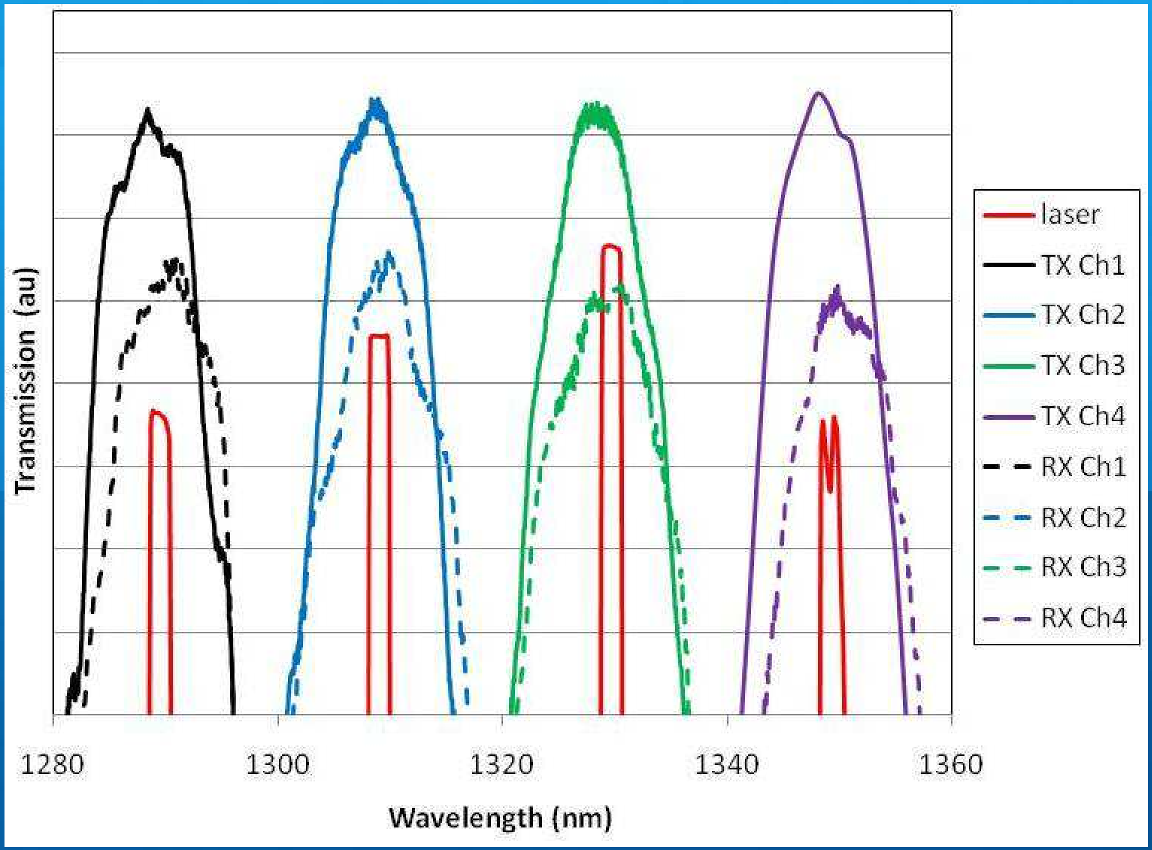
Integrated Transmitter Optical Eye Diagrams



Performance parameters

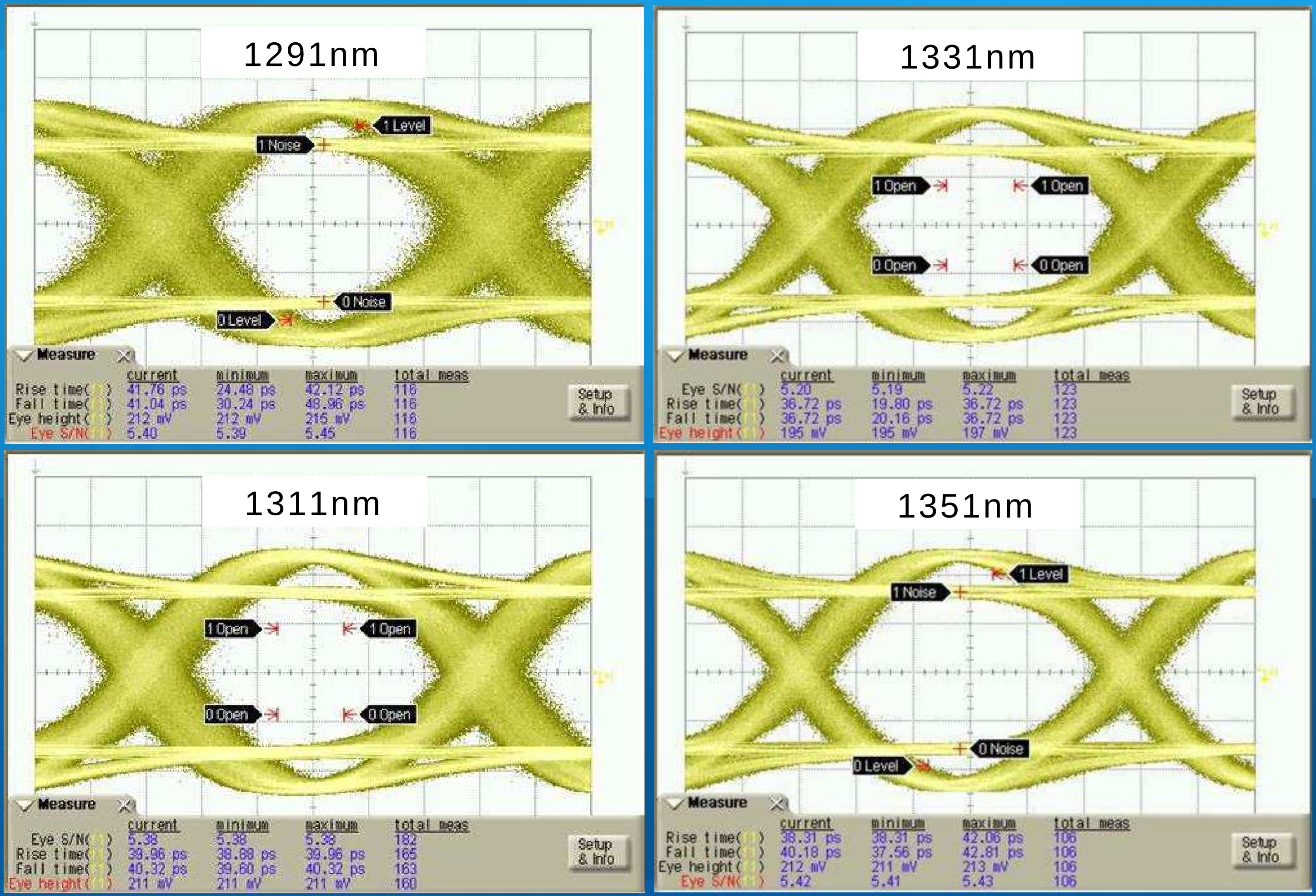
- Extinction Ratio = 4.4-6.3dB
- Rise/Fall Time = 41-44ps
- Total Jitter = 23-34ps
- CW Silicon Hybrid Laser die output power from 2mW to 9mW

Wavelength Channel Alignment



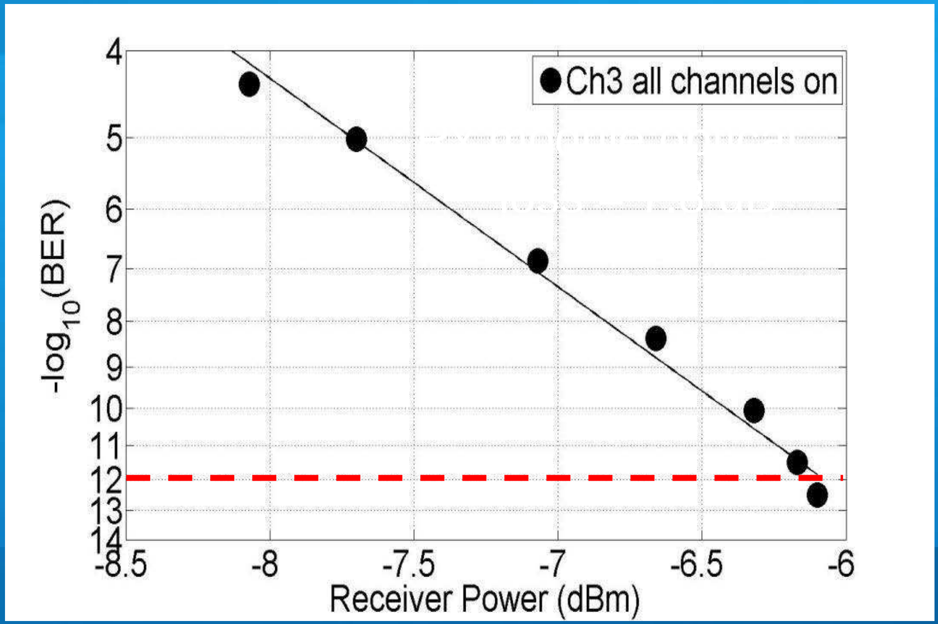
- CWDM Channels were chosen – 20nm spacing (1291nm, 1311nm, 1331nm & 1351nm
- No temperature tuning or stabilization was used
- Alignment of laser, multiplexer and demultiplexer channels are ~1nm
- Estimated λ mismatch loss <0.3dB

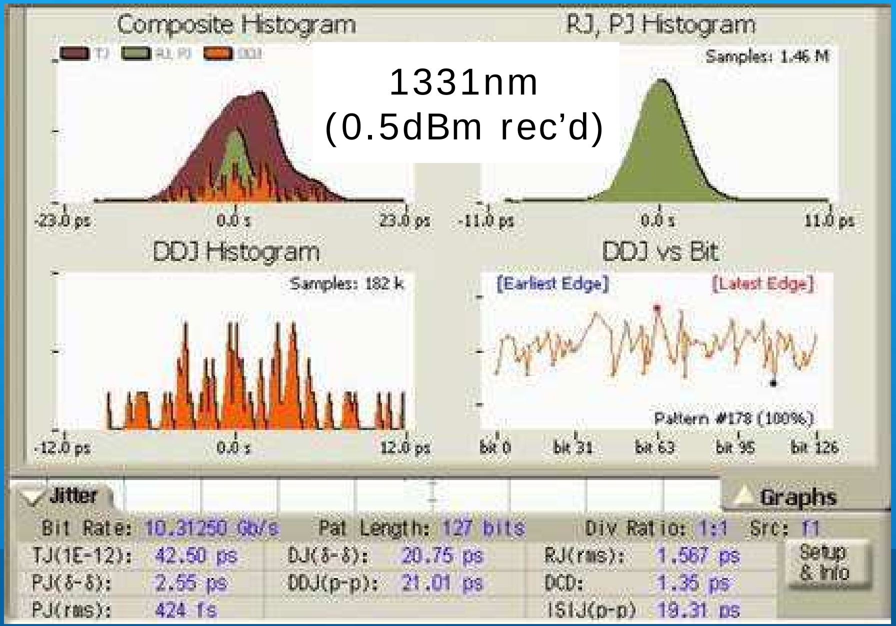
40Gbps (4λx10Gbps) Link Performance



- Output electrical eye diagrams
- Travelling wave silicon MZ modulator
- Intel designed driver IC, with 1.35V across modulator
- ER from 4.4dB to 6.3dB
- Rise/Fall Time = 41-44ps

10Gbps Link Margin



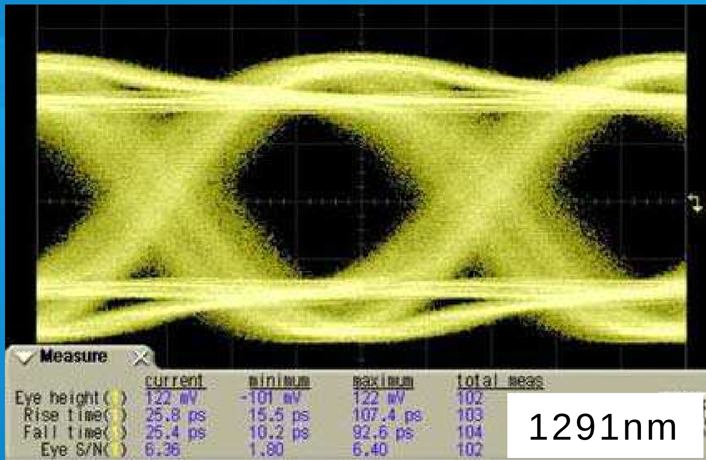


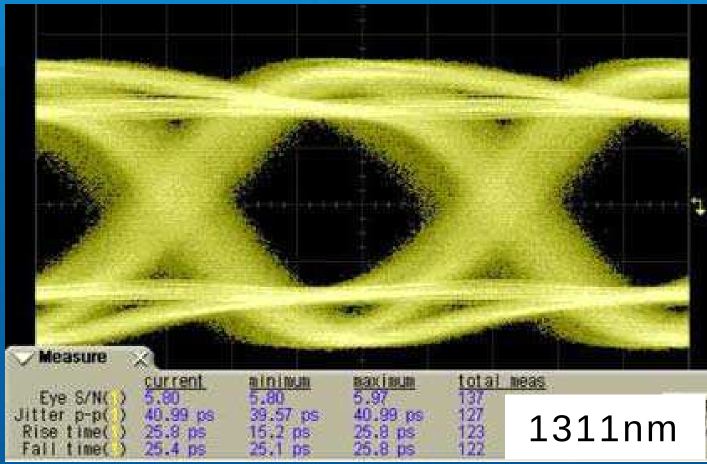
Link Margin = 6.7dB for BER of 10^{-12}

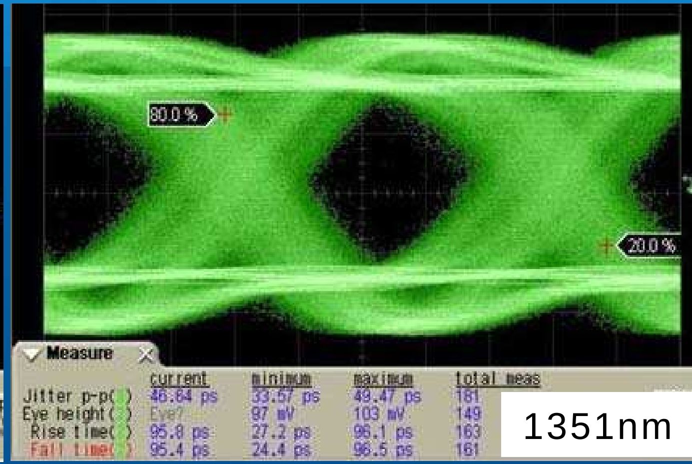
Jitter Measurements

- Link Total Jitter ~43ps
- Random Jitter ~1.6ps
- Deterministic Jitter ~21ps

50Gbps (4λx12.5Gbps) Link Performance







- Devices were "overclocked" to 12.5Gbps
- Eyes remained open, link remained stable
- Ch1-3 BER $< 10^{-12}$, Ch4 $\sim 3x10^{-10}$
- ER from 3.4dB to 5.6dB
- Rise/Fall Time = 38-42ps

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The Path to Tera-scale Data Rates

Today: 12.5 Gbps x 4λ = 50Gbps

Scale UP

25 Gbps x 4λ = 100Gbps

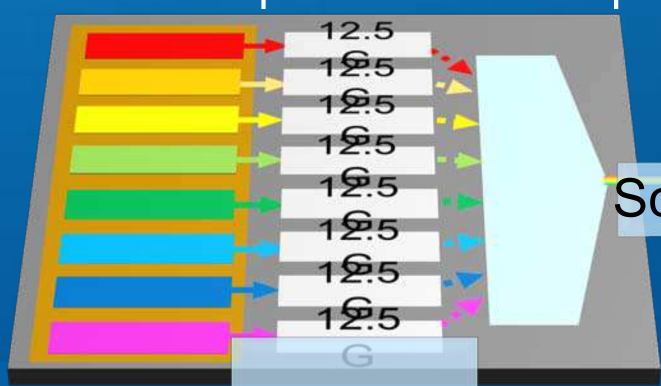
40G, 100G…

Scale OUT

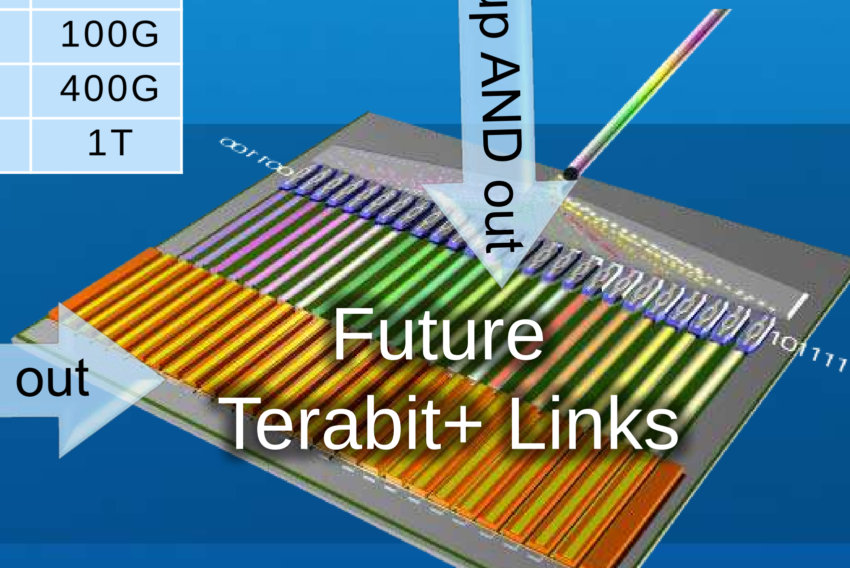
Speed	Width	Rate
12.5	x4	50G
12.5	x8	100G
25	x16	400G
40	x25	1T

Scale up AND out

12.5 Gbps x 8λ = 100Gbps



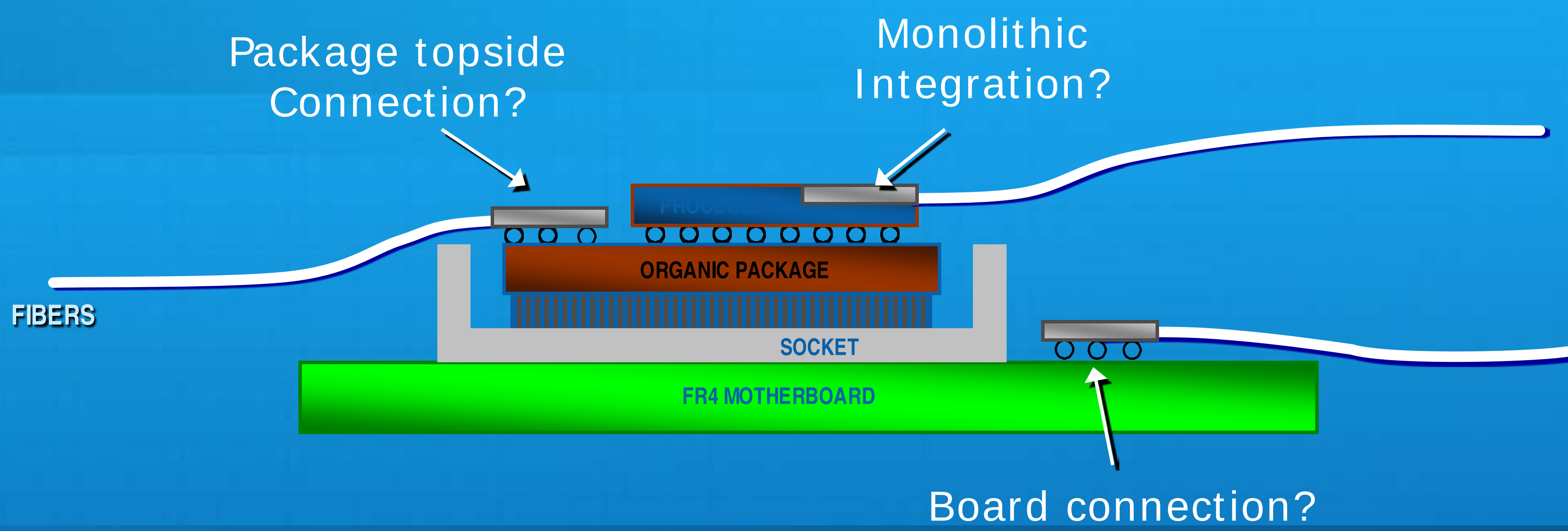
Scale up AND out



x16, x32…

Could enable cost-effective high speed I/O for data-intensive applications

Challenges: Optical Integration with CPU



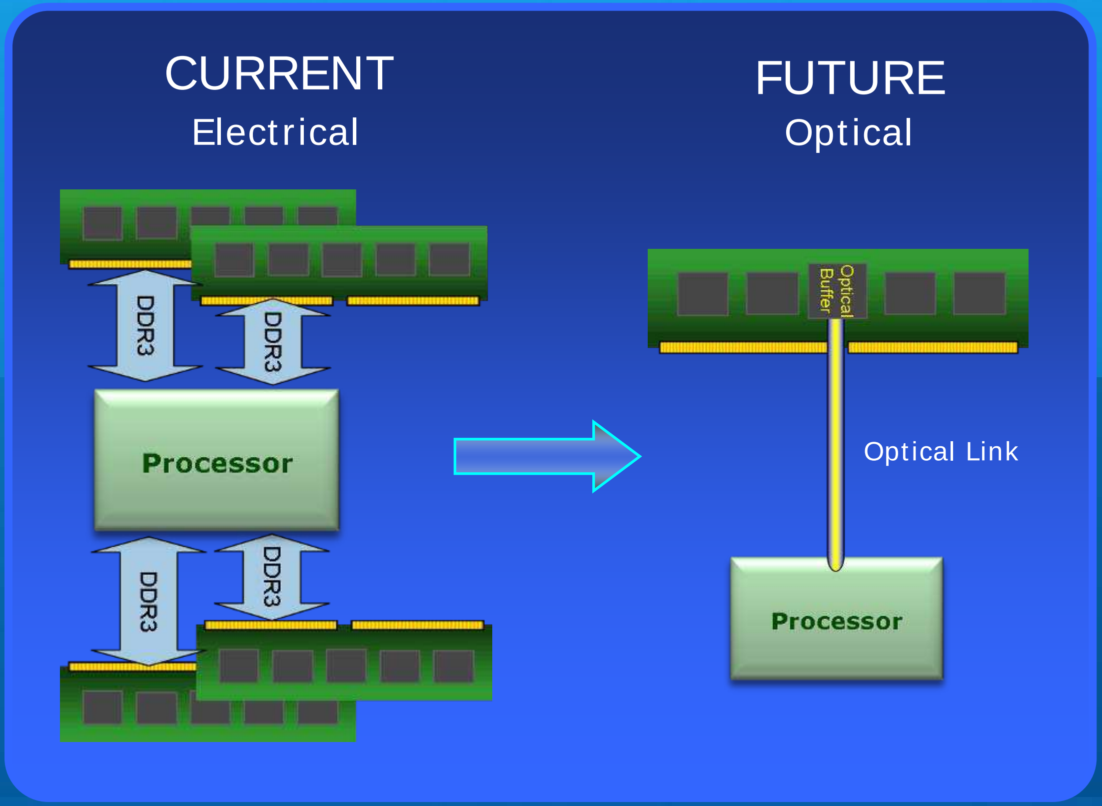
Challenges:

- Power: CPU's operate with Temperatures near ~85°C
- Packaging: Compatibility with existing HVM packages
- Testing: Testing co-packaged optical /electrical CPU modules

Multiple approaches. Must balance performance, flexibility and cost

Data Center: Remote Optical Memory

Can increase design flexibility and drive down cost by extending CPU-memory distance



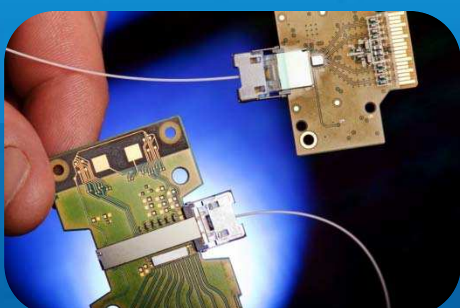
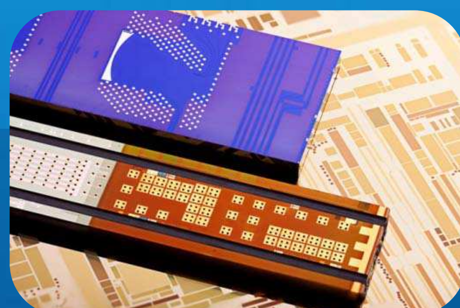
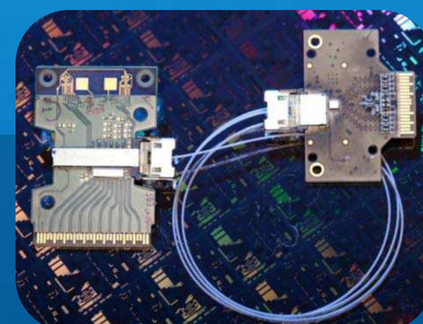
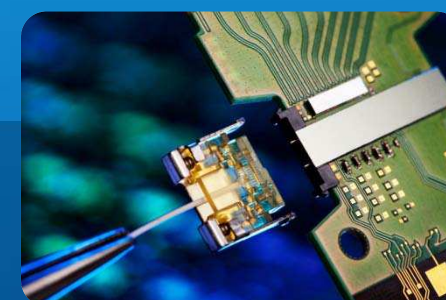
Potential Advantages

- Higher capacity and higher B/W at reduced system cost
- Distance flexibility as memory can be further from processor
- Board cost reduction due to less complex routing
- Potentially overall power reduction at system level

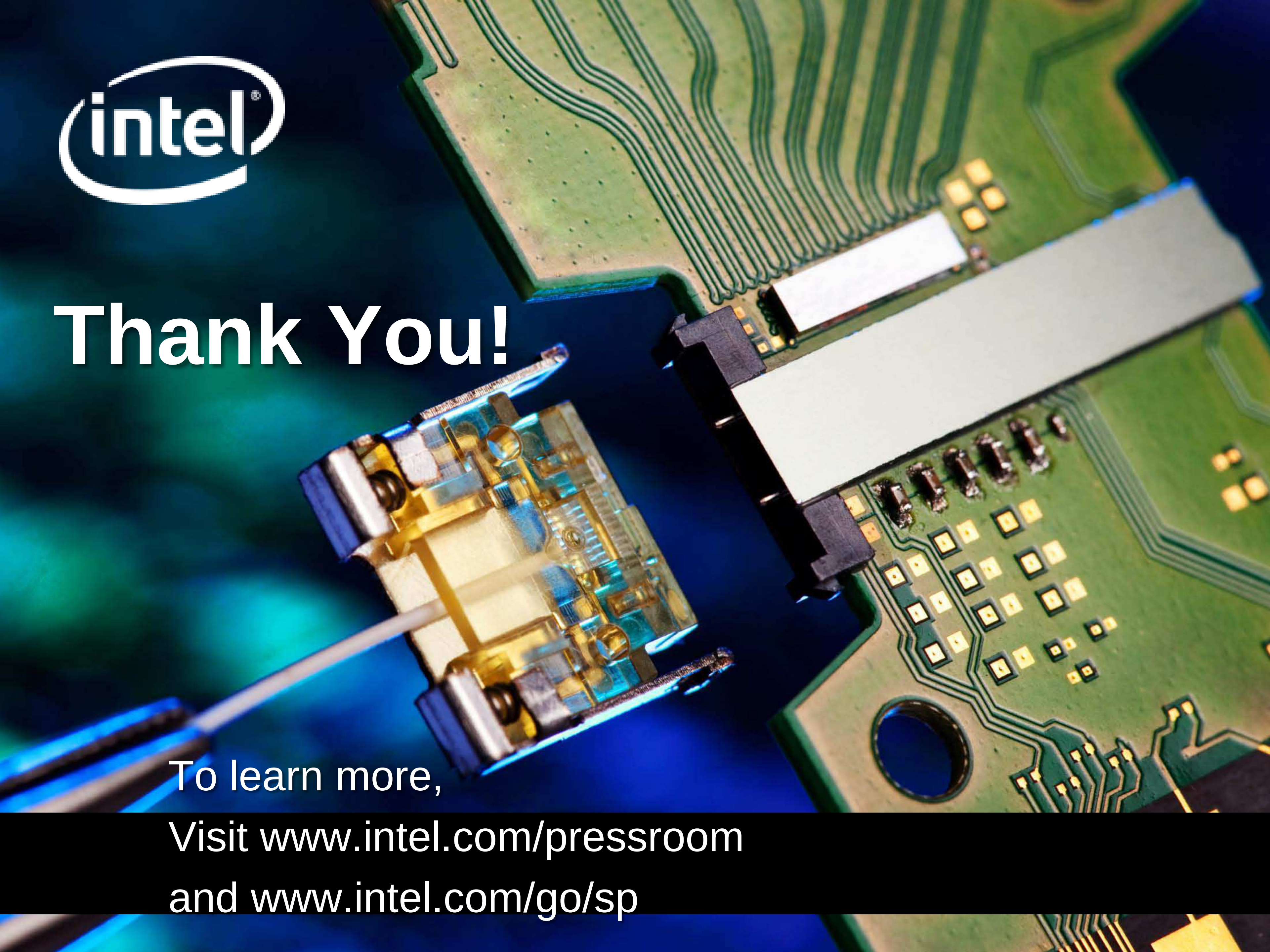
- Thermal & mechanical challenges to co-package with/next to CPU

WDM Silicon Photonics Link Summary

- Demonstrated the first silicon hybrid laser and modulator WDM link with all technologies required for system integration
- Demonstrated a 4 channel WDM system at 10Gbps – aggregate bandwidth of 40Gbps
- Further demonstrated the link at 50Gbps with channels operating at 12.5Gbps

- **<u>Acknowledgements</u>**
- Aurrion Ltd – For InP processing and hybrid laser developments
- Micron (Numonyx) – For Silicon Photonics processing



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