HOT CHIPS

Transcede™

Solving 4G Challenges for Pico, Micro and Macrocell Platforms

Jim Johnston
CTO

Communications Convergence Processing
Mindspeed Technologies, Inc.

MINDSPEED
BUILD IT FIRST®

August 24, 2010

The Next Internet Wave – Mobility and Content

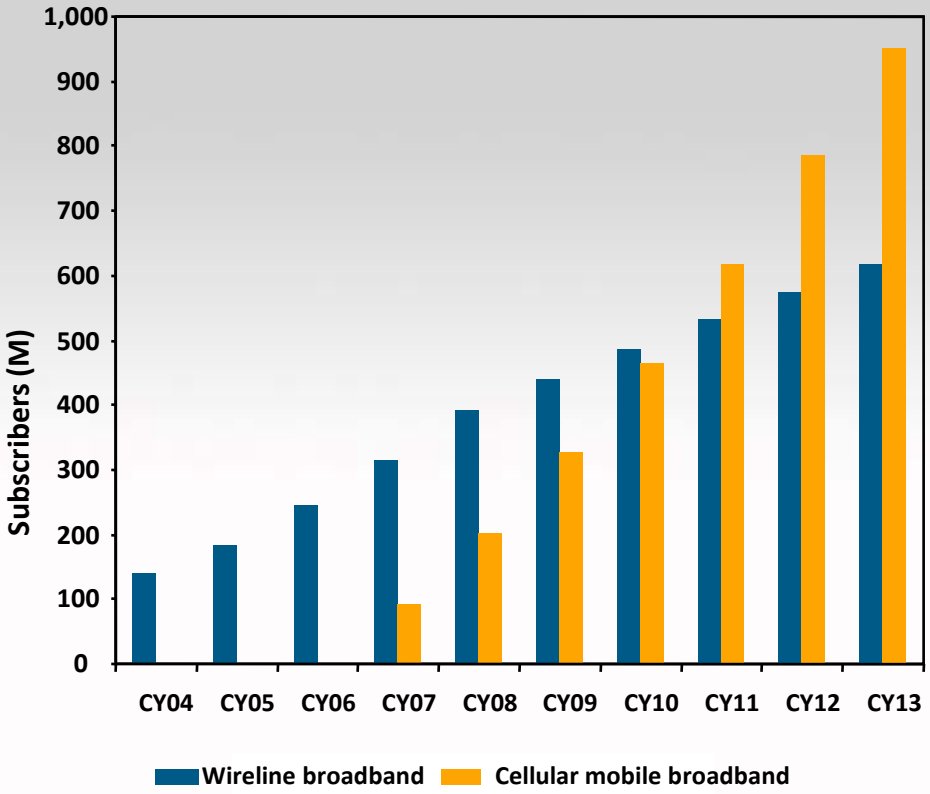
Innovative New Platforms

+

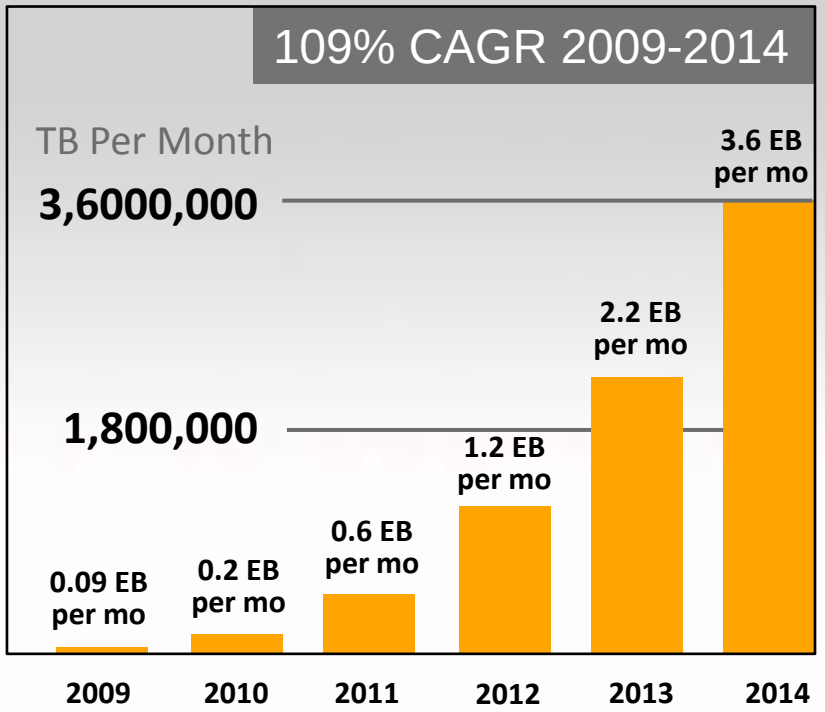
New Networked Applications

= **Explosive demand for Mobile Broadband**

Impact on Service Providers



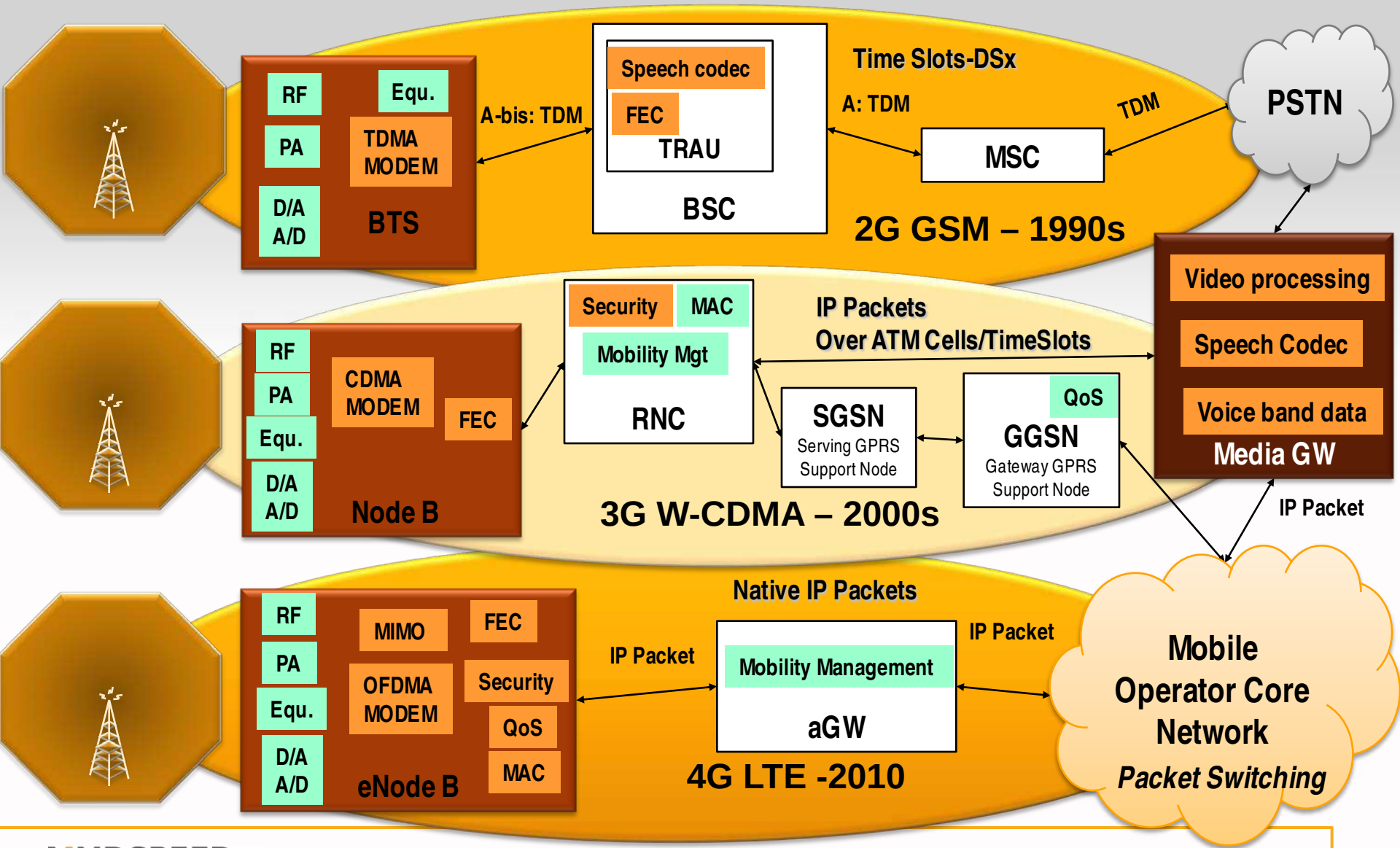
Source: Infonetics Q4'2009



Source: 2010 Cisco VNI Mobile

… Overloaded Networks

2G to 4G - System Architecture Evolution - to the Evolved Packet Core



Mobile Broadband Architecture – Going Distributed

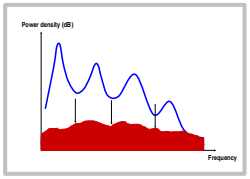
Macro	Micro	Pico	Enterprise Femto	Femto
Metro	Urban	High-Density Subs	Business	Residential
1200	400	200	50	10

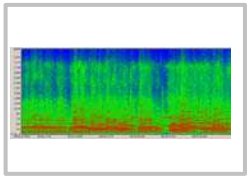
Supported Subscribers

Serving a broad range of basestations - from Macro to Femto

Mindspeed SoC Competencies

Multi-Processor Communications Technologies





Algorithms

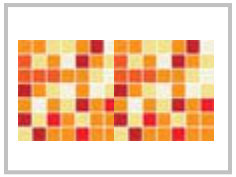
Standards Certification

Multi-Core Software

Software Verification

Software Architecture

Convergence Applications



Packet Processing

Voice, Video, and Modems

Silicon Architecture Evolution

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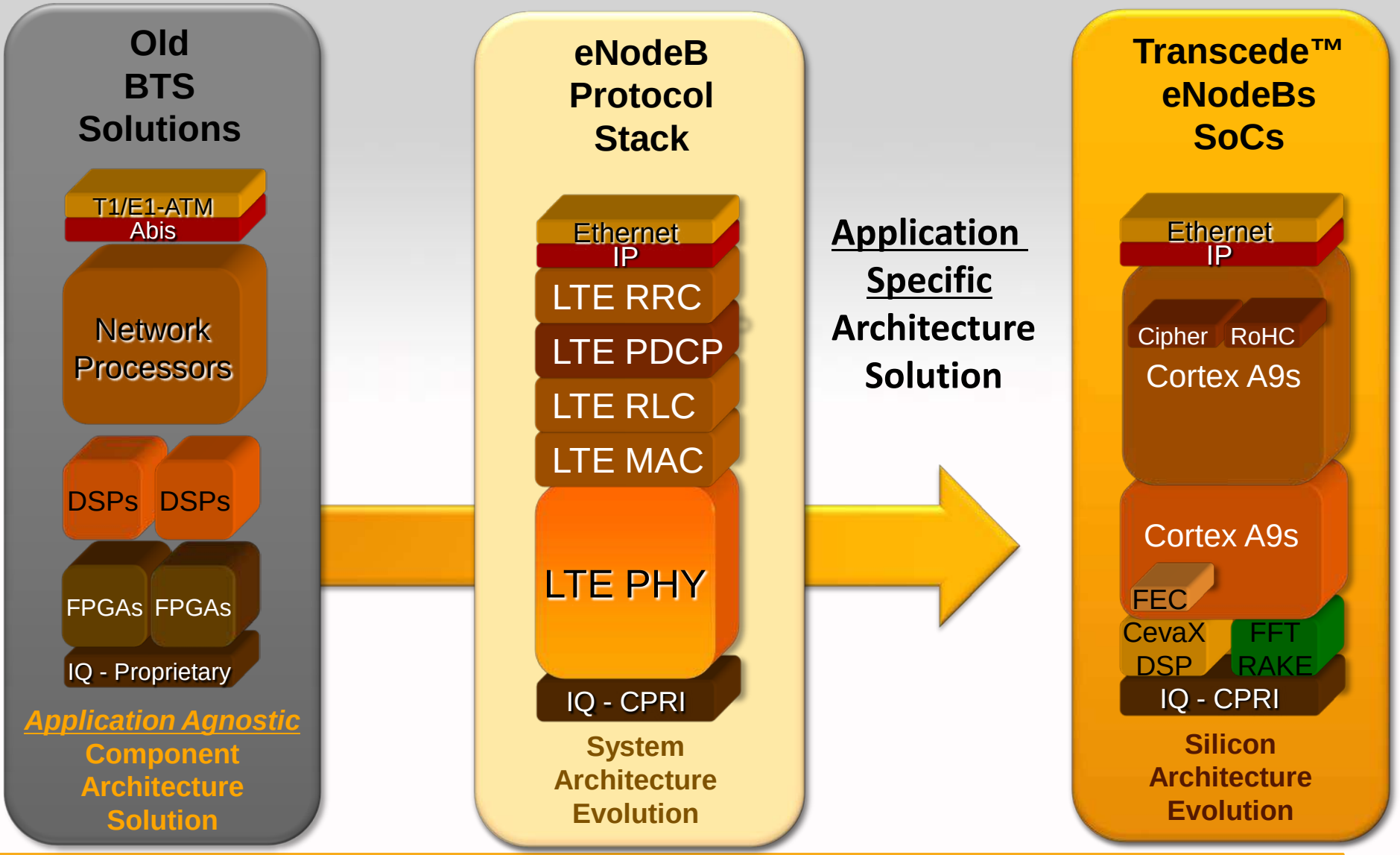
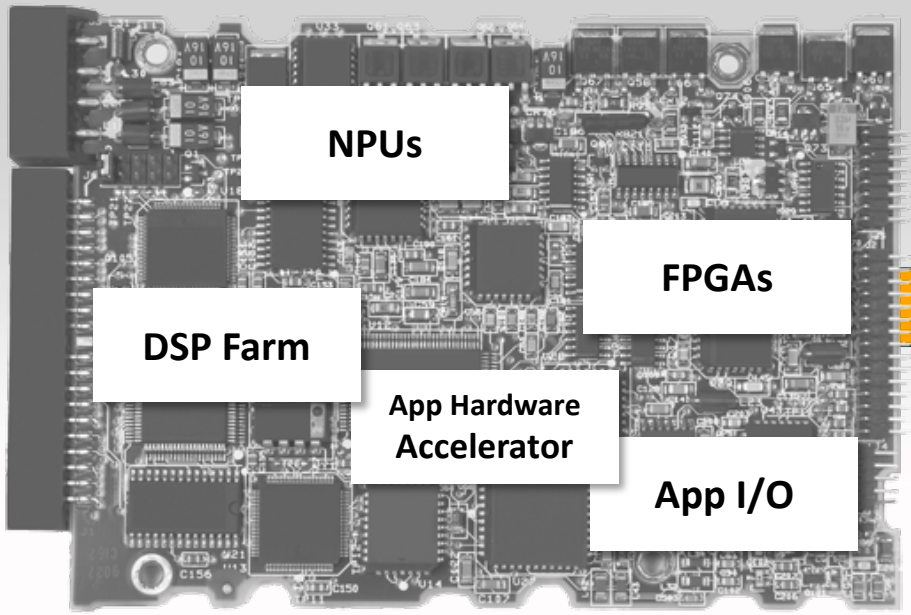
Silicon & System Architecture Innovation



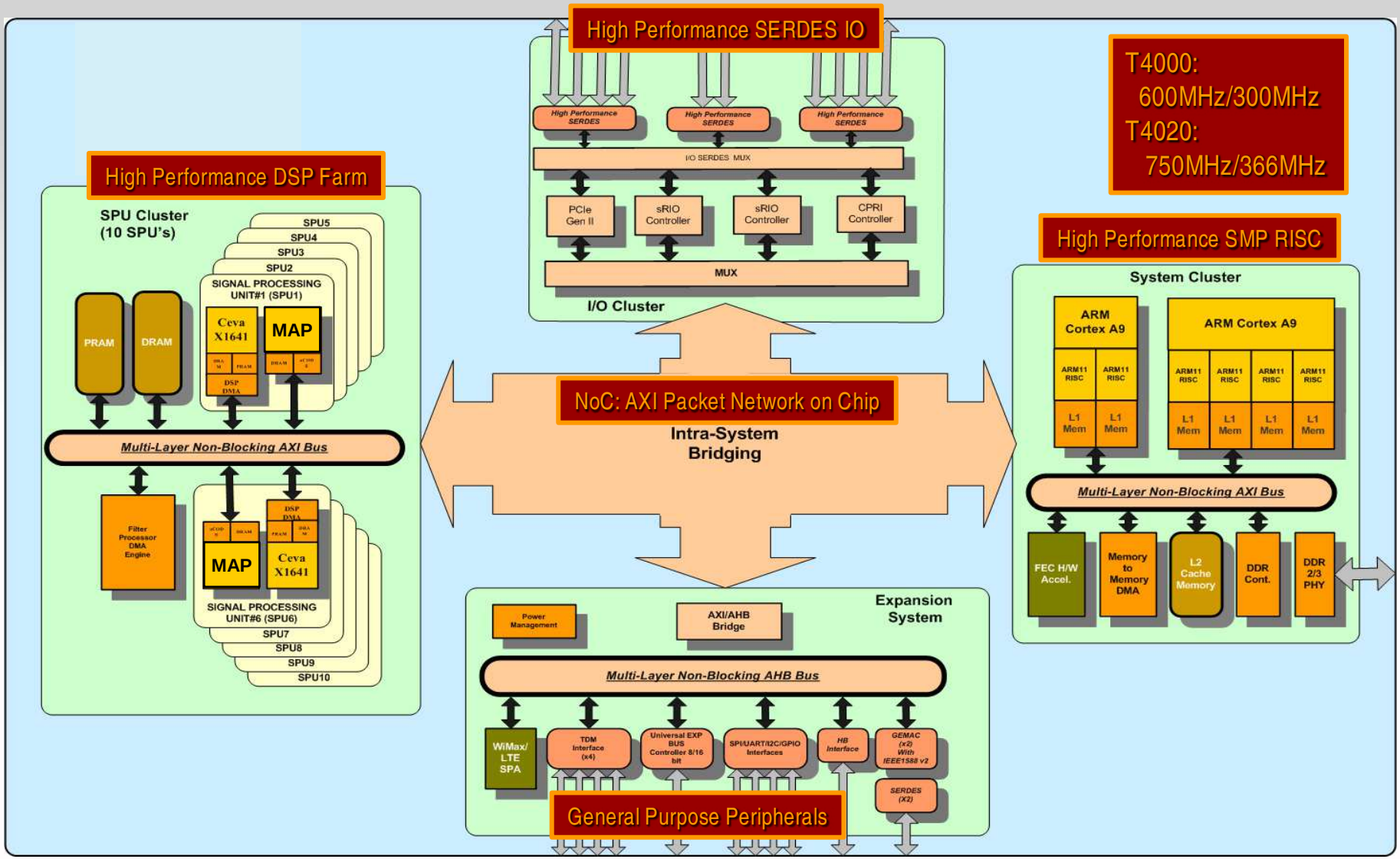
Transcede™ Dramatically Reduces System BOM



> $3000 **< $300**

… while significantly accelerating Time-to-Market

eNB Transcede™ - Multi-Core SoC



Processors: Instruction and Data Level Parallelism

High Efficiency Instruction Level Parallelism

- **600MHz to 750MHz Operation**
- **4 A9 Multi-Processing Cores**
  - SMP & AMP support
  - Parallel Cores with HW Snoop Logic
  - 32bit Instructions
  - Load/Store Register File
  - 13 stage Pipeline
- **Small L1 Memories**
  - 32kB Program Cache
  - 32kB Data Cache
- **Large L2 Memories**
  - **512kB Unified Cache**
- **Embedded Trace Module**
  - Complex Instruction Diagnostics
- **Dual Data/Program DMA/Cache**
- **Extensive Tool Chain**
  - C-Compliers/Debugger/etc.

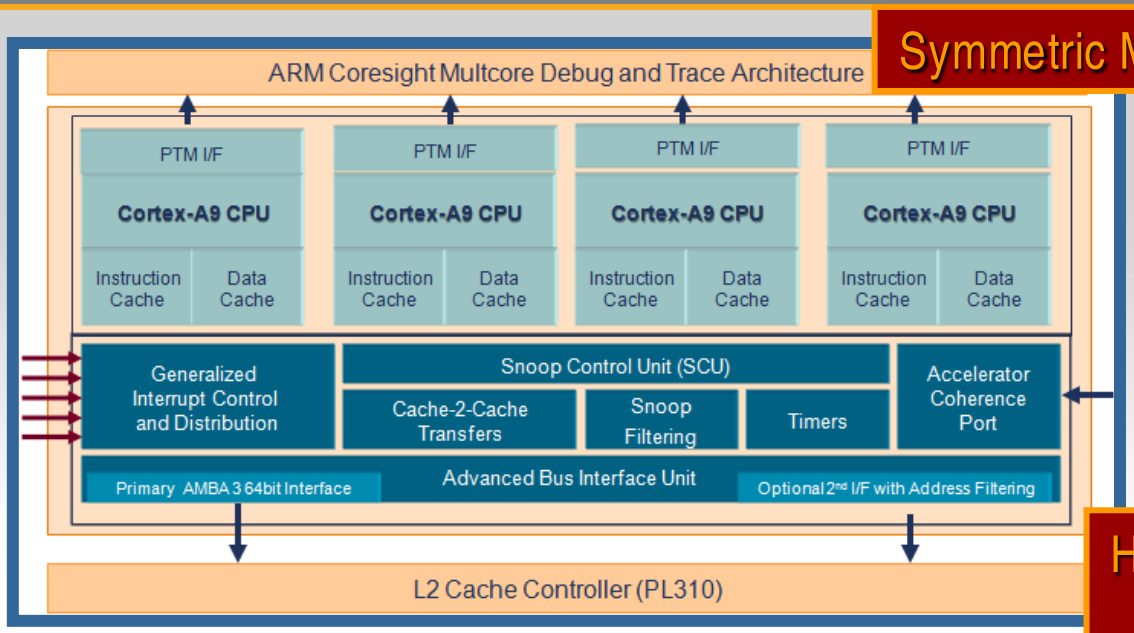
High Efficiency Instruction & Data Level Parallelism

- **600MHz to 750MHz Operation**
- **256bit-8 Way VLIW DSP**
  - 8-32bit Parallel Instructions
    - Most common size
    - 16-16bit Parallel Instruction
  - 9 stage Pipeline
- **128bit 4/8 MAC SIMD**
  - 4- 16bit x 16bit MACs
  - 8- 8bit x 8bit MACs
- **Large L1 Memories**
  - 96kB Program RAM
    - Direct Mapped Cache Option
  - 128kB Data RAM
  - Banked Simultaneous Access
- **On-chip Emulation Module**
  - Complex Breakpoints/Trace/etc.
- **Dual Data/Program DMA/Cache**
- **Extensive Tool Chain**
  - C-Compliers/Debugger/etc.

High Efficiency Data Level Parallelism

- **600MHz to 750MHz Operation**
- **160bit-VLIW DSP**
  - Fine Grain VLIW
- **160bit SIMD**
  - 24bit x 16bit MACs
- **Built in FFT Radix Support**
- **Large L1 Memories**
  - 10kB Program RAM
  - 80kB Data RAM
  - Banked Simultaneous Access
- **External Sequencer Control**
- **High Performance DMA**
- **Side-band Multi-Core Sequencing Control Channel**
  - **Processor to Processor Pipelined Data Flow**

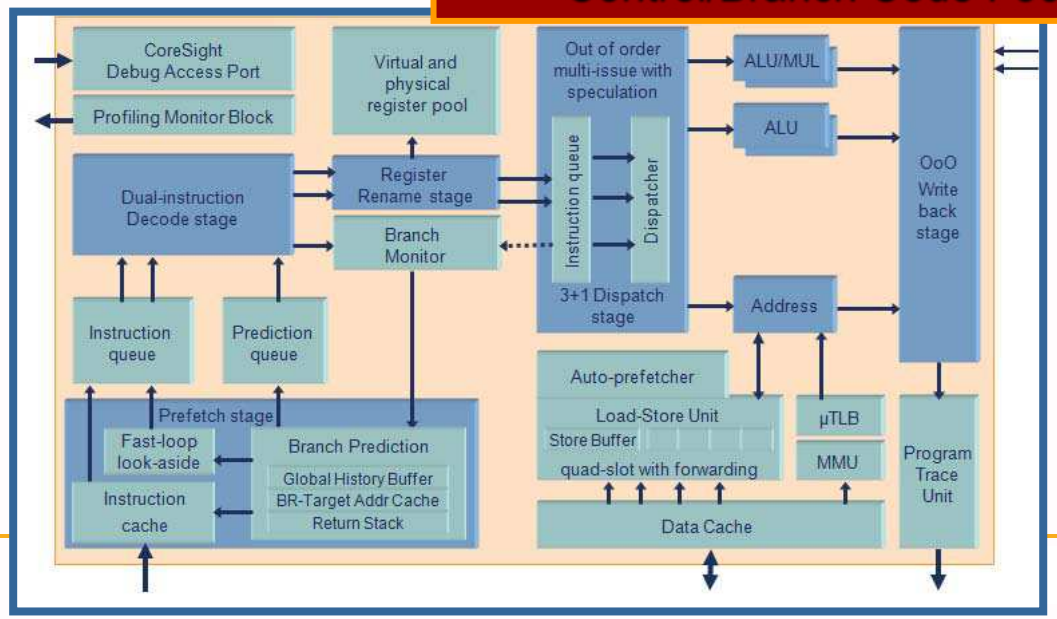
Processors: Instruction and Data Level Parallelism



Cortex
Intelligent Processors by ARM

High Core Level Instruction Parallelism
Control/Branch Code Focus

Cortex-A9 CPU



600MHz to 750MHz CevaX1641 8-way VLIW DSP

- **600MHz to 750MHz Operation**
- **256bit-8 Way VLIW DSP**
  - 8-32bit Parallel Instructions
    - Most common size
  - 16-16bit Parallel Instructions
- **128bit 4/8 MAC SIMD**
  - 4- 16bit x 16bit MACs
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- **Large L1 Memories**
  - 96kB Program RAM
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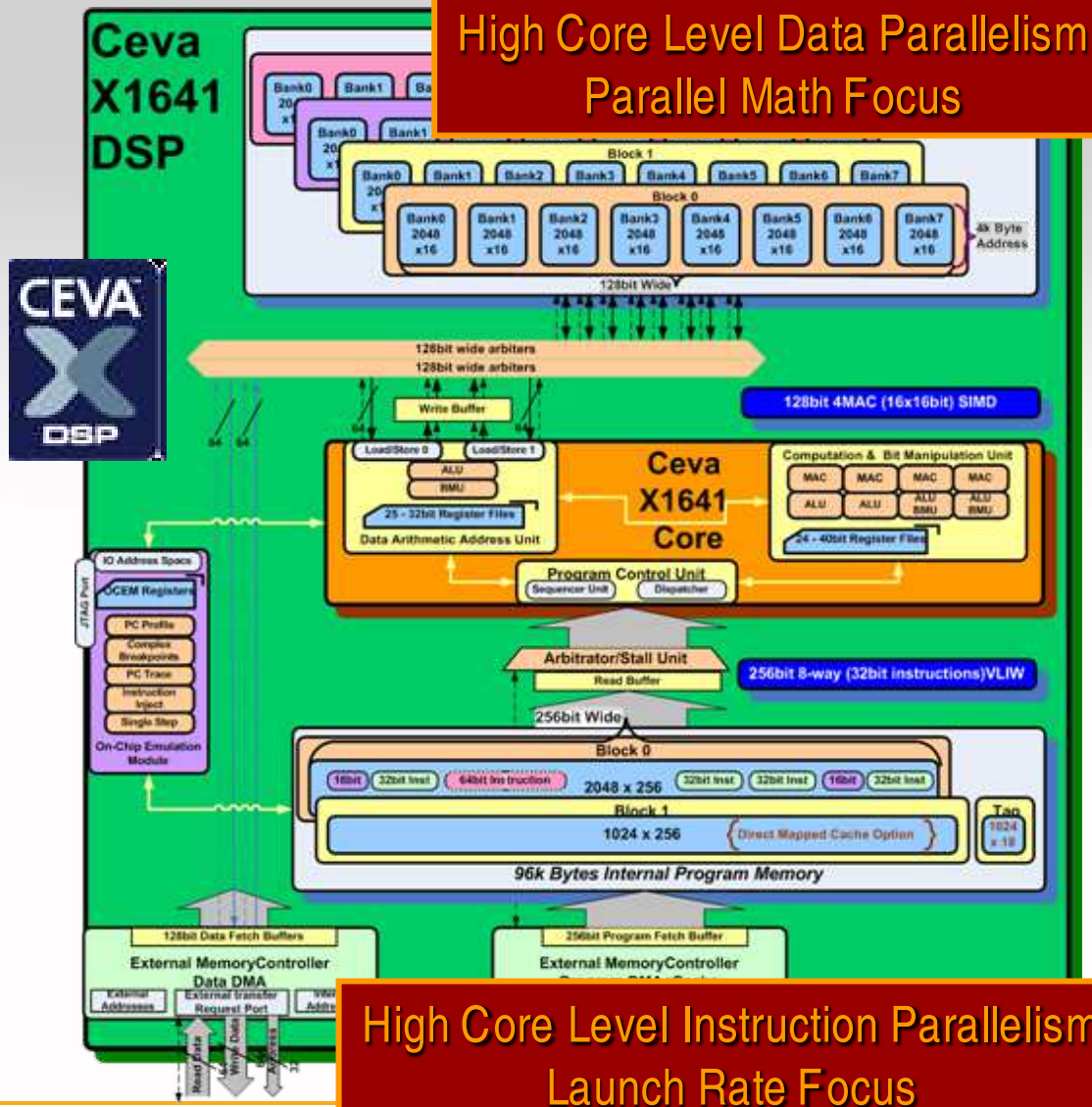
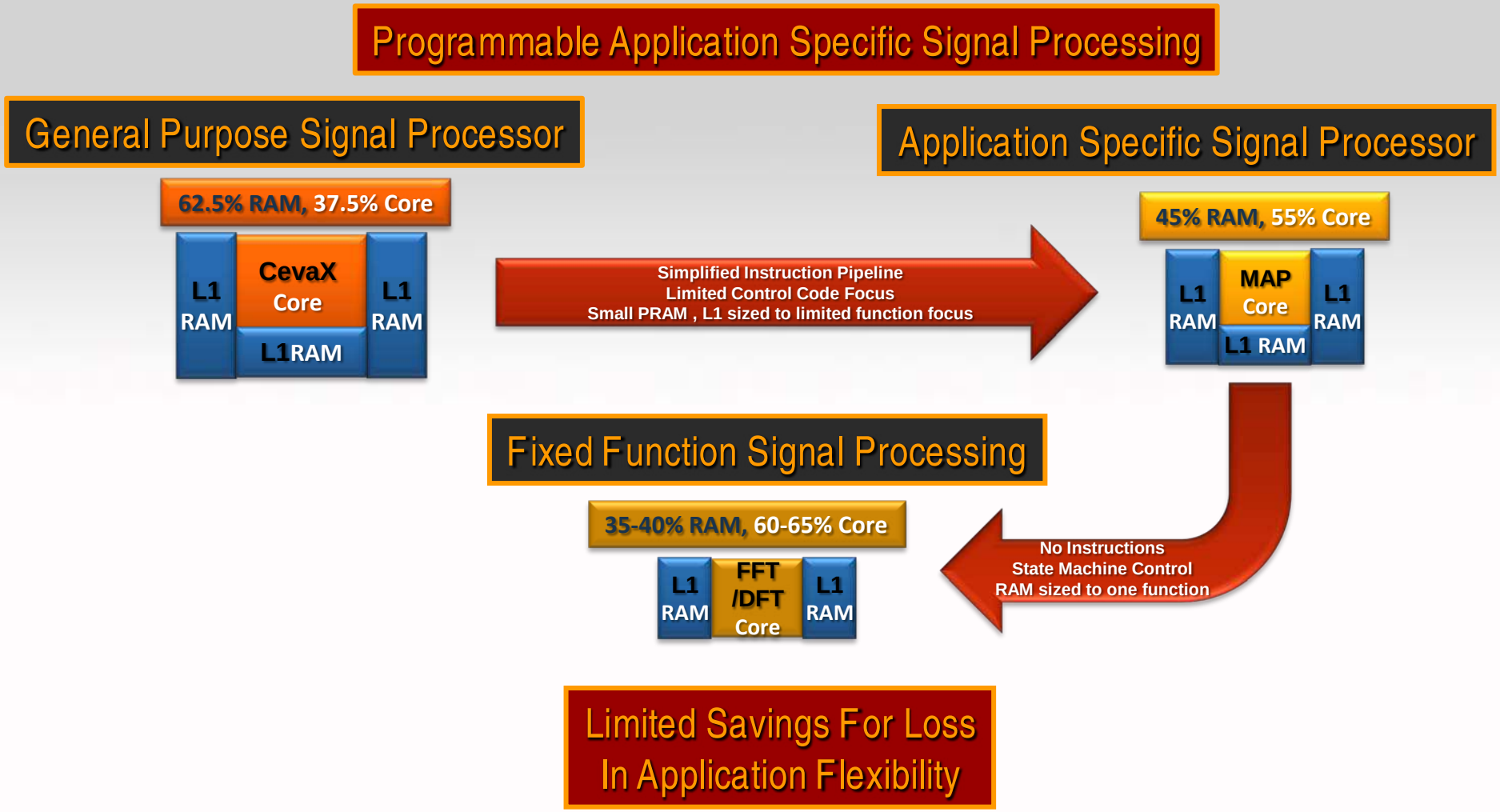
  - Banked Simultaneous Access
- **On-chip Emulation Module**
  - Complex Breakpoints/Trace/etc.
- **Dual Data/Program DMA/Cache**
- **Extensive Tool Chain**
  - C-Compliers/Debugger/etc.

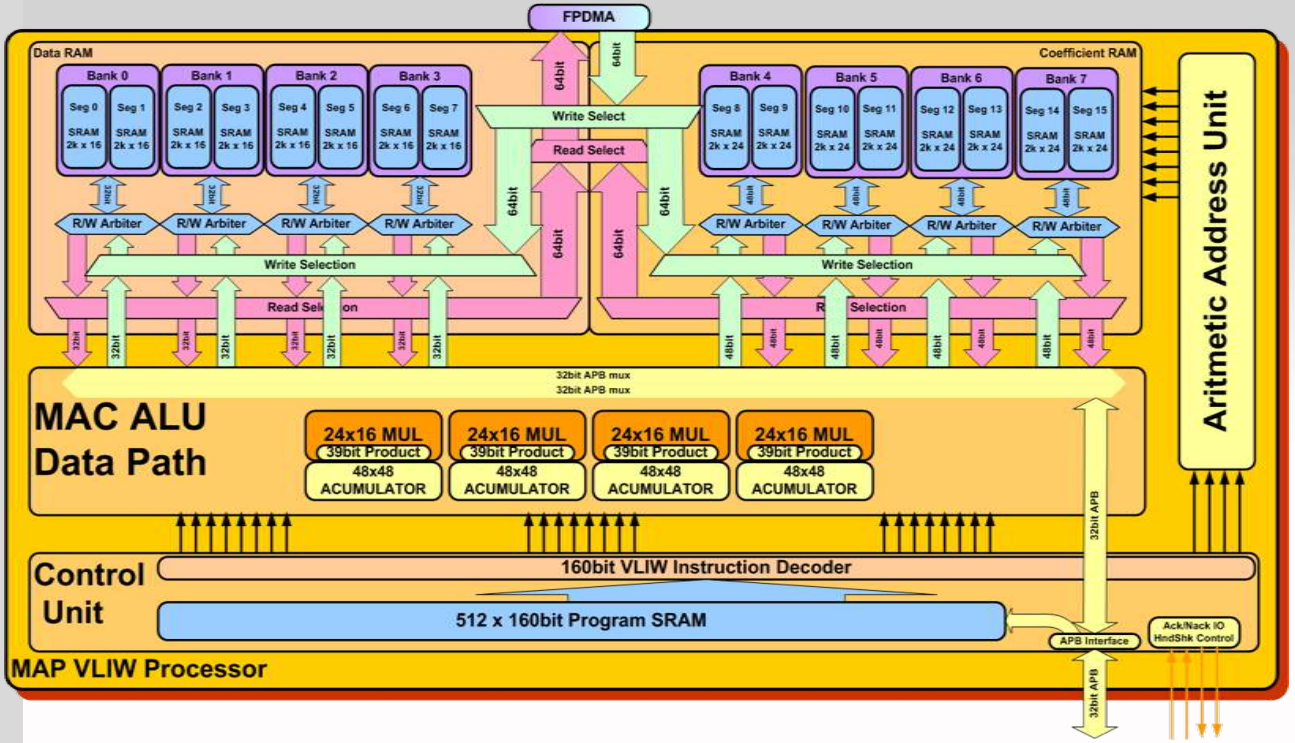


Mindspeed Application Processor

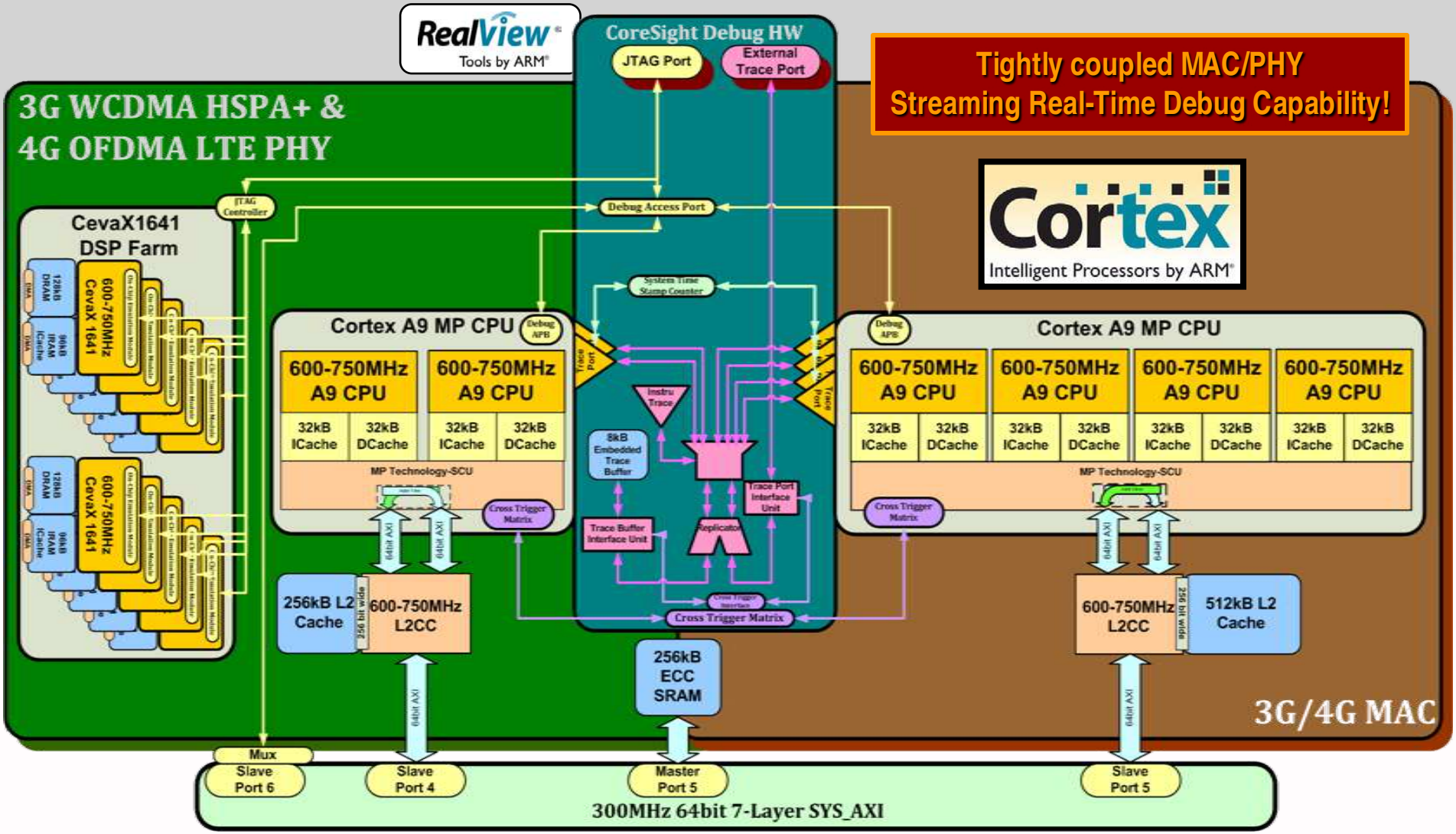


Mindspeed Application Processor (MAP)

- 600MHz to 750MHz Operation
- 160bit-1 Way VLIW DSP
- 160bit 4 MAC SIMD
  - 4- 24bit x 16bit MACs
- Built in FFT Radix Support
  - Bit Reverse Addressing
- Circular Buffering
- Built in Byte Data RAM read
- Very Wide/Large L1 Memories
  - 10kB Program RAM,
  - 80kB Data RAM
  - Banked Simultaneous Access
- External Sequencer Control
- High Performance DMA for Data
- 4G/3G Application Library

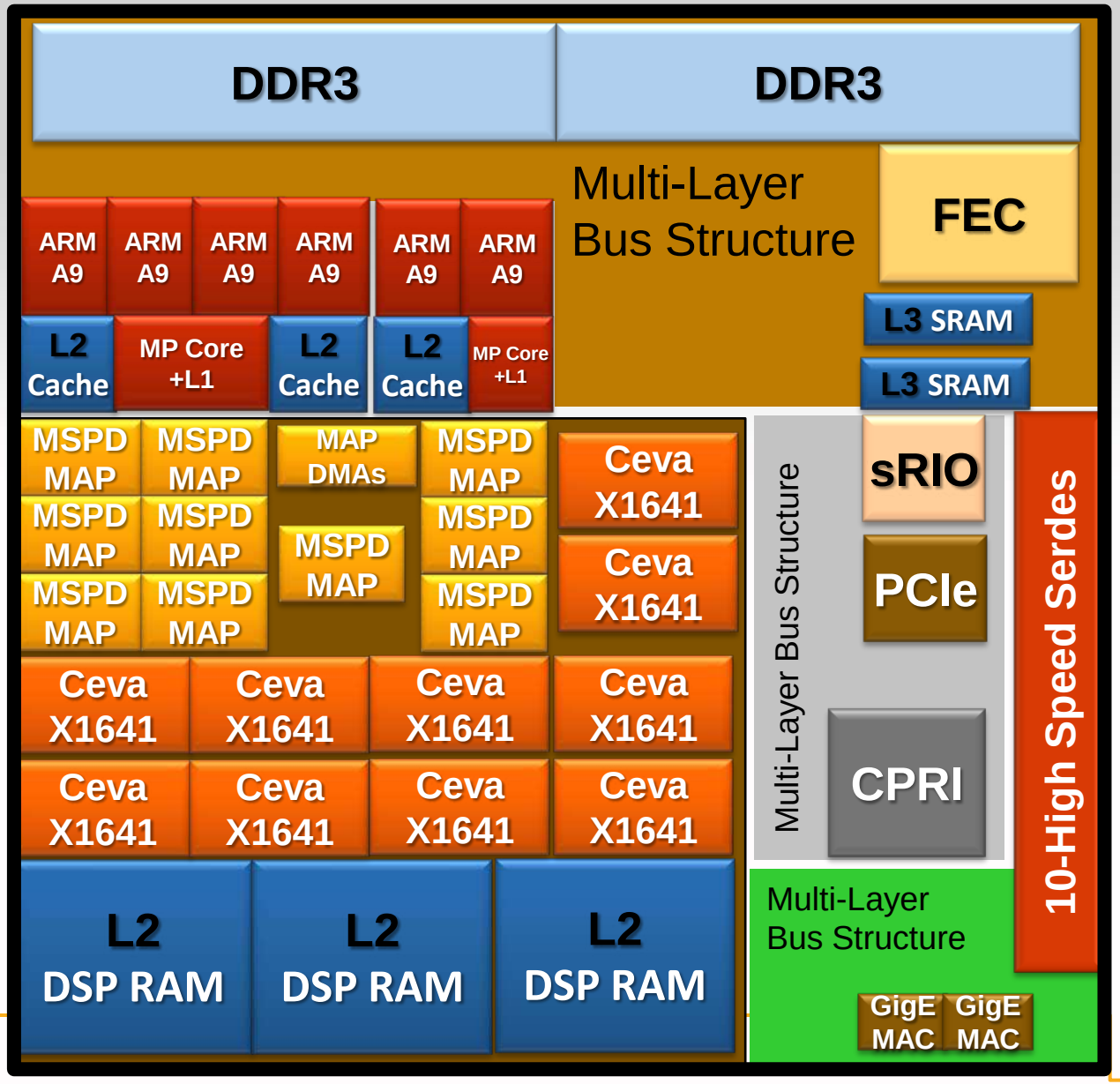


CoreSight™ SoC HW SW Debug Support



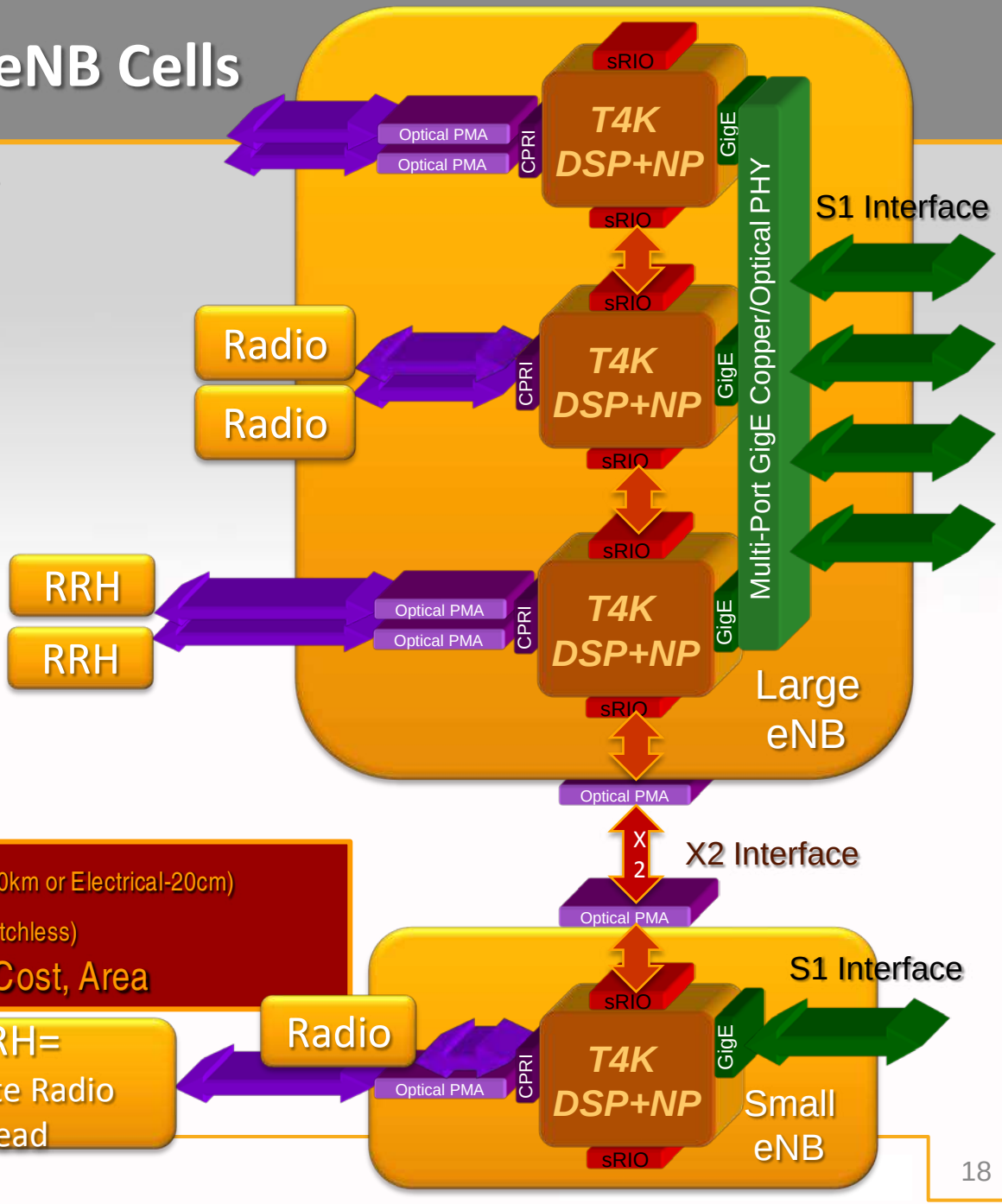
Transcede™ 4000 SoC

- TSMC 40G Process 0.9V
- 12W typical
- 31mm x 31mm
- 26 Processors
- 9.1MBytes RAM
- >300M transistors



Multi-SoC Chaining in eNB Cells

- Each T4k is Chainable to other T4ks
  - Shared Inter-T4k Memory Maps
    - sRIO based HW Bridges
    - T4k(s) Share DDR,SRAM,IO,etc.
  - sRIO Mailbox System For Control
  - sRIO AXI DMA for Data Transfers
- T4k(s) can chain between eNodeBs
  - Create a eNB optical X2 interface
    - sRIO or VPN GigE
- T4k Distributed Antenna Systems
  - CPRI5.0 up to 20km
  - Between BBU and RRH @10GT/s



Chainable Processing Tiles (Optical-20km or Electrical-20cm)
Seamless Scalability (Switchless)
Resulting In Lowest: Power, Cost, Area

RRH= Remote Radio Head

Software Architecture Evolution

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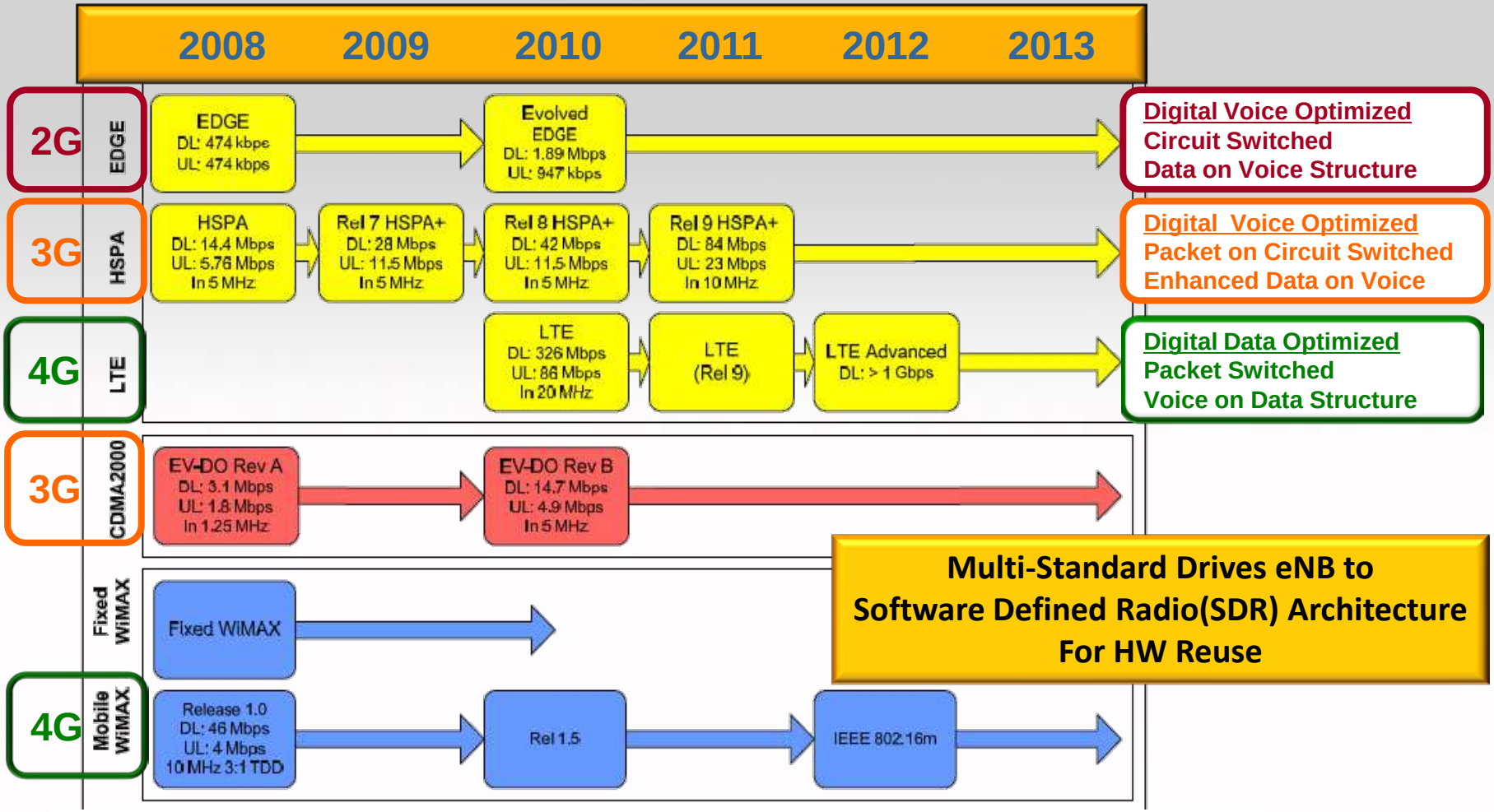
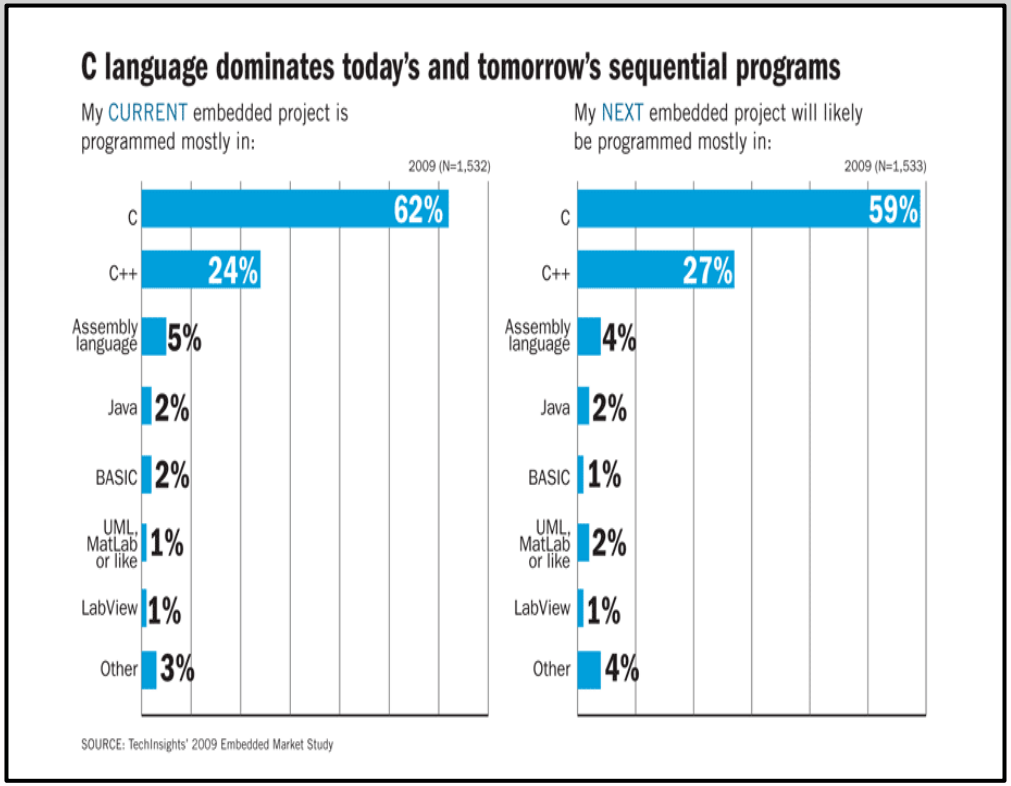
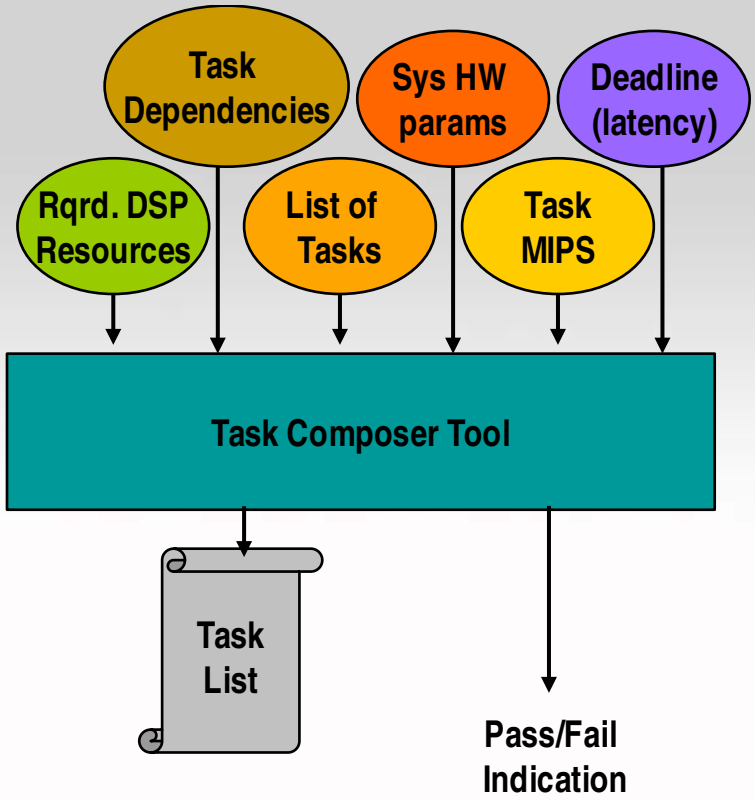
Mobile Data Link Standards Evolution



Notes: Throughput rates are peak theoretical network rates. Radio channel bandwidths indicated.
Dates refer to expected initial commercial network deployment except 2008, which shows available technologies that year.

Innovation in Multi-Core Programming

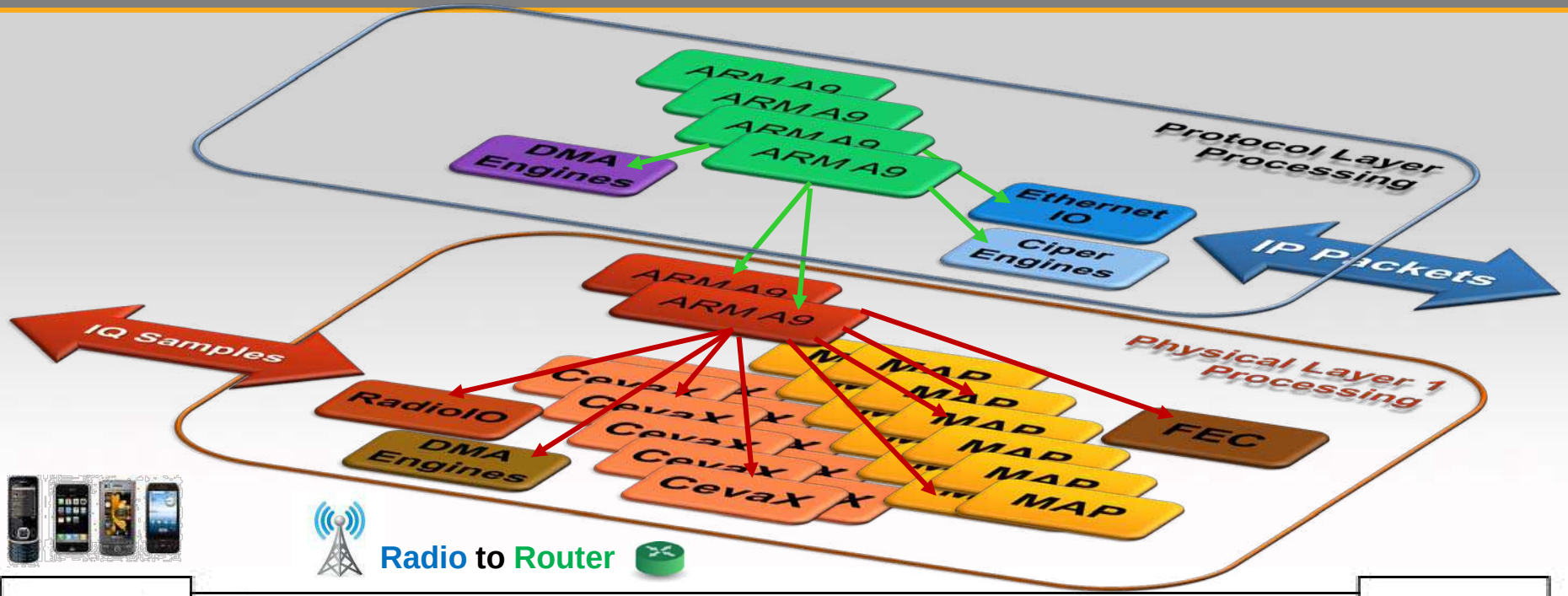




However, C is a sequential language, so how do application developers map their C code into multi-core SoCs?

New modeling approach allows application partitioning and profiling early on in the design phase

Software Multi-Core HW Mapping: LTE PHY & L2



Radio to Router

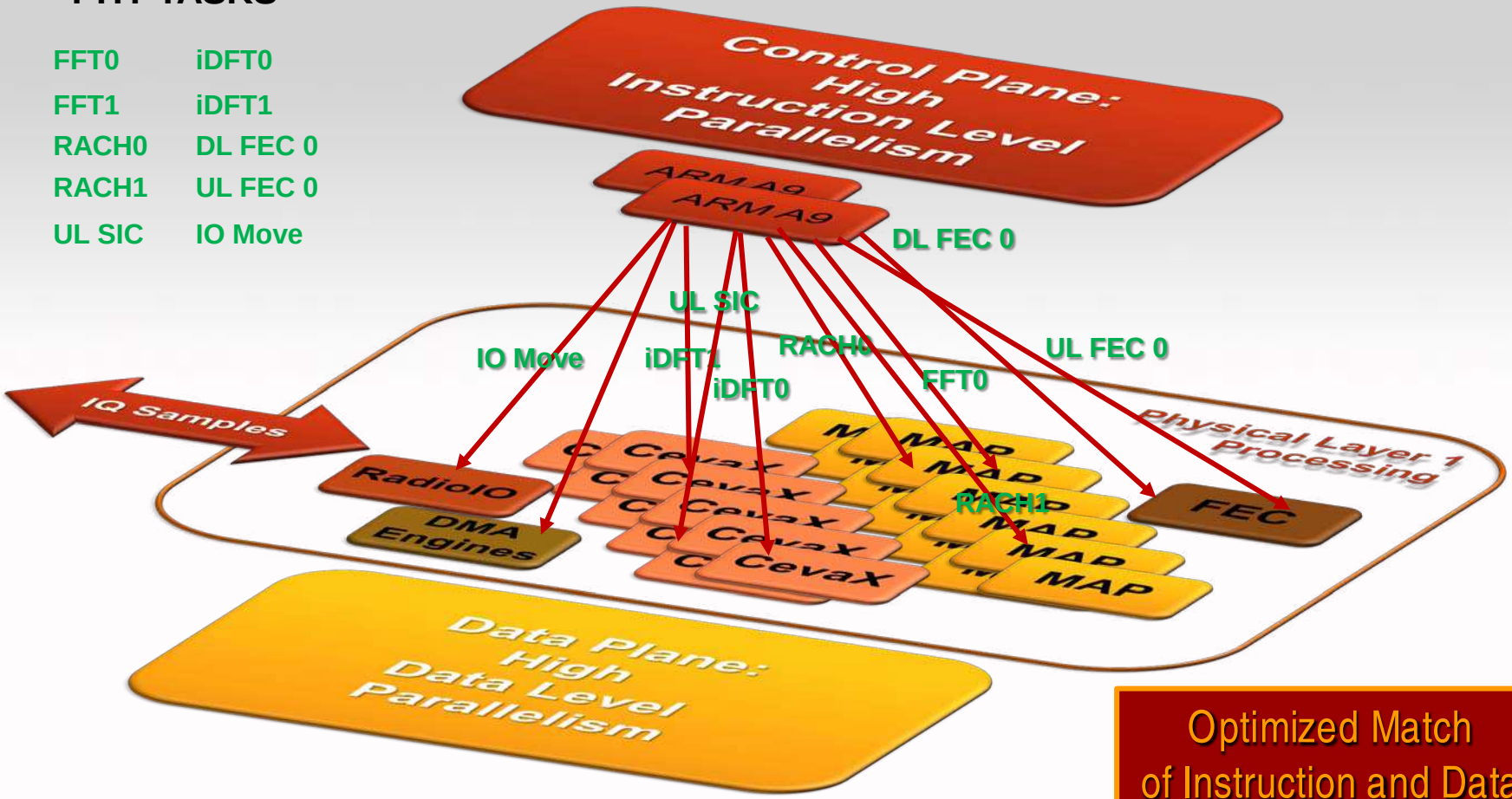
UE		eNodeB			MME
NAS					NAS
RRC		RRC	S1-AP		S1-AP
PDCP		PDCP	SCTP		SCTP
RLC		RLC	IP		IP
MAC		MAC	L2		L2
L1	LTE-Uu	L1	L1	S1-MME	L1

Relay

Software Multi-Core HW Mapping: LTE PHY

PHY TASKS

FFT0	iDFT0
FFT1	iDFT1
RACH0	DL FEC 0
RACH1	UL FEC 0
UL SIC	IO Move



Optimized Match of Instruction and Data Parallelism

Key Differentiators of the Transcede™ Family

- Software configurable for all flavors of LTE, W-CDMA and WiMAX (SDR)
  --- Supports China standards, including TD-SCDMA and TD-LTE
- Significantly reduces system bill of materials
- Integrated L2 and L1 on a single SoC provides lowest possible latency
- Simplified programming model allows easy adaptation
- Roadmap of scalable SoCs delivers a range of performance/cost points across the range of base stations

THANK YOU!