Optical interconnect circuits: some design considerations

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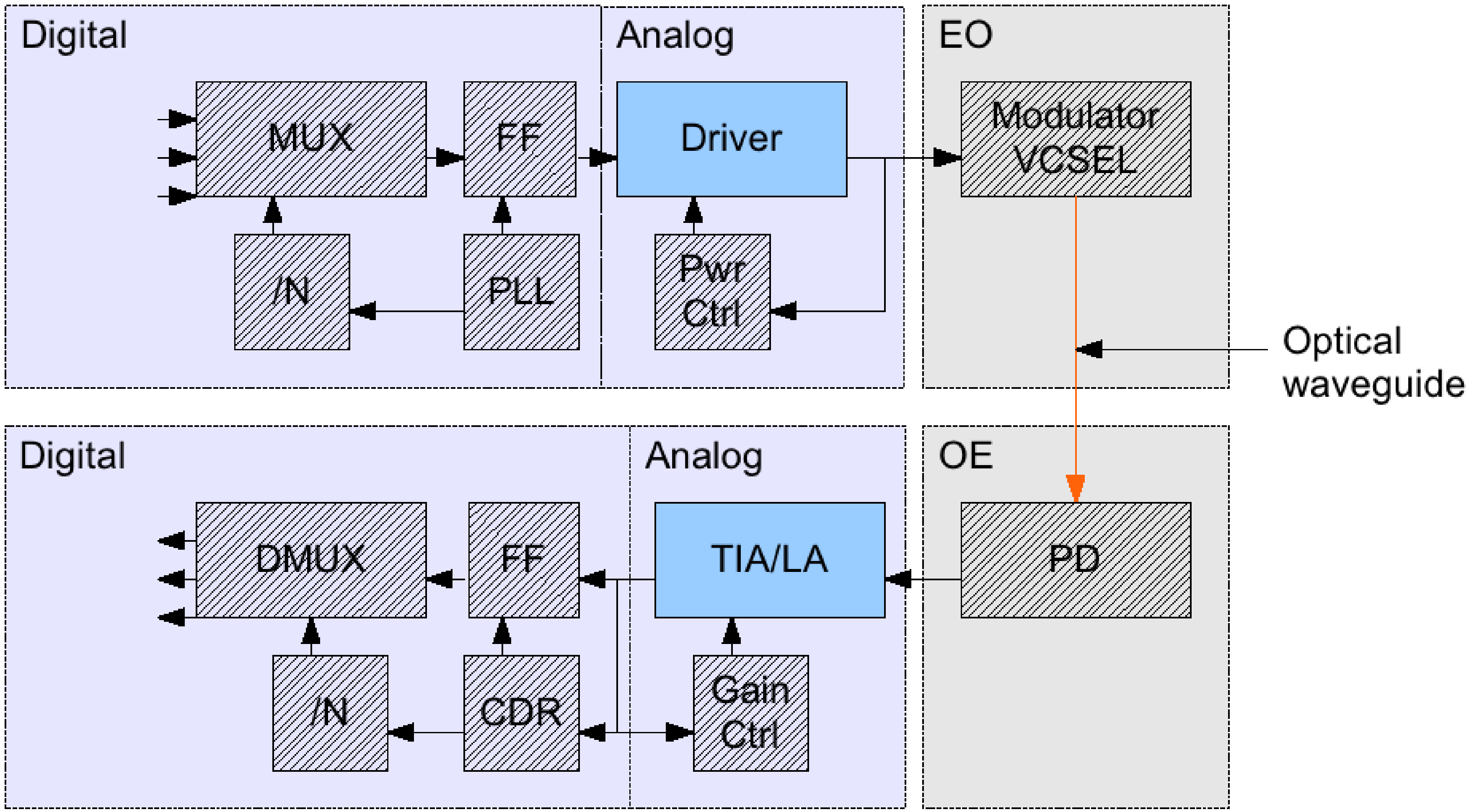
Why consider optics?

- Increased interest in silicon photonic interconnect
  - Potential win in density, energy, BW over wires
- From an architectural view, optics is just another tool
  - Use it if its characteristics give a net “win”
  - But then we need to understand its costs
- This is an introduction to these costs
  - From a circuit/physical design perspective
  - A list of things to consider in a system evaluation

A generic serialized system

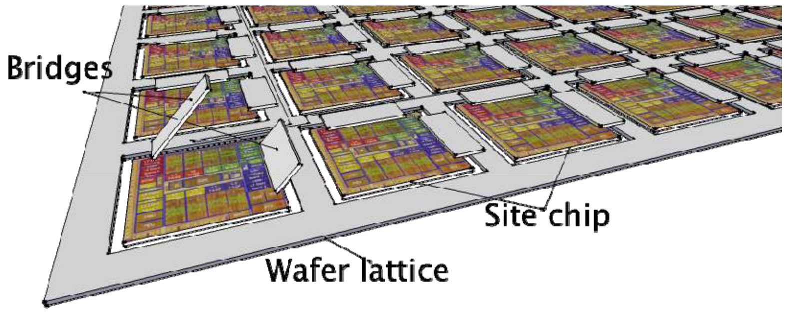
Here we consider just part of the whole system



Designers tweak all parts of this system

Lots of design effort in the CDR, PLL, mux/demux, etc.

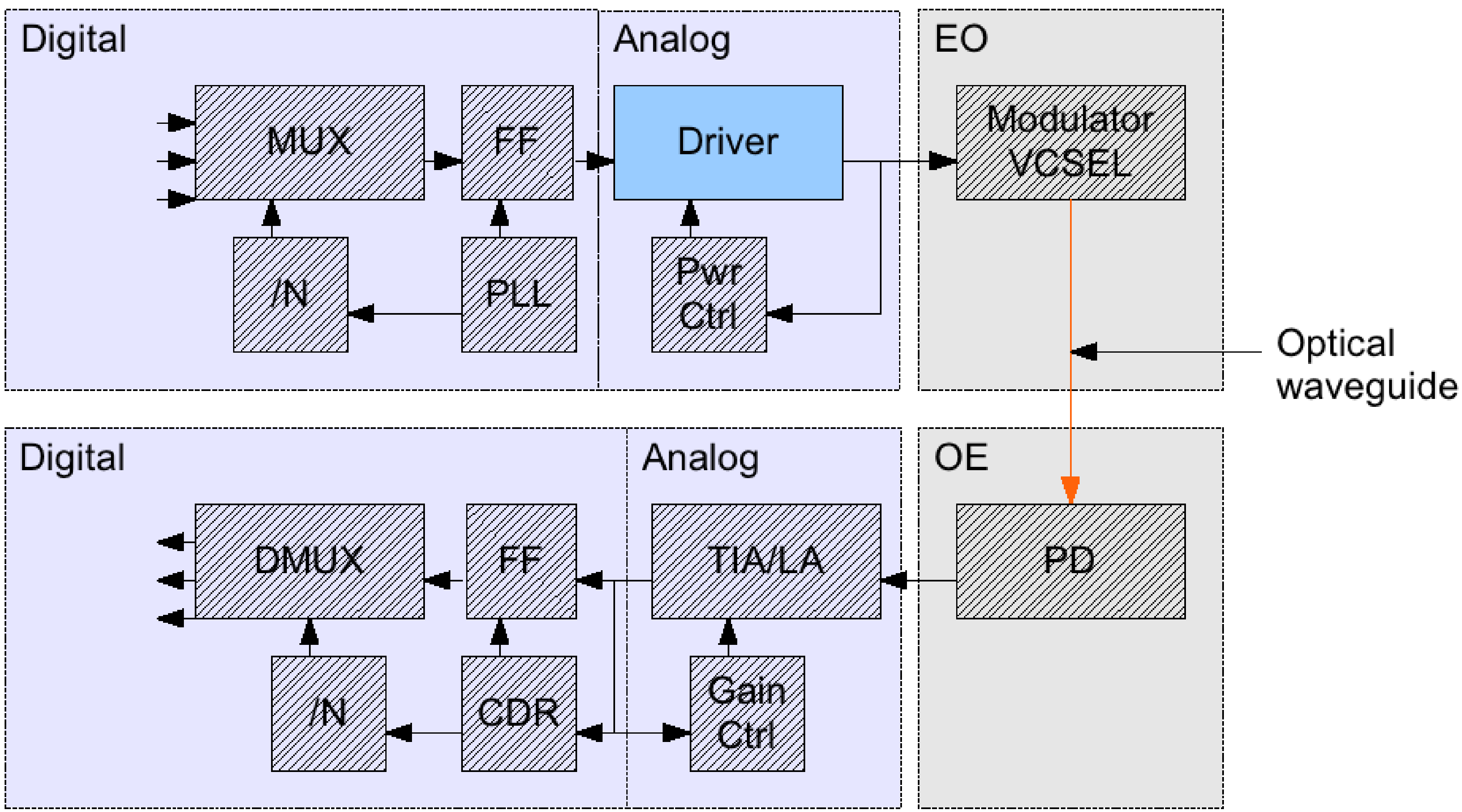
- Link design depends on the architectural use-case
  - Some applications allow system simplifications



- E.g., Oracle's "macrochip"
  - Co-packaged chips sharing a silicon substrate [8]
  - Optical links are inter-chip, but within-package
    - Shared mesochronous clock between RX/TX
    - Use periodic calibration (common time-sense)
    - DWDM has potential for wide parallel I/O

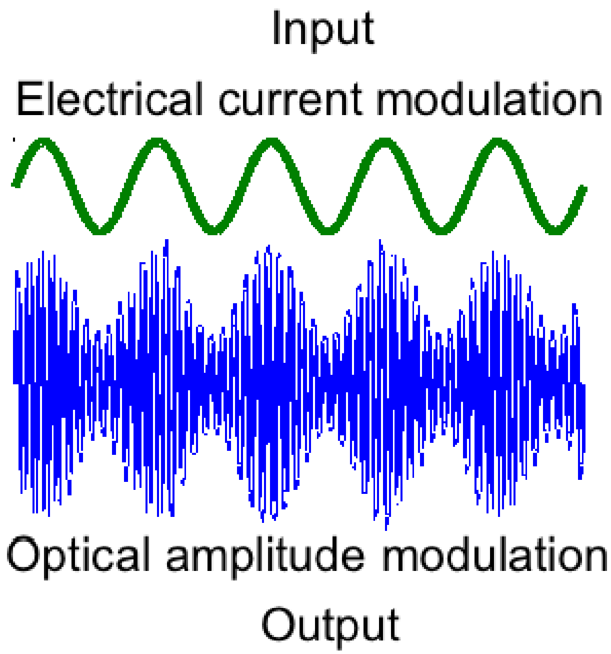
But today we’ll just cover a few simple themes

Start with the driver



Transmitter basics

- TX converts electrical signals into optical signals
- Many device flavors
  - Local light sources
    - VCSELs, LEDs
    - CMOS integration tricky
  - Modulating a remote source
    - MZs, rings, quantum wells
    - Better integration prospects



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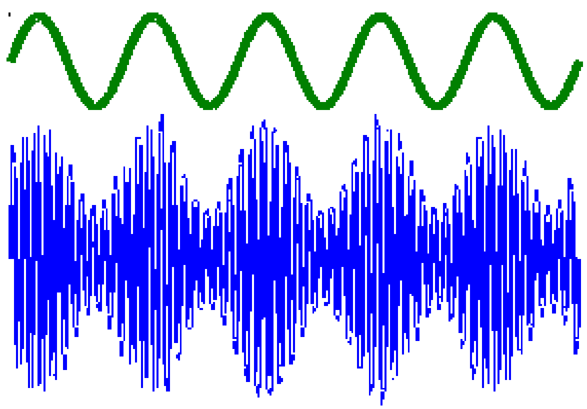
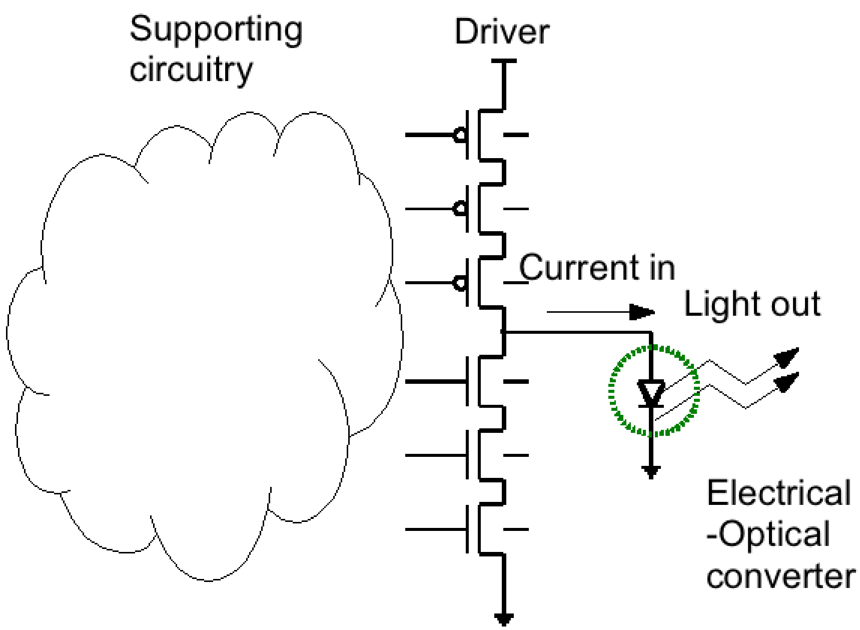


Consider these here

Transmitter basics, con't

Driving ring modulators

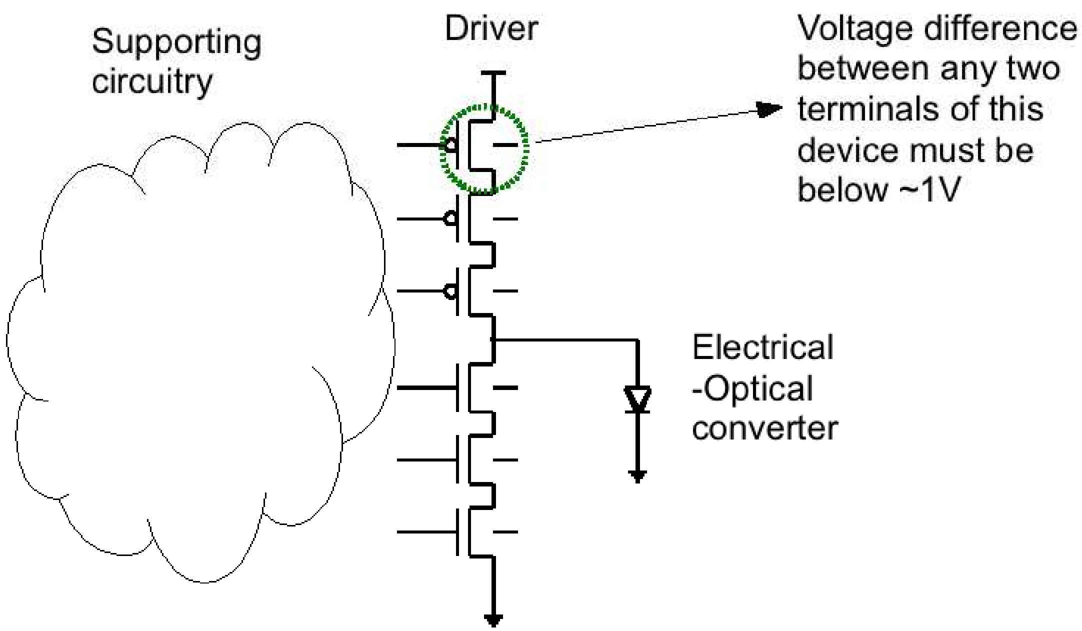
- Good: ring modulators look like a lumped capacitance
  - Simple abstraction for designers; matches CMOS
- Bad: they typically require a high voltage [1]



Transmitter basics, con't

Driving ring modulators

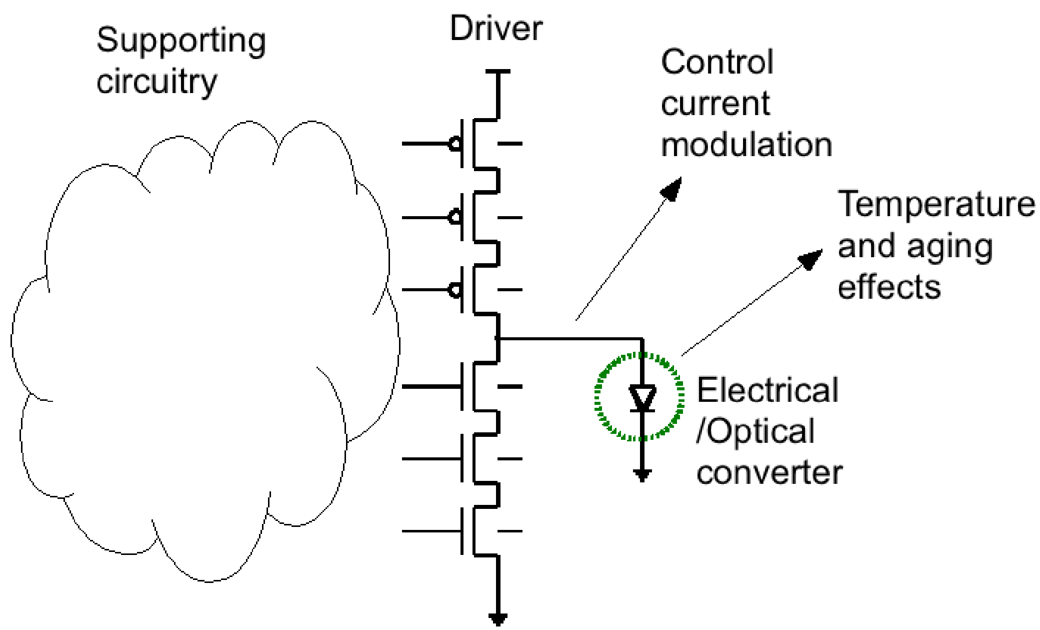
- Fast high voltage switching using low-voltage devices
  - Must take care to protect circuits [2]



Transmitter basics, con't

Driving ring modulators

- Bad: modulators see temperature and aging effects
  - Need driver power and/or environment control [3]



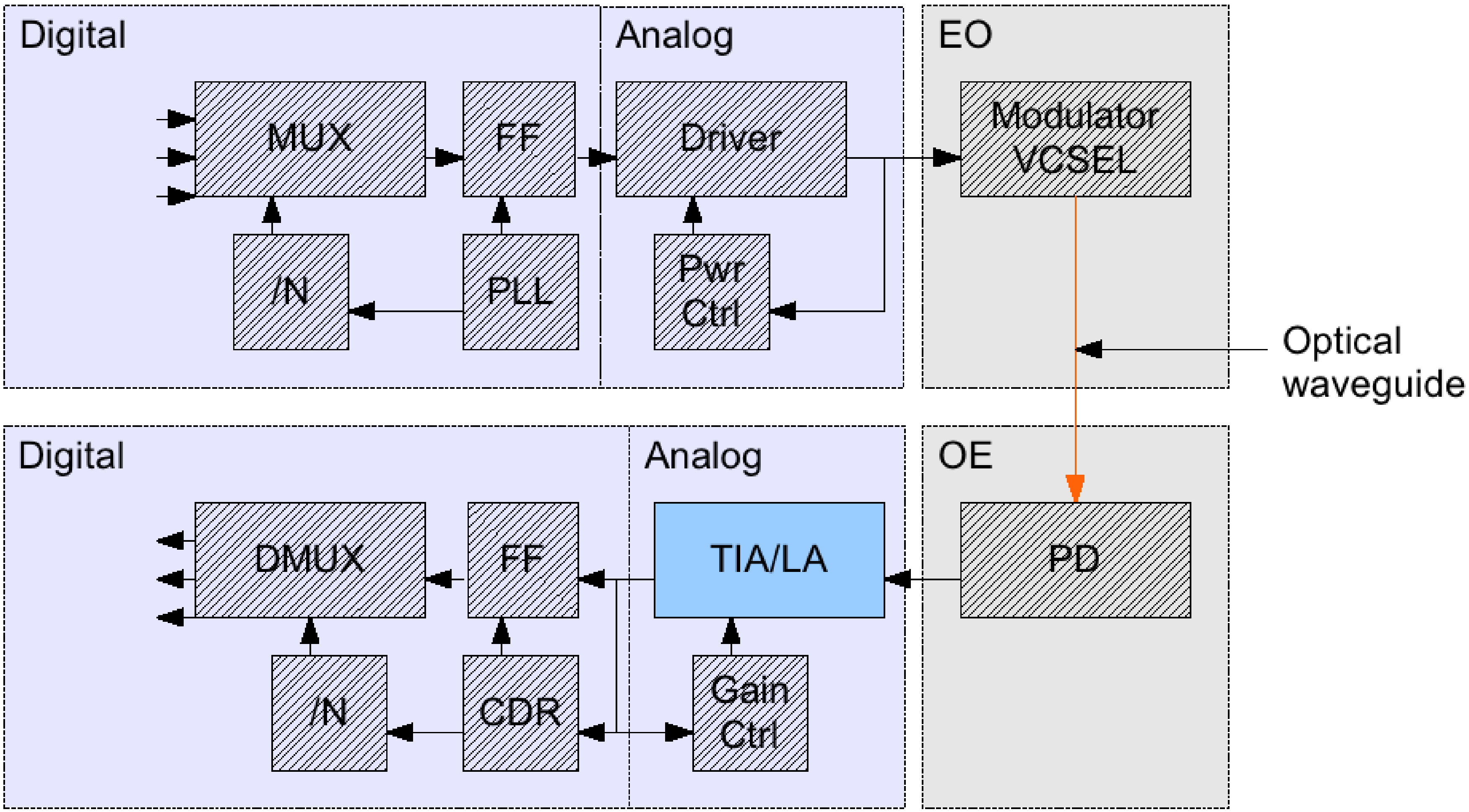
Transmitters and ring modulators

- High-voltage drive is not a very difficult problem
  - At least, it's fairly well understood

- The hard problem is temperature control
  - Rings sensitive to sub-1^{o} K temperature changes
  - Standard solution is to dynamically heat them
    - Is this efficient enough to make rings useful?
    - Until shown (at scale), this is *the* gating issue

Back to the generic system diagram

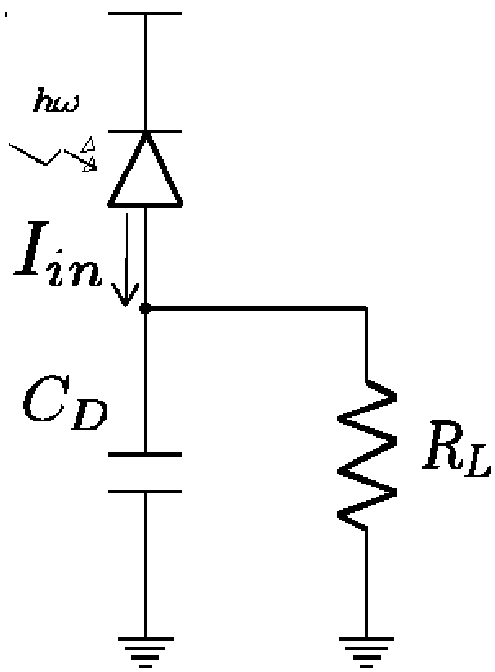
The RX has a different (perhaps more interesting?) set of issues

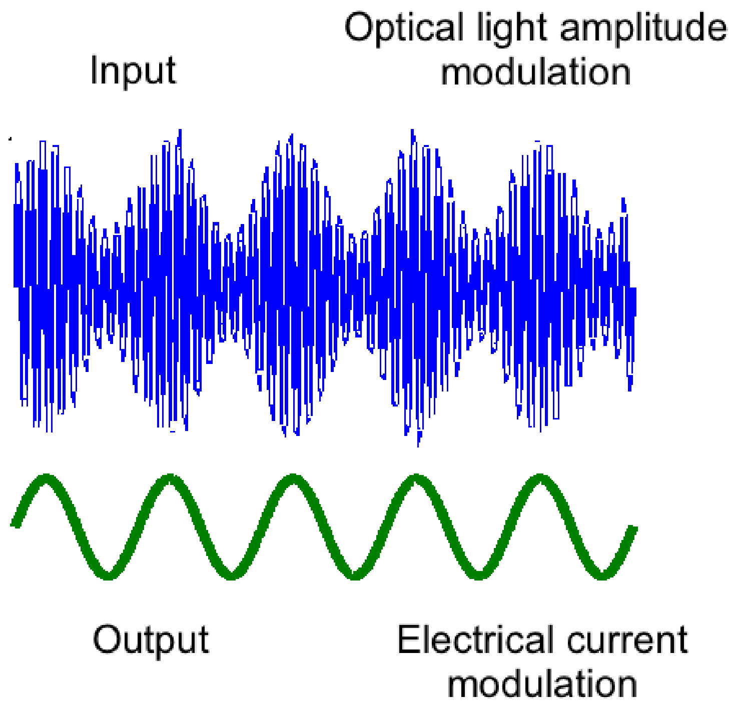


Receiver basics

Let's start with the simplest system possible

- Simple mechanism: photodiode turns light → current
  - "Responsivity" is on order of 1 μA per μW

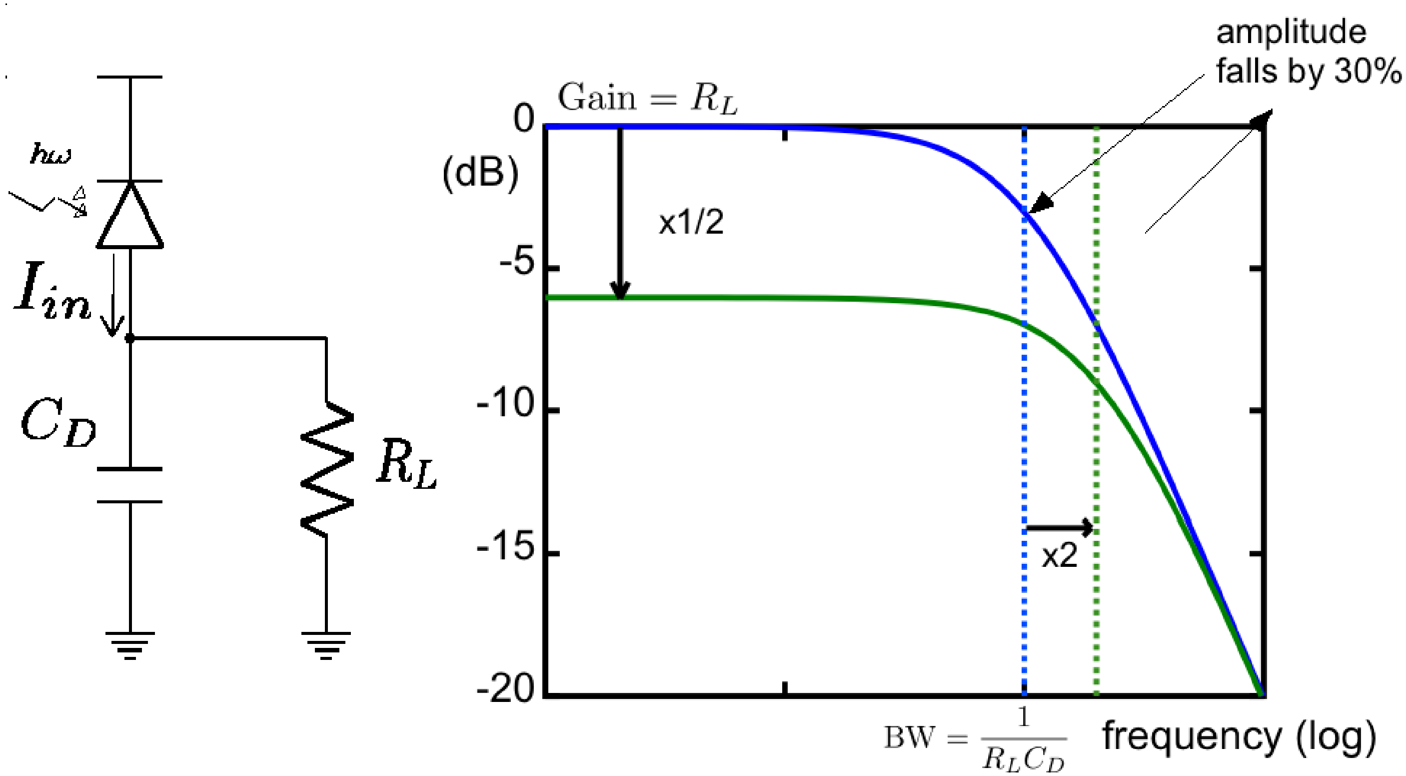




Not surprisingly, this is a simple circuit

Go back to Circuits 101

- Resistor performs a current-to-voltage conversion
  - Capacitor introduces a low-pass filter pole [5]



A key characteristic of any receiver is its SNR

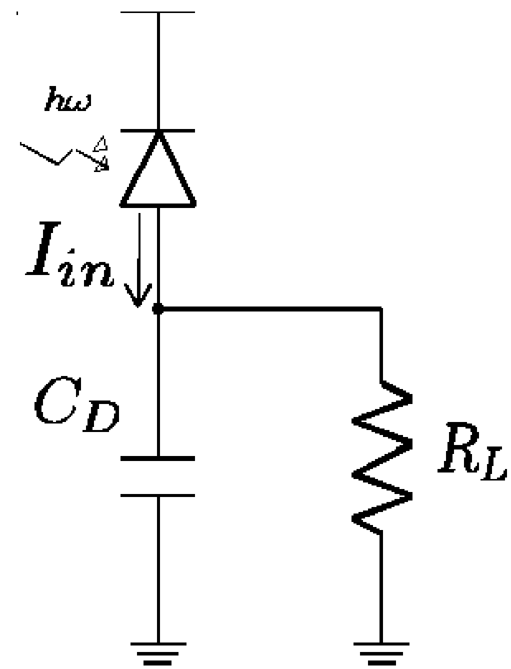
Signal-to-noise ratio

Thermally induced voltage fluctuations

- For this receiver, SNR is relatively simple

$$\mathrm{BW} = \frac{1}{R_L C_D} \qquad \mathrm{Gain} = R_L \qquad \mathrm{Noise} = \frac{kT}{C_D}$$

$$\boxed{\mathrm{SNR} = \frac{I_{in}^2 R_L^2}{\frac{kT}{C_D}} = \frac{I_{in}^2}{kTC_D \mathrm{BW}^2}}$$

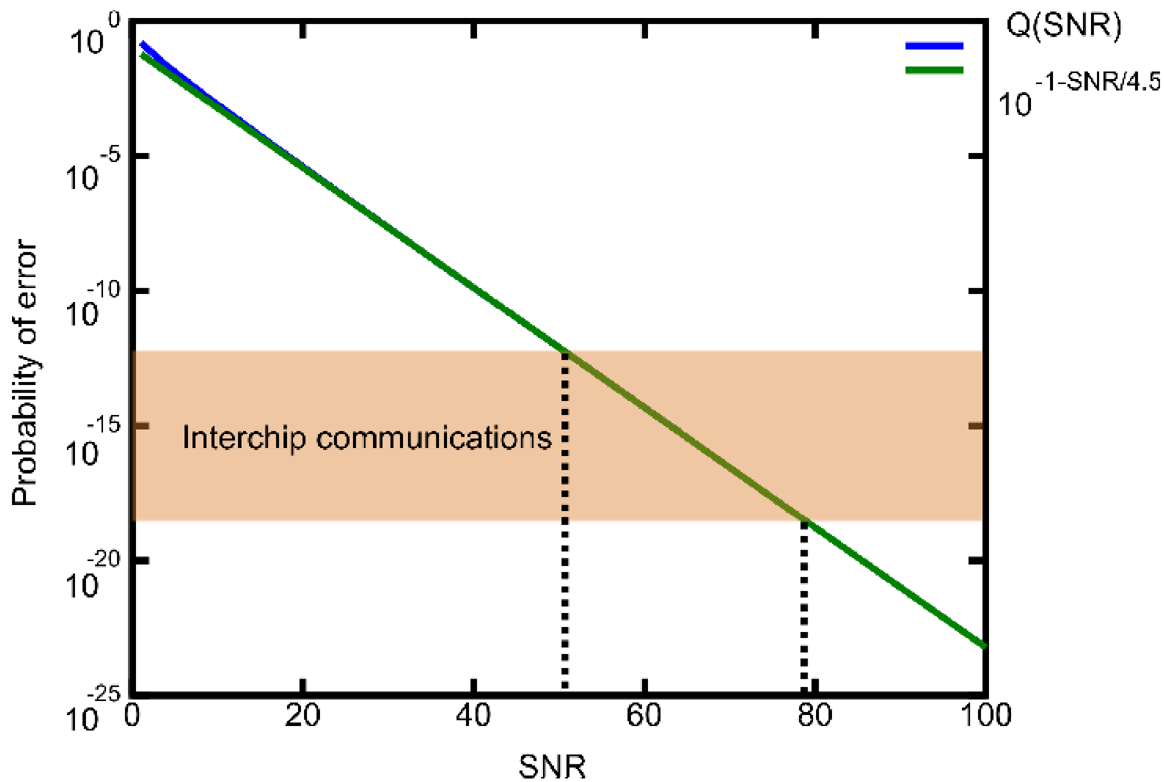


- Note that SNR is independent of R_L
  - For a fixed BW and C_D

Why do we care about SNR?

(If it were *really* important, wouldn't the internet cease to exist?)

- Larger SNR → smaller probability of error
  - A reasonable estimate of BER: $10^{-SNR/4.5}$



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SNR example

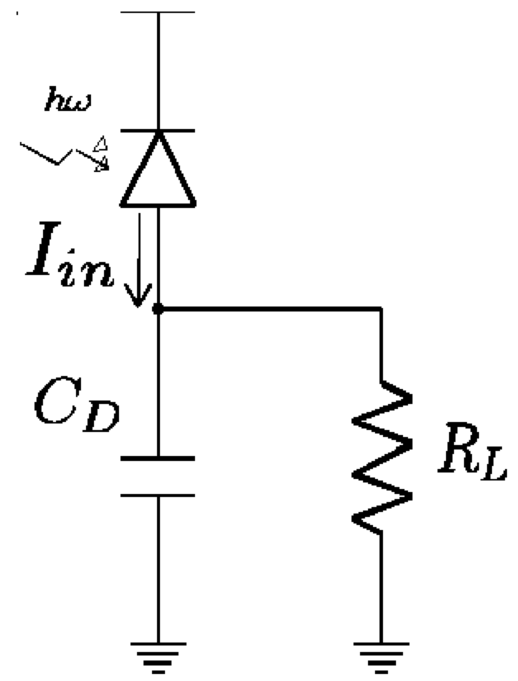
Signal-to-noise ratio

- Let's pick some interesting numbers

$$\mathrm{BW} = \frac{1}{R_L C_D} \qquad \mathrm{Gain} = R_L \qquad \mathrm{Noise} = \frac{kT}{C_D}$$

$$\mathrm{SNR} = \frac{I_{in}^2 R_L^2}{\frac{kT}{C_D}} = \frac{I_{in}^2}{kTC_D \mathrm{BW}^2}$$

$$\left.\begin{aligned} \mathrm{BW} &= 2\pi \times 4\mathrm{GHz} \\ C_D &= 50\mathrm{fF} \\ I_{in} &= 10\mu\mathrm{A} \end{aligned}\right\} \mathrm{SNR} = 760$$

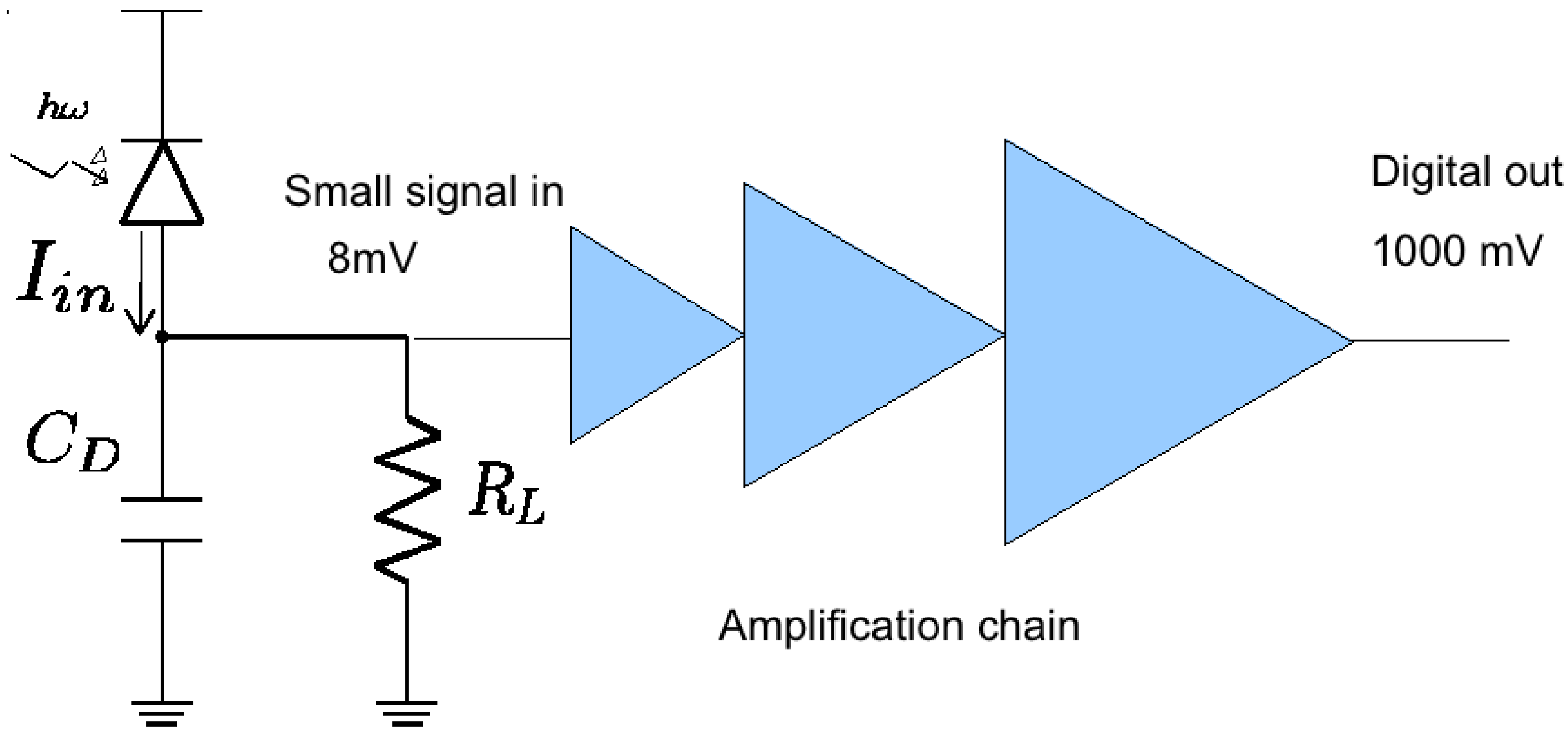


- This is huge! So what's the catch?

The catch is that the gain is too small

Cascaded amplifiers (to get a ~1V signal at the output) degrade the SNR

- Noise of the cascade is set by noise of the 1st stage
  - So concentrate on a low noise factor 1st stage



But how do we get more gain in the first place?

Big BW requires small capacitance and small resistance

- Recall that

$$\mathrm{BW} = \frac{1}{R_L C_D} \qquad \mathrm{Gain} = R_L$$

- So in this case, R_L (=gain) must be at most 800Ω
  - An input signal of 10 μA turns into at most 8 mV
  - For more signal you need more R_L—and go slower
- R_L tightly couples signal gain and bandwidth
  - How can we decouple these two?
  - Answer: with amplification and feedback

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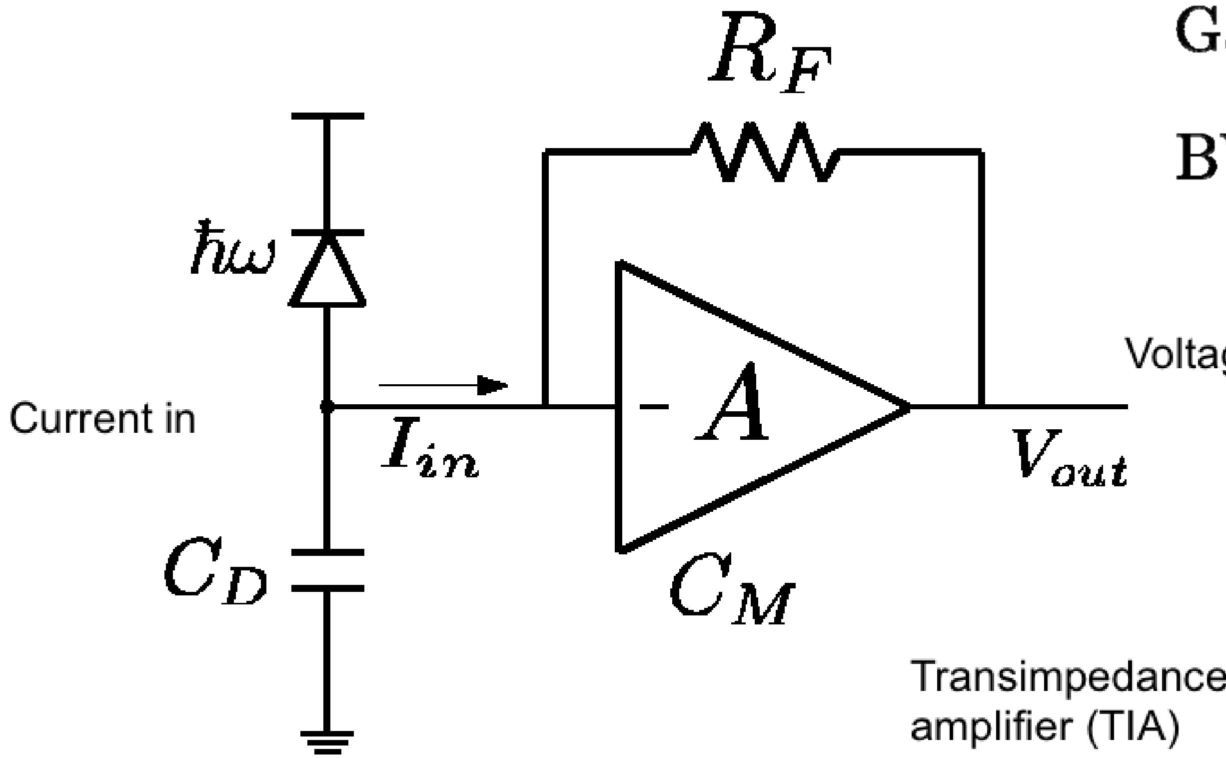
An example first-stage amplifier

A “textbook” transimpedance amplifier (TIA)

- For an equivalent BW, the gain has gone up by *A*
  - But at what cost? What about noise?

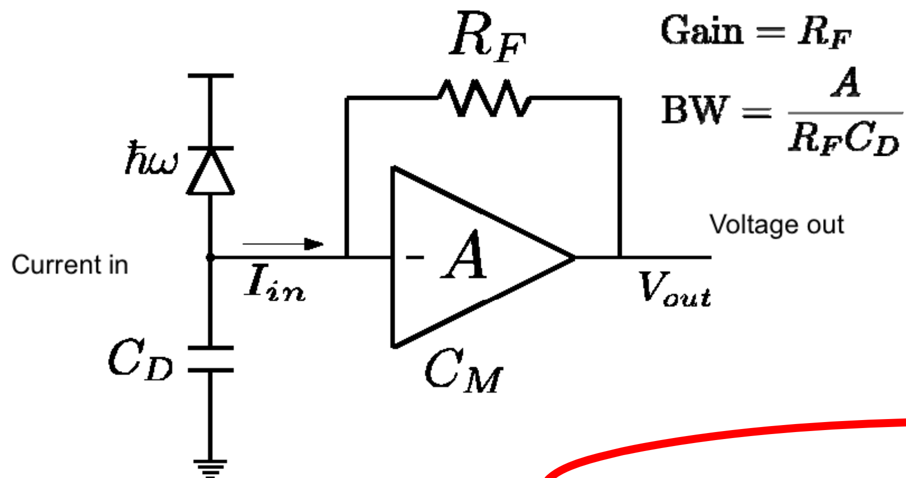
$$\text{Gain} = R_F$$

$$\text{BW} = \frac{A}{R_F C_D}$$



"There ain't no such thing as a free lunch"

- The amplifier degrades SNR
  - Basic trade-offs independent of amplifier topology



$$\mathrm{SNR} = \frac{I_{in}^2}{kTC_D\mathrm{BW}^2} \times f\left(\frac{C_M}{C_D}, \frac{\mathrm{BW}}{\omega_T}\right)$$

Relative size of input stage w.r.t. input capacitance

Technology parameter

What does this mean?

$$\text{SNR} = \frac{I_{in}^2}{kTC_D\text{BW}^2} \times f\left(\frac{C_M}{C_D}, \frac{\text{BW}}{\omega_T}\right)$$

Relative size of input stage w.r.t. input capacitance

Technology parameter

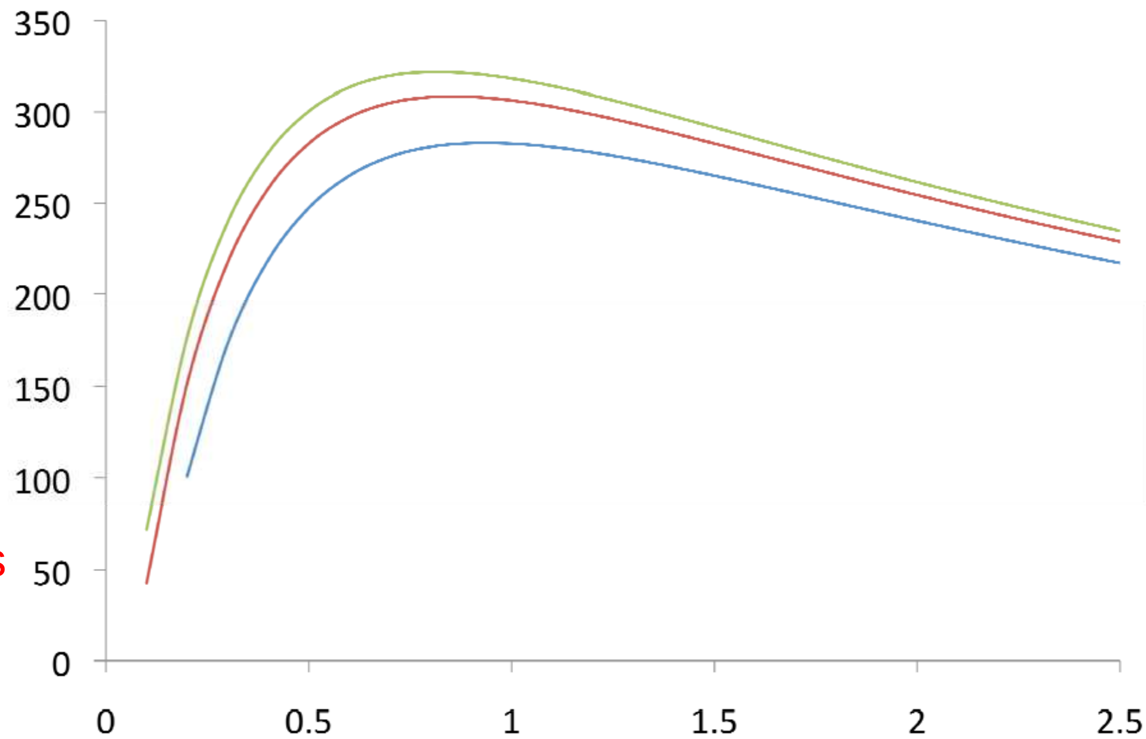
- SNR relationship shows the fundamental tradeoffs
  - Between BW, input capacitance and input signal
  - This applies to the vast majority of RX topologies
- The function f is of secondary importance
  - Can be derived analytically for simple TIA designs
  - See discussion in [7]

SNR degradation from an inverter amplifier

The actual amplifier topology does not change the results a lot

- At optimal $\frac{C_M}{C_D} = \frac{1}{\sqrt{2}}$, SNR degraded by nearly 3X

C_M/C_D falls: SNR falls b/c small devices are noisy



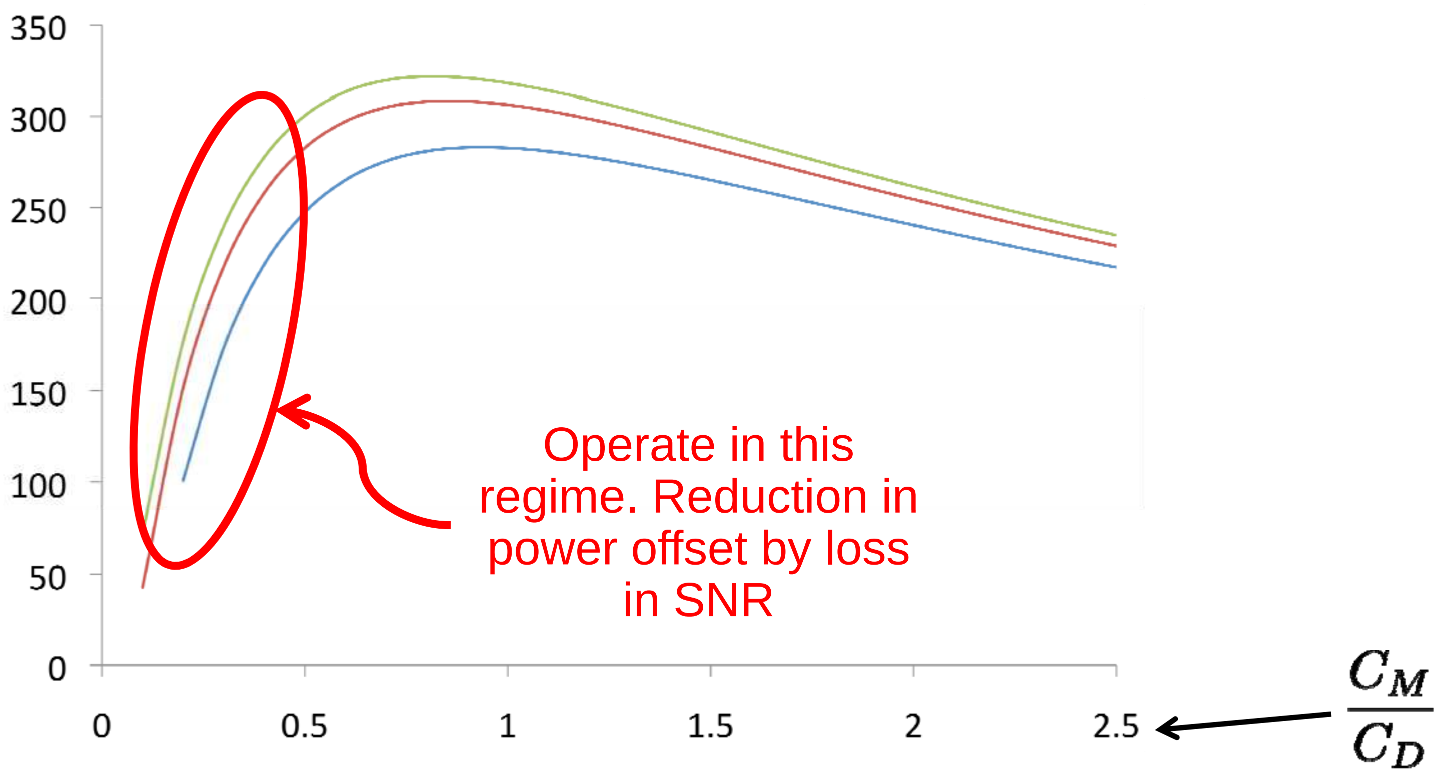
C_M/C_D rises: SNR falls b/c larger input cap requires smaller feedback resistor and hence more thermal noise

$\frac{C_M}{C_D}$

Operating under power constraints

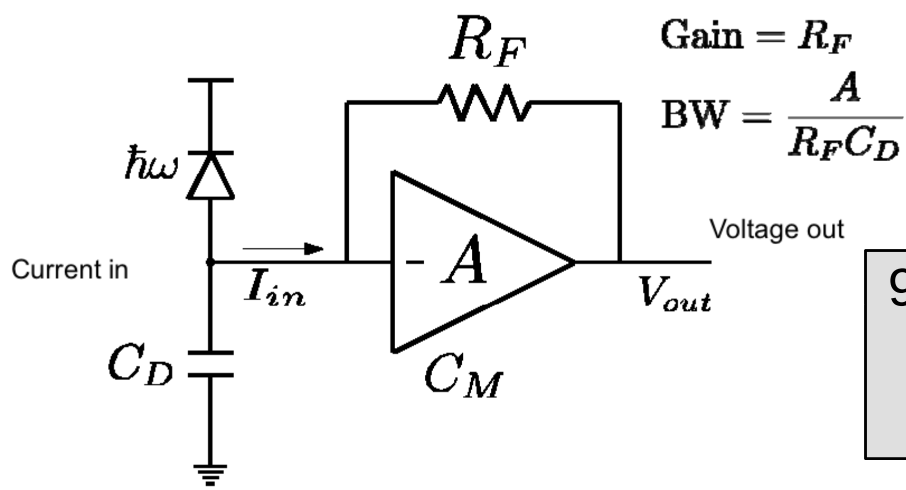
We don't usually operate at the condition for optimal SNR

- Under power constraints, we pick a required SNR
  - Let that set the power (i.e., the ratio C_M/C_D)



Capacitance ratio C_M/C_D is a proxy for power

- For optimum SNR, the amplifier power is constrained
  - Fixed by the parasitic capacitance C_D



90nm @ 4Gb/s
SNR=50
200 fJ/b [6]

$$\text{Power} = \left(\frac{C_M}{C_D}\right)_{opt} \times C_D \times \frac{1\mu\text{m}}{1\text{fF}} \times \frac{150\mu\text{A}}{1\mu\text{m}} \times V_{\text{DD}}$$

Bottom line

- TX, RX circuits consume 2/3rds of optical link energy
  - About 1/3rd for each
- TX: Control of temperature and aging effects critical
- RX: For a given Prob(Error) target
  - There is a fixed SNR, and
  - There is a fundamental tradeoff between
    - SNR, signal, bandwidth, and input capacitance
  - Input capacitance is a proxy for power

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  - Microelectronic Circuits, Sedra and Smith
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