Nonvolatile Memory Seminar
Hot Chips 2010

Aurangzeb Khan
Citius Consulting Group, LLC

Dan Lenoski
Cisco Systems, Inc.

August 22, 2010
Memorial Auditorium
Stanford University

Motivation

- **Flash: Extraordinary growth / scale**
  - NVM: Boot code, look-up tables or configuration data
  - Flash: pervasive / enabling; ubiquitous in digital consumer electronics
    - Annual cost reductions of 50% to 30% (2005-2009, 2010-2013)
    - 15 years ship first 0.5B ICs (1991-2006) → 3 years next 1B ICs (2007-2009) → 2 years next 1B ICs
  - Growing/new applications: consumer, mobile, SSDs, NVM for system memory hierarchy…

- **Emerging challenges, potential solutions**
  - Density scaling, performance, endurance, latency…
  - Architecture / software / controller, wear leveling, more bits per cell, 3D,…

Source: SanDisk Investor Day Presentation, 2/26/10

Motivation

- ## NVM technologies in development

  – Phase Change Memory

  – 45nm 1 Gb (ISSCC2010); scalability, performance, latency, bit alterable writes; reset current, localized heat, (finite) # write cycles…

  – MRAM

  – 4Mb-16Mb in production; no wear-out, bit-level read/writes; spin torque → scalability (reduce switching currents); materials science…

  – RRAM

  – Scalability, performance; reset currents, materials science…

- ## Growth drivers

  – SSD opportunity; system requirements, technical challenges

  – Storage class memory → NVM-enabled system performance

Topics

Time			Topic	Presenters
9:00 AM	-	9:10 AM	Introduction	**Aurangzeb Khan** (Citius Consulting), **Dan Lenoski** (Cisco Systems)
9:10 AM	-	9:50 AM	Managing the Evolution of Flash: beyond Memory to Storage	**Tony Kim** Director, Technical Marketing Mobile/Flash Solution Team Lead Samsung Semiconductor, Inc.
9:50 AM	-	10:30 AM	Forging a Future in Memory — New Technologies, New Markets, New Applications	**Ed Doller** V.P. & Chief Memory Systems Architect Corporate Vice President Micron Technology, Inc.
10:30 AM	-	10:45 AM	Break	
10:45 AM	-	11:15 AM	Status and Prospect for MRAM Technology	**Dr. Saied Tehrani** Chief Operating Officer Everspin Technologies, Inc.
11:15 AM	-	11:45 AM	Memory Overview and RRAM Materials Development at SEMATECH	**Dr. Paul Kirsch** Director, Front End Process SEMATECH
11:45 AM	-	12:15 PM	The Inevitable Rise of Nonvolatile Memory in Computing	**Jim Handy** Founder/President Objective Analysis
12:15PM	-	1:00 PM	Storage Class Memory: Technology, Systems and Applications	**Dr. Richard Freitas** IBM Almaden Research Center IBM Corporation

Supplemental information

Nonvolatile Memory Seminar
Hot Chips 2010

August 22, 2010
Memorial Auditorium
Stanford University

NVM Seminar - Abstract

The exceptional rate of improvement in flash memory density and price performance over the past decade has enabled consumer electronics products which are ubiquitous today but were impractical a few years ago. Flash memory is now making a strong impact on enterprise class storage systems also and, with continuing improvements in storage density coupled with closer integration with systems software to manage the technology, appears to be well-positioned for continued growth in current and new applications.

Over the same timeframe, emerging technologies for nonvolatile memory - which emphasize different aspects of the nonvolatile technology/attributes spectrum - have made substantial progress: phase change memory has demonstrated gigabit levels of density this year; magnetoresistive RAM (MRAM) has become a commercial technology and resistive RAM promises high performance and density capabilities. The capabilities of these nonvolatile memories have the potential to enable new applications and improve system products substantially.

In the semiconductor technology presentations in this seminar, nonvolatile memory domain experts will share with us their perspective on future prospects for flash memory, phase change memory, MRAM and RRAM, including the challenges and opportunities each technology faces in its continuing evolution.

The final two presentations are from domain experts who will provide a prospective view on the potential for further growth in demand for nonvolatile memory in enterprise computing, and the emerging application of storage class memory.

Managing the Evolution of Flash: beyond Memory to Storage

- **Abstract:** As mobile systems become more intelligent as the hub of personal computing, the demand for higher performance and bigger capacity of Flash memory is all but insatiable. Managing Flash memory for reliability, performance and cost requires insight into not only the architecture of Flash technology but also how they are managed from software perspective at device and the host operationg system and file-system. The tutorial presents understanding these factors and the optimization of Flash storage device and host systems.

- **Tony Kim**

  - Director, Technical Marketing; Mobile/Flash Solution Team Lead, Samsung Semiconductor, Inc.

  - Tony Kim is Technical Marketing Director for Samsung Semiconductor and works as the Mobile/Flash Solution team lead. He joined Samsung Electronics in 1993 as an application engineer and has spent the last 17 years in product planning and applications engineering team for its memory division. He holds a B.S. degree in Electrical Engineering.

Forging a Future in Memory — New Technologies, New Markets, New Applications

- **Abstract:** The current non-volatile memory trends are allowing new applications such as solid-state drives (SSD) in enterprise systems to become a reality. However, scaling challenges associated with charge storage based memory (e.g., NAND) will undoubtedly add cost and/or performance hurdles that may ultimately limit SSD market penetration. Additionally, as customers begin to re-architect their systems to take full advantage of an SSD, they are left wanting for even more performance. Responsiveness in many of these initial use models is directly dependent on random latency, ranging from the time to access code or meta data, to the time it takes for critical information to be committed into a durable, reliable state. Phase change memory (PCM), while in its infancy, has the ability to scale well beyond charge based storage devices and provide non-volatile DRAM like latency closing the gap between storage and main memory.

- **Ed Doller:** Ed is currently the vice president and chief memory systems architect of Micron Technology. Prior to Micron's acquisition of Numonyx, Ed served as their Chief Technology Officer throughout its history. During his tenure at Intel, he held a variety of positions in the flash memory group before being named Chief Technology Officer in 2004. Prior to joining Intel, Ed held several key positions at International Business Machines (IBM) in East Fishkill, N.Y. all in advanced semiconductor memories. Ed has over 25 years of experience in semiconductor memories, holds multiple patents, is a co-author of the IEEE floating gate standard, and is a frequent keynote speaker at memory conferences. He received a BS in computer engineering from Purdue University in 1984.

Status and Prospect for MRAM Technology

- **Abstract** : Magnetoresistive Random Access Memory (MRAM) relies on magnetic polarization to store state of the memory. The MRAM unique attributes of non-volatility, high reliability, high performance, and unlimited endurance does not exist in any memory today and gives MRAM a differentiating position as the only viable nonvolatile working memory. MRAM availability has been growing rapidly and today 35ns products ranging from 256kb-16Mb are available from Everspin.   Recent advancement in MRAM technology, which will be discussed in this presentation, promises to enable MRAM to continue to grow in the market place and capture larger portion of the memory market.

- **Dr. Saied Tehrani** is chief operating officer and co-founder of Everspin Technologies. Prior to the formation of Everspin in June 2008, Saied was a director of Analog and Mixed Signal Technologies at Freescale Semiconductor, Inc. His R&D team was responsible for the development of power, analog, RF, sensor, and magneto-resistive random access memory (MRAM) technologies. Upon joining Freescale in 1985 (at that time known as Motorola Semiconductor Products Sector) he was involved in device and process research and development of heterojunction devices for high efficiency and low power applications. This included transferring the technology into production for wireless applications. In 1995, Saied was instrumental in beginning Freescale's MRAM program and has continued to lead the research and development progress of MRAM. Under his direction, Freescale became an industry leader in this technology. In late 2003, Freescale unveiled the industry's first MRAM samples to a select group of customers. In July 2006, Freescale announced the industry's first commercial MRAM device in volume production. Saied was co-recipient of the IEEE Dan Noble award for development of MRAM technology. He became a Motorola Fellow in 2000 and a Freescale Semiconductor Fellow in 2006. He has co-authored more than 80 articles in refereed journals, given more than 20 invited presentations at various international conferences and has 75 issued patents. Saied received his bachelor of engineering degree from the University of North Carolina, Charlotte in 1981. He received both his master's and doctorate in electrical engineering from the University of Florida, Gainesville in 1982 and 1985, respectively.

Memory Overview and RRAM Materials Development at SEMATECH

- **Abstract**: Metal oxide RRAM is a promising candidate for future non-volatile memory because it is capable of nanosecond switching speeds and effective densities approaching 1 F2. Several issues remain to be optimized such as lesser switching currents (power) and the associated switching mechanism. The key to some of these questions may be related to materials science - i.e. in reproducibly engineering defects in the metal oxide RRAM. This contribution will discuss progress on the development of manufacturable metal oxide materials for RRAM.

- **Dr. Paul Kirsch** received a B.S. (1995) in chemical engineering from the University of Wisconsin-Madison and Ph.D. (2001) in chemical engineering from the University of Texas at Austin. He was with IBM Systems and Technology Group from 2001 to 2007 working high performance gate stacks for bulk and silicon-on-insulator technologies. He joined the SEMATECH Front End Process team in 2007 and is currently the director of the front end process group. He has authored and co-authored more than 100 journal and conference papers in the various semiconductor research areas including high-k dielectrics, metal gates, high mobility channels, non-volatile memory and DRAM. He also holds 3 patents.

The Inevitable Rise of Nonvolatile Memory in Computing

- **Abstract**: SSDs roared into the storage market a few years ago with promises to replace all HDDs in all applications. While they haven't even partially reached that level of acceptance, these devices have achieved rapid adoption in the enterprise for certain tricky applications. The enterprise has served as a proving ground for the technology, and has brought about a far better understanding of how and where this new storage tier makes sense. This presentation explores flash in computing, and shows how and why flash storage will be embraced in systems of all levels without eradicating HDDs. The presenter will detail many of the new challenges flash presents to the system, and explains why software will need to change to accept flash and other new technologies that will eventually replace flash.

- **Jim Handy**, a well-known and respected memory market industry analyst, is known for his deep insight and firm understanding of the memory chip industry and its drivers. A frequent speaker and highly-published author, Handy combines a unique blend of technical strength (BSEE Ga Tech) with business savvy (MBA Univ. of Phoenix). Handy is founder/president of Objective Analysis, the author of "The Cache Memory Book", and a patentholder in the field of memory ICs.

Storage Class Memory: Technology, Systems and Applications

- **Abstract:** Storage Class Memory (SCM) is the term used to describe a new class of solid-state, nonvolatile memory technologies. There are several (≥ 10) such technologies currently under active research and development that are vying to become the SCM of choice. As a group, their performance is nearer memory than storage while their cost is nearer storage than memory. In the systems designer's eye, these performance and cost characteristics blur the historic distinction between memory and storage. Exploiting SCM will require significant changes in the design of memory and storage systems. These changes at the system level will force or enable changes at the application level as well as opening up new application opportunities. In this talk we will discuss several of today's leading SCM technologies, discuss their potential impact on the design of memory and storage systems, consider the changes that might be needed to existing applications and explore some of the potential opportunities for future applications.

- **Dr. Richard Freitas** is a Research Staff Member at IBM's Almaden Research Center, 650 Harry Rd., San Jose, CA 95120. Dr. Freitas received his PhD in EECS from the University of California at Berkeley in 1976. He has held various management and research positions in architecture and design for storage systems, servers, workstations and speech recognition hardware at the IBM Almaden Research Center and the IBM T J Watson Research Center. His current interests are in exploring the use of emerging nonvolatile solid state memory technology in computer systems.