Xilinx Virtex-6 and Spartan-6 FPGA Families

Peter Alfke, Xilinx, Inc

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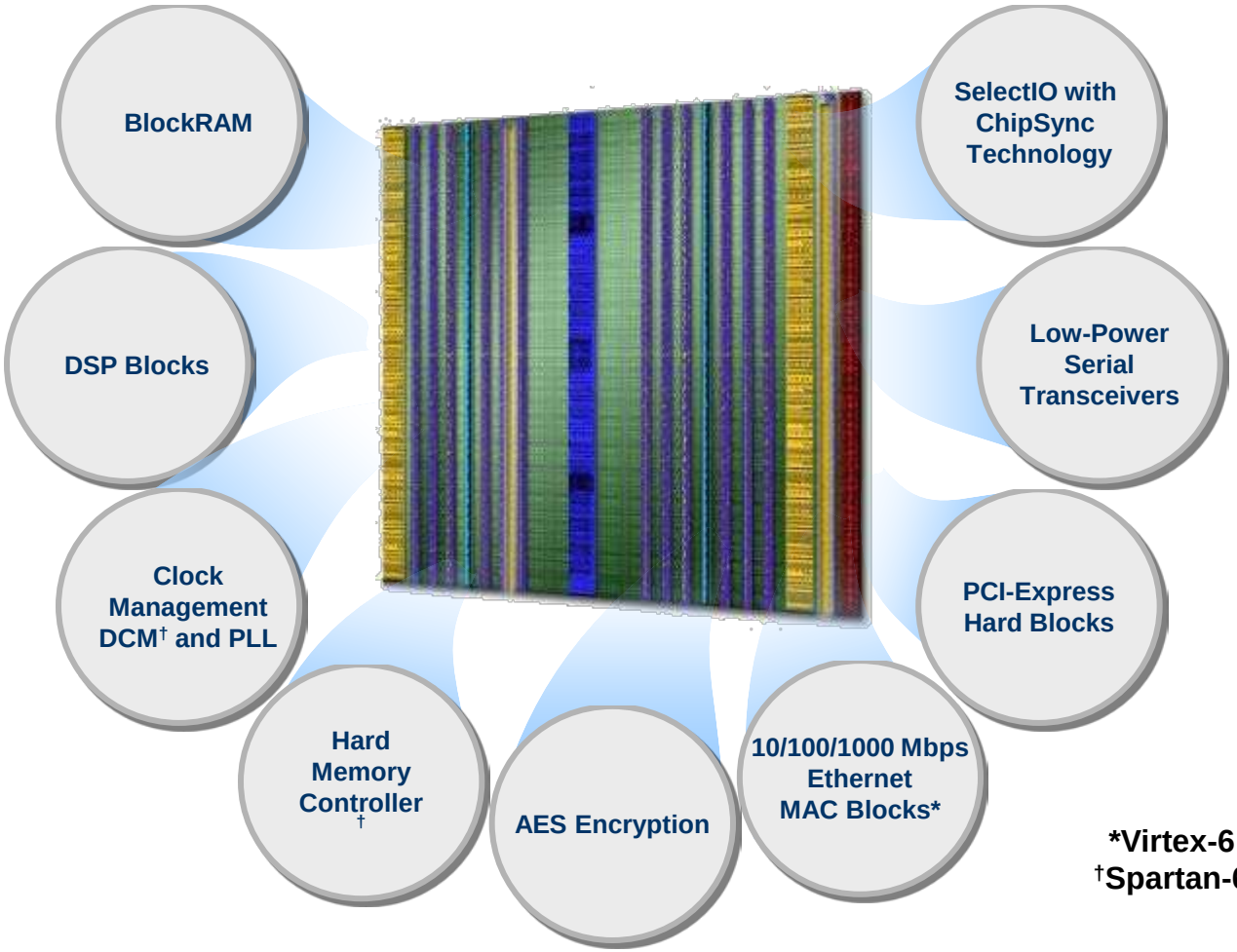
Virtex-6 and Spartan-6 FPGA Families

- **Moore's Law**
  - Doubles the max capacity, compared to the previous generation
  - Reduces cost per function
- **Architecture and circuit innovations**
  - Increase speed and lower power consumption

- **Wide range of capacity, applications, cost**
  - Virtex-6 and Spartan-6 FPGAs cover a 250 : 1 capacity range
    - At the high end: Virtex-6 covers a 10 : 1 ratio
    - At the low end: Spartan-6 covers a 40 : 1 ratio
      - The name always indicates the logic capacity: XC6V760 to XC6S4

- **Virtex-6 and Spartan-6 share architecture, technology, software**
    - Different emphasis on cost, performance, power, size, packaging
    - Used to be cousins, now they are siblings
- **Both families are sampling since mid-2009**

Virtex-6 and Spartan-6 Hard-IP Blocks

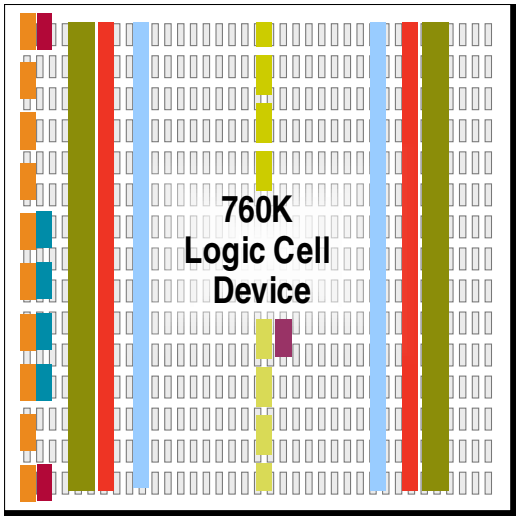


*Virtex-6 Only
†Spartan-6 Only

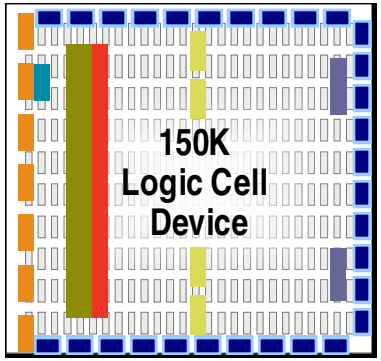
Hard IP blocks for widely-used functions: faster, more efficient, lower power
Careful choice: every user must pay for these functions, whether used or not

Virtex-6 and Spartan-6 Architecture Alignment

Virtex-6 FPGAs



Spartan-6 FPGAs



Common Resources

- LUT-6 CLB
- Block RAM
- DSP Slices
- High-performance Clocking
- Parallel I/O
- Gigabit Transceivers*
- PCIe® Interface

- FIFO Logic
- Tri-mode EMAC
- System Monitor

- Hardened Memory Controllers
- 3.3 Volt compatible I/O

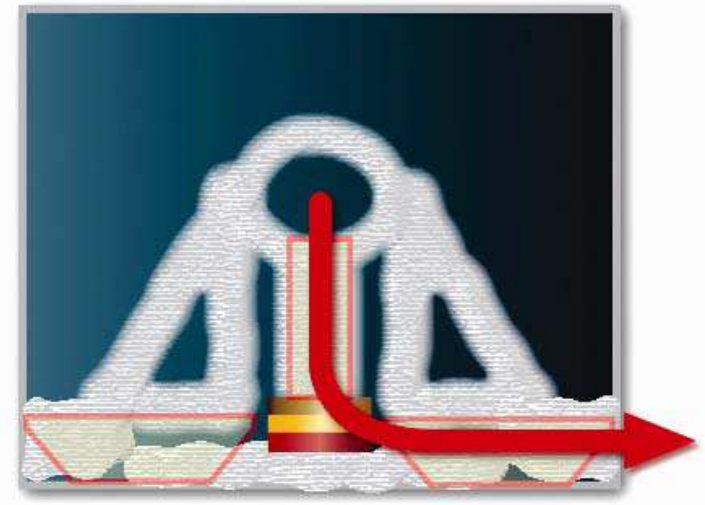
*Optimized for target application in each family, Gigabit transceivers in large Spartan-6 devices

Enables design portability, allows design re-use

What is Virtex-6 ?

- **Next Generation 40nm Virtex Product Family**
  - Increase in size, density and cost reduction compared to Virtex-5
  - Increased speed and reduced power mainly through architecture and cicuitry
  - Evolutionary Feature Enhancements from Virtex-5
- **Three Platforms**
  - **LXT:** popular mix of logic, memory, DSP and serial connectivity
  - **SXT:** additional DSPand Memory, same serial connectivity
  - **HXT:** adds 11.2 Gbps transceivers for highest total bandwidth
- Staged Rollout
  - **LXT & SXT:** “ES” 3Q09, General avalability 4Q09, Production early 2010
  - **HXT:** Production 2010

Power Focus: Process and Circuit Innovation



- **Low static power (controlled leakage)**
  - 3rd generations of Triple Oxide innovation
    - Fast transistors wherever needed, low leakage everywhere else
  - Speed without additional leakage:
    - Silicon Germanium (SiGe) implant layer
    - Strained silicon
- **Low dynamic power**
  - Process shrink and low-K dielectric material
  - Vccint = 1.0 V with 0.9 V option
    - 20% lower power @ 10% lower speed

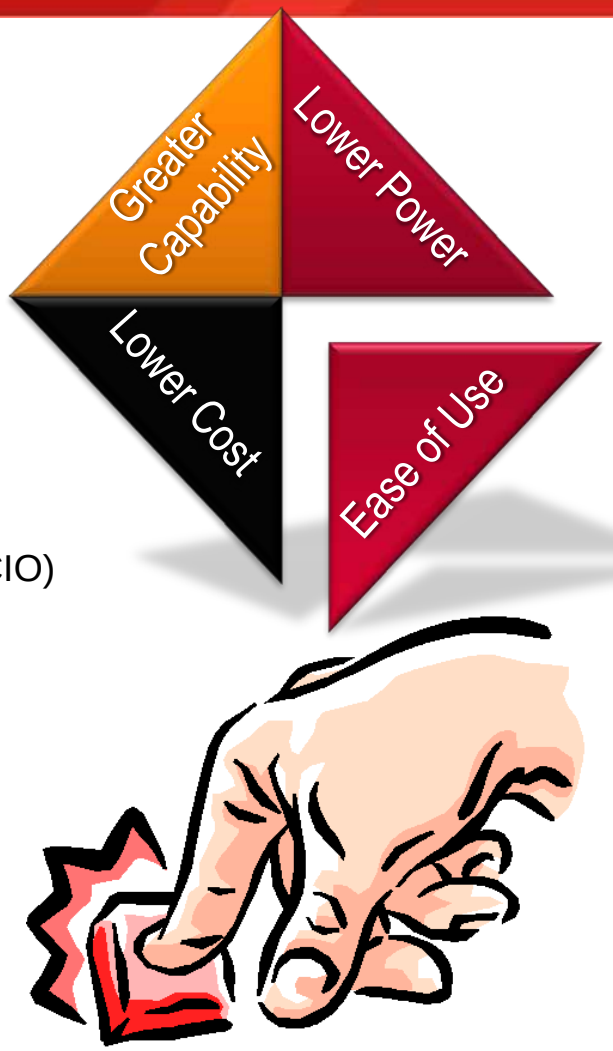
Careful power reduction while maintaining performance

Performance Improvements, Virtex-6 over Virtex-5

- **Logic: 15% faster**
  - Advanced process, improved routing, faster pipelining
- **Serial Transceivers: 86% higher total bandwidth**
  - Up to 72 transceivers delivering 580 Gbps in Virtex-6 HXT
  - Compared to 48 transceivers delivering 312 Gbps in Virtex-5 TXT
- **General-purpose I/O: 33% higher bandwidth**
  - Enables advanced memory interfaces (DDR3)
- **Global clocking: 10% faster**
  - Lower skew, improved jitter, faster clock trees
- **DSP bandwidth more than doubled**
  - Over 2,000 enhanced DSP slices

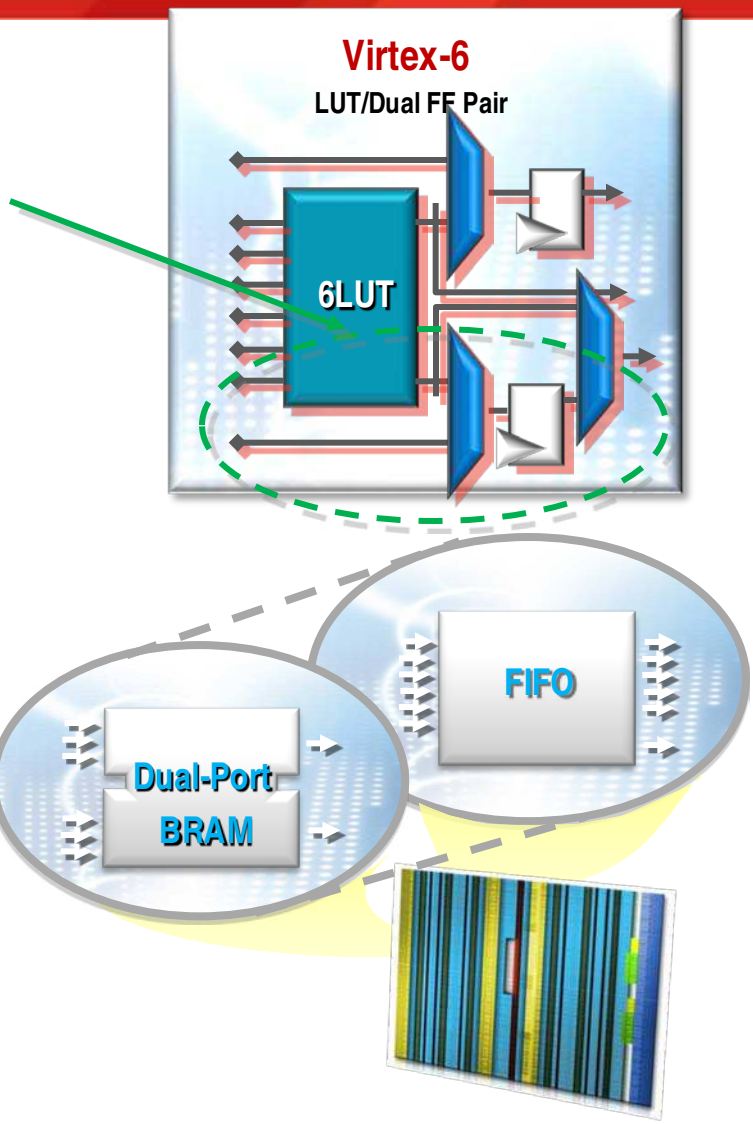
Ease of Use and Lower Cost

- **Designed to be backward compatible with Virtex-5**
  - Same GTX, SelectIO, BRAM, MMCM, & LUT6 primitives
  - Superset of CLB and DSP fratures
- **Simple IO planning and board layout**
  - All IOs support all standards at all speeds, period.
  - Homogenous IOs simplify layout
- **Simple power supply planning**
  - Requires only three power supplies. (VCCINT, VCCAUX & VCCIO)
  - Embedded decoupling capacitors
- **Shorter Time to Market**
  - Easy Migration from previous generations
  - Large set of available and portable IPs



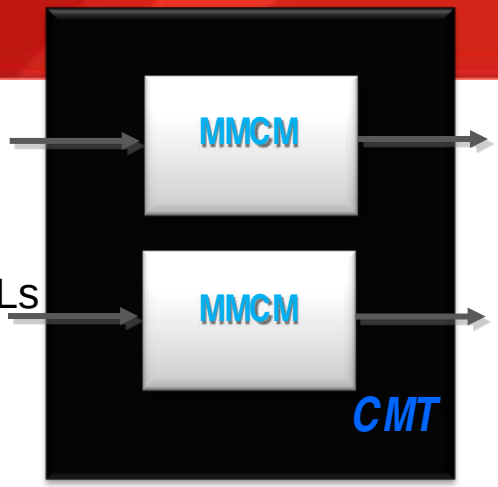
Virtex-6 Logic and BlockRAMs

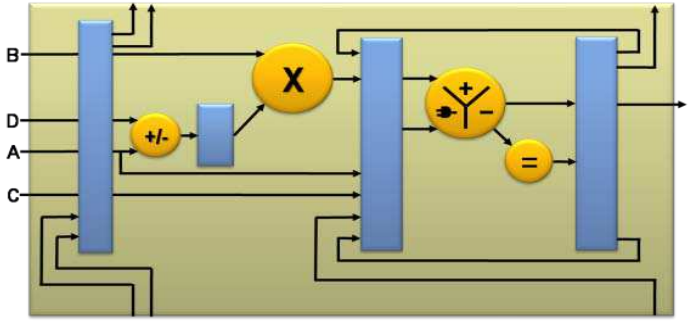
- ***CLB differences from Virtex-5***
  - Double the number of flip-flops
  - Much more efficient pipelining
- ***Block RAMs same as in Virtex-5***
  - Higher memory / logic ratio in LXT
  - Up to 38 Megabits of Block RAM
  - Still the same features:
    - 36k Block splittable in 2x 18k Blocks
    - Single-port, simple dual-port and true dual-port
    - Read before write, as well as write before read
    - FIFO option
- ***Don't tamper with success***



Clocking and DSP

- ***Large chips + high speed pose challenges***
- ***Multiple clocks derived on-chip***
  - Mixed Mode Clock Manager (MMCM) replaces DCMs and PLLs
    - PLL-based technology with DCM-like enhancements
- ***Very large chips need large Global Clock trees***
  - High fan-out, low delay, low skew, low jitter
    - Fan-out is driven from the center
    - In spite of this, largest chip lacks fastest speed grade
- ***Dedicated DSP48 Multiplier / Accumulator***
  - Up to 2000 DSP48 circuits support parallelism
  - Superset of the Virtex-5 DSP block
  - Pre-adder saves logic and power
    - improves performance
      especially for symmetrical FIR filters
  - ALU-like second stage reduces power

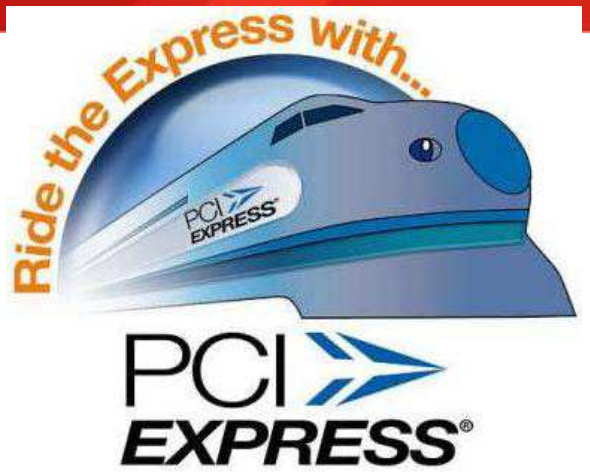




Select IO and Gigabit Transceivers

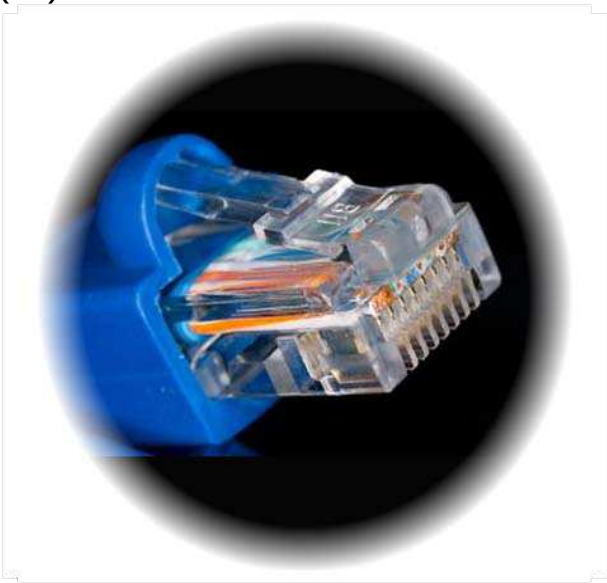
- ***Select IO has higher performance***
  - LVDS @ 1.4Gbps, DDR3 @ 1066+ Mbps
  - Support for new memory types
    - DDR3-DIMM, RLDRAM-II, QDR-II+
- ***GTX transceivers in every Virtex-6 device***
  - 150 Mbps to 6.5 Gbps, wide range @ low power
  - Generates less jitter, tolerates more jitter
    - Critical for CEI6, PCIe Gen 2, OC-48, OTU-1
  - Up to 72 Transceivers for highest bandwidth
  - Growing demand for popular standards above 3.75G
    - PCIe Gen2, SRIO2, CPRI/OBSAI 6G, CEI-6G, Interlaken, …
- **GTH transceivers in the HXT family**
  - highest speed: 11.2 Gbps,
  - Narrow-range LC-based VCO for lowest jitter

Dedicated Blocks for High-Bandwidth Standards

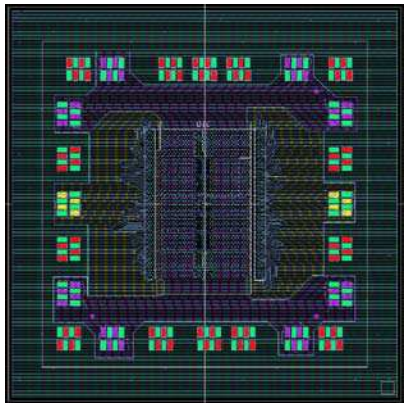


- ***PCI-Express***
  - Now supports 5 Gbps Gen 2 (Spec 2.0): x1, x2, x4
    - Full Root Complex is supported with a soft IP wrapper
    - Allows simple FPGA to FPGA communication
  - Small wrapper for Endpoint implementation
    - Easier timing closure:
      <100 LUT for Virtex-6 FPGA vs. 3,000LUTs for Virtx-5 FPGA (x8)

- ***EMAC***
  - *Ethernet at* 10/100/1000/2500 MHz
  - Stable standard; well understood use model
  - Very Similar to the Virtex-5 TEMAC block
    - Added 2.5G over-clocked mode (2500)
    - Demand for 2.5 G operation is growing
    - Interoperable with Broadcom ASSPs: 2.5 G switches

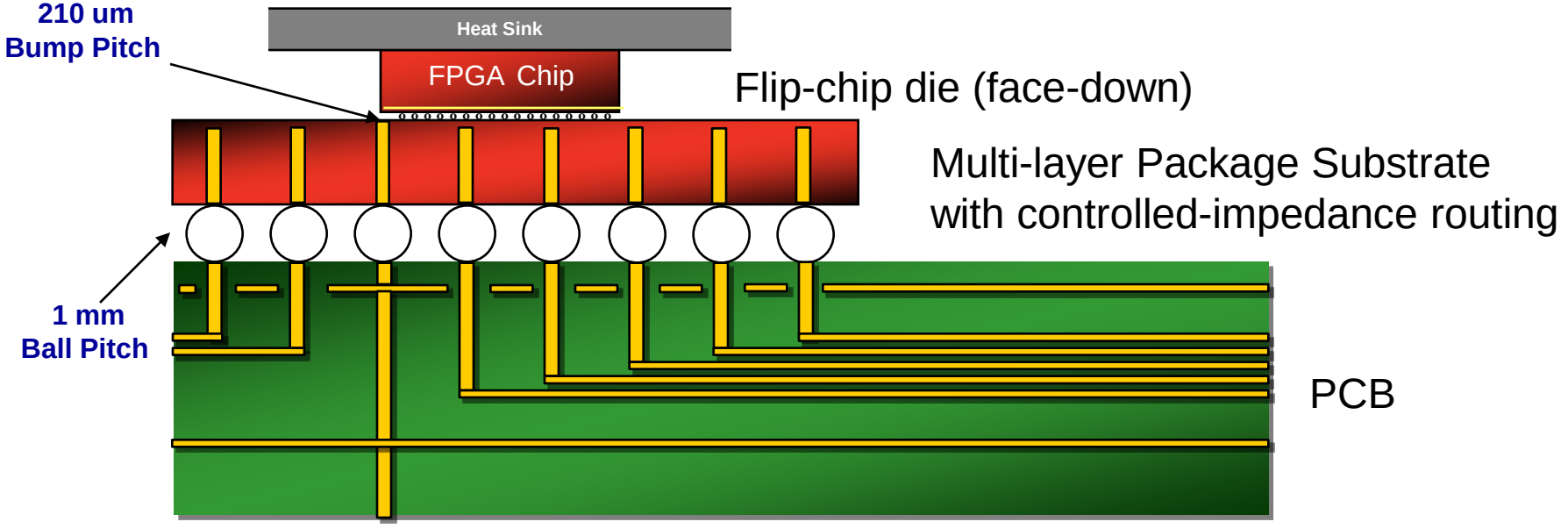


Attention to Signal Integrity Issues



- **Virtex-6 uses Flip-Chip technology**
- **I/Os spread over the chip,**
  - not limited to the periphery
  - No wire-bonded I/Os, less inductance
  - Up to 8000 micro-bumps attach to the package
- **Generous decoupling capacitors inside the package**
  - More effective, better quality, lower cost for the user
- **10-layer controlled-impedance package substrate**
  - 1-mm ball pitch to ease board layout
  - “Sparse Chevron” interspersed Vcc and GRD
  - Gigabit transceivers isolated on the left edge
  - Improved thermal performance,
  - metal top attached to the chip,
  - low thermal resistance to the board

Virtex-6 Device Package Cross-Section



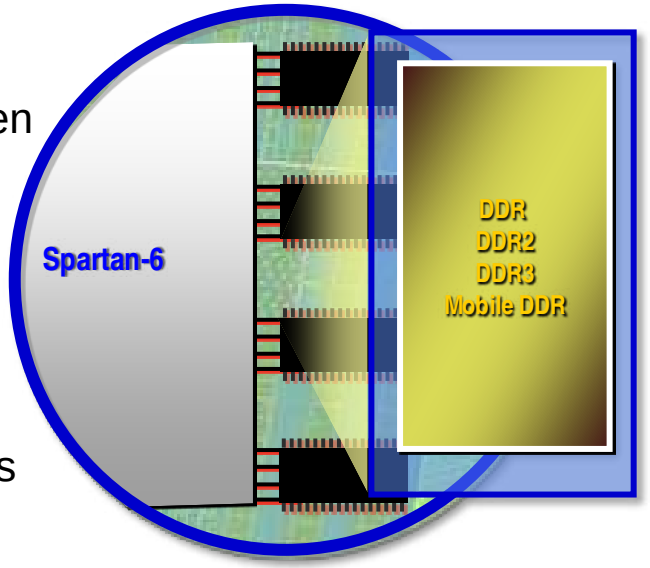
High-performance flip-chip technology **Most designs are I/O-bound**

High-End Features in Spartan-6 FPGAs

- **Spartan-6 uses a 45-nm process, optimized for low power**
  - Low-cost FPGAs usually sacrifice performance
  - But there are exceptions:
- **DDR3 Controller**
  - DDR3 is lowest cost external memory, but needs a demanding interface
  - DDR3 requires clock rate of >300 MHz (PLL on the memory device)
  - Spartan-6 devices incorporate 2 or 4 dedicated DDR3 controllers.
- **Multi-Gigabit Transceivers @ up to 3.125 Gbps**
  - For bit-serial connectivity between devices, boards and boxes
  - eliminates clock / data skew, reduces board area or cabling
  - differential signals, 4 wires total, support high-bandwidth traffic,

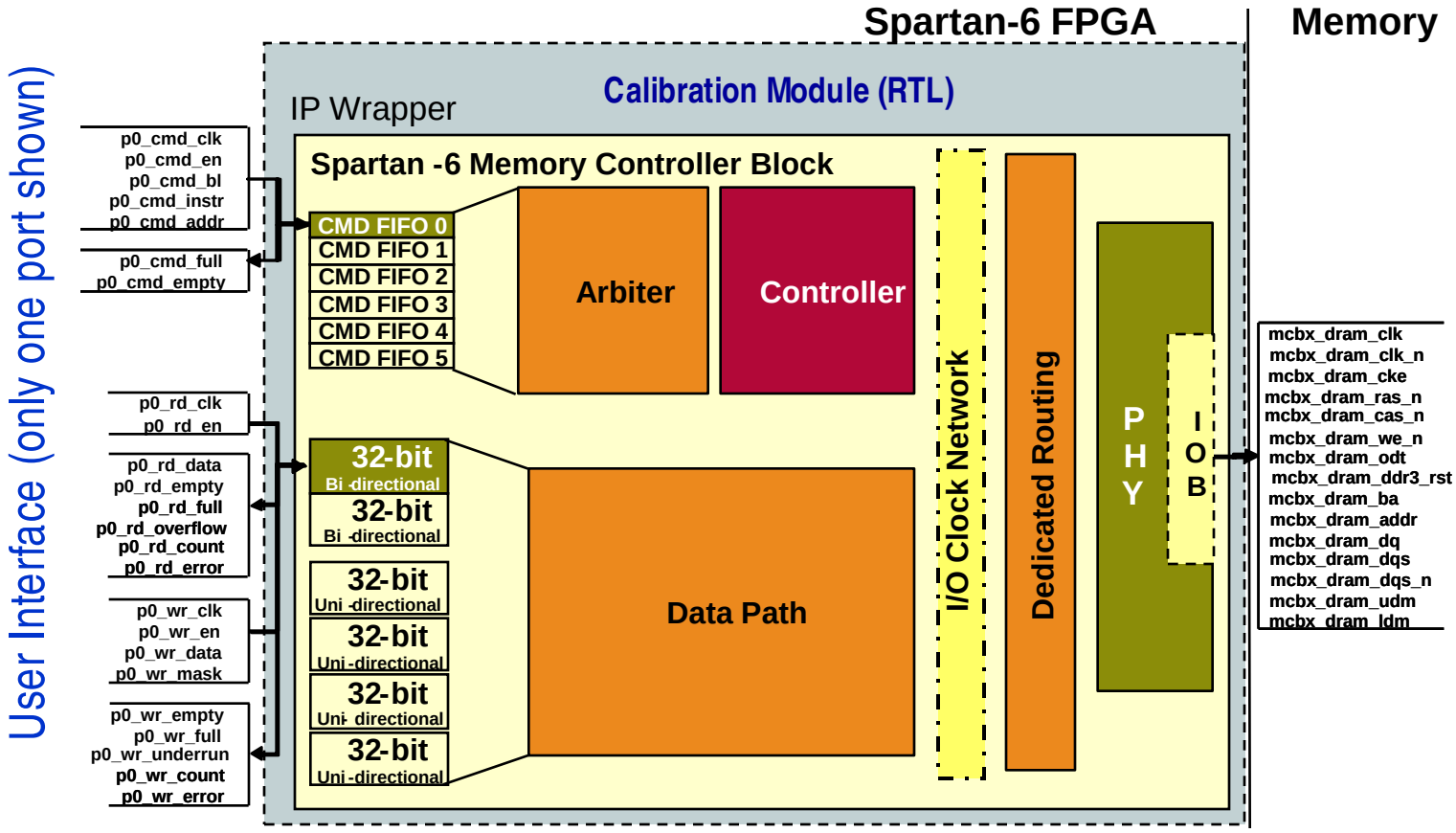
Integrated Memory Controller in Spartan-6 FPGAs

- **Provides interfaces from low cost FPGAs to industry's most popular DRAM memories**
  - DDR, DDR2, DDR3, mobile DDR
- **Up to 4 controllers in each Spartan-6 device**
  - Each of the these hard-coded controllers saves between 500 and 2000 LUTs versus soft solution
  - Very important for cost-sensitive designs
- **12.8 Gbps bandwidth per controller**
  - 16-bit wide, 400MHz / 800Mbps operation
  - Each controller interfaces to one DDR3 chip, no DIMMs
- **Fast and easy implementation**
  - Wizard guided design flow
  - Virtex-6 solution uses soft controller for flexibility



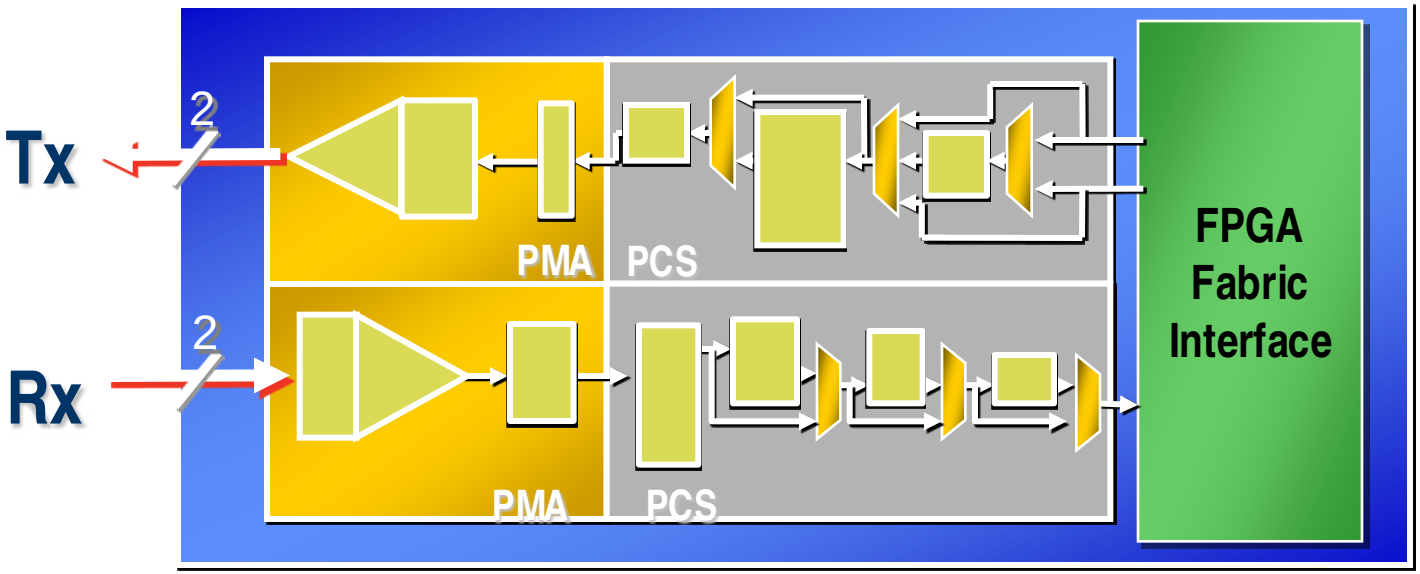
•Low-cost FPGA meets low-cost, but fast memory

Memory Controller Block Diagram



- **Simple user interface abstracts away complexity of memory transactions**
- **MIG / EDK wrapper delivers complete interface solution**
  - Internal block assembly and signal connectivity is made transparent to the user

Multi-Gigabit Transceivers in Spartan-6 FPGAs



- **Dedicated parallel-to-serial transmitter and serial-to-parallel receiver**
  - Many programmable features, compatible with a wide range of standards
  - Unidirectional, differential bit-serial data I/O
  - Integrated PLL-based Clock and Data Recovery (CDR)
- **Parallel interface to the FPGA internal fabric**
  - 8 to 40 bit wide, to accommodate internal speed limits and optional fabric encoding
- **Serial interface to the Printed Circuit Board (differential signaling)**
  - Differential Current Mode Logic (CML)
  - Two traces for the transmitter, and two traces for the receiver, removes common-mode noise
  - Programmable signal swing and Tx & Rx equalization

Availability

Three Levels of Availability

- **Initial ES Silicon:**
  for Xilinx-internal use, testing, evaluation, and sometimes for special customers

- **General ES Silicon**:
  available for general ordering through distribution with a specified lead-time.
  Usually has an errata sheet.
  - **Third-quarter 2009 availability :** Spartan-6: LX16, LX45, Virtex-6: LX240T

- **Production:**
  100% tested and verified, available for general ordering through distribution.
  Distributor quotes price and lead time.
  - All devices, temperature and speed grades

Virtex-6 and Spartan-6 FPGA Families Summary

- **Both families take advantage of 40/45 nm technology and innovative architecture and circuit design**
  - Improved performance, smaller size, lower cost, lower power
  - Virtex-6 evolved from the successful Virtex-5 family
  - Spartan-6 more closely related to Virtex-5 and Virtex-6 than to Spartan 3A
- **Similar in architecture, but each is optimized**
  - Virtex-6 for performance, features, and capacity
  - Spartan-6 for low cost and low power
- **Complete documentation on the web:**
  - Data Sheets and User Guides:
  - Evaluation Boards
  - Software