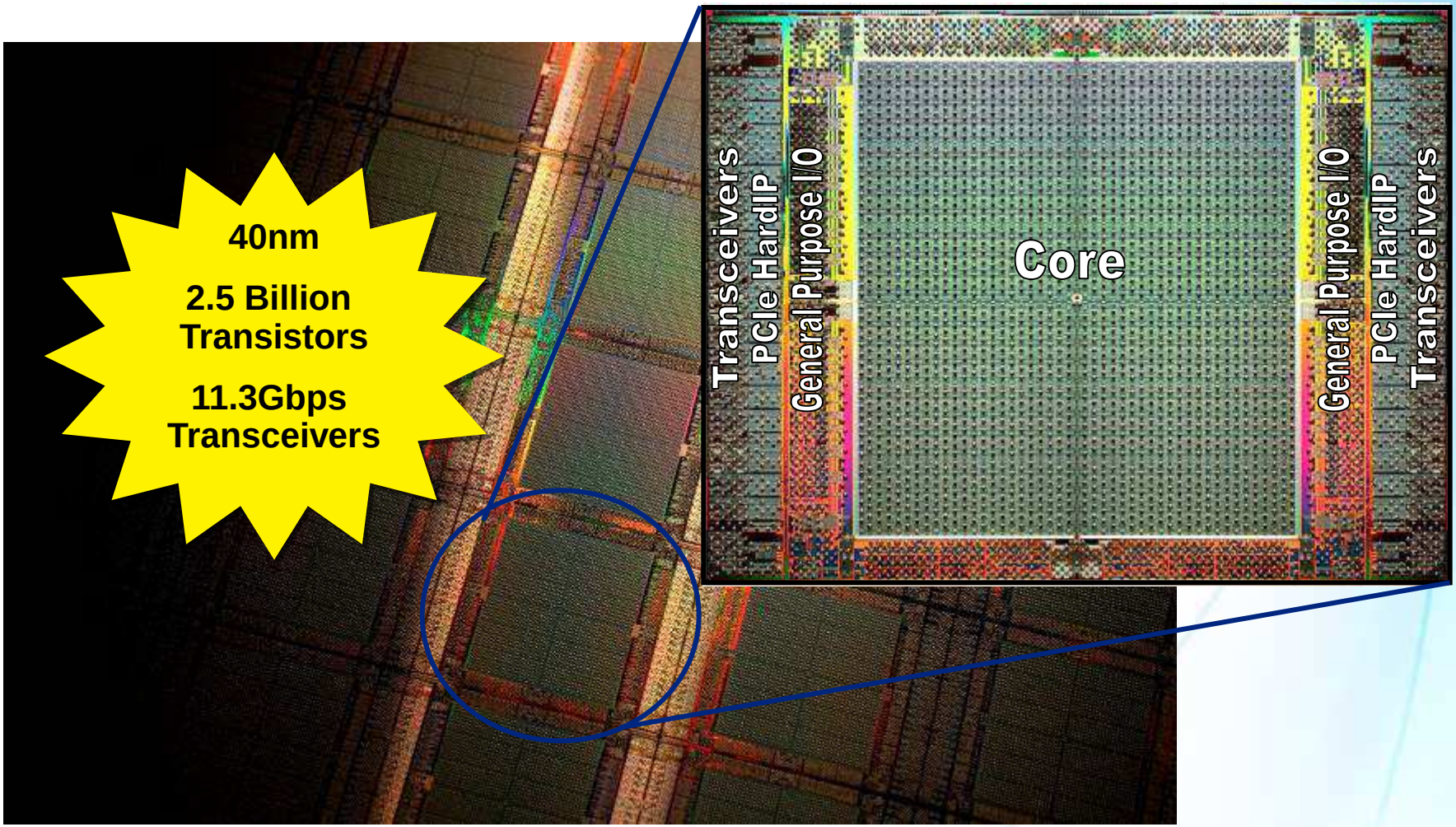
# Newest Additions to Altera's Integrated Transceiver Portfolio

**Stratix IV GT FPGA**
**Integrated 11.3Gbps Transceivers**

**Arria II GX FPGA**
**Integrated 3.75Gbps Transceivers**

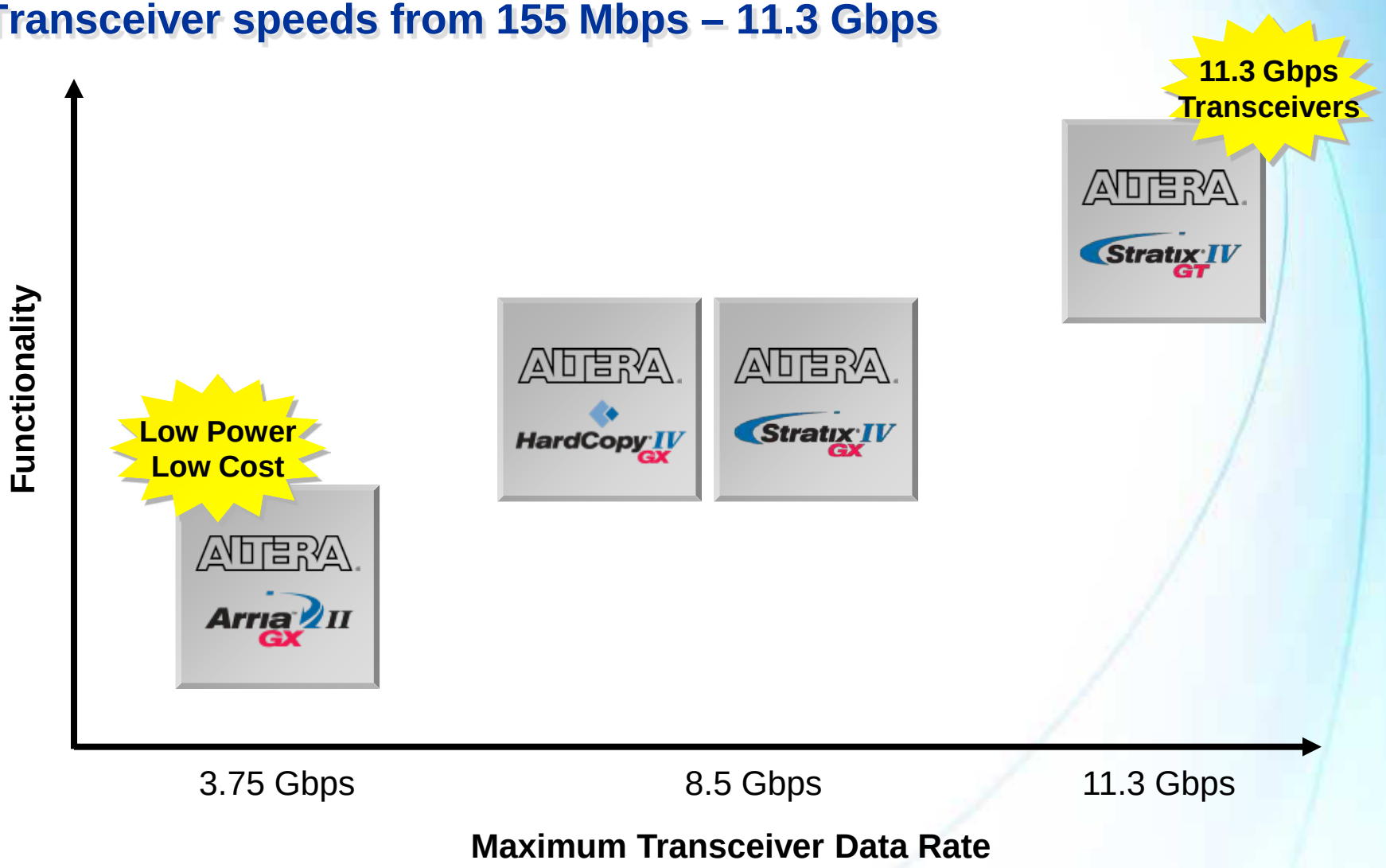
*Dan Mansur, Altera Corporation*

# Stratix IV GT FPGA – Shipping 1Q09



# Broadest Integrated Transceiver Portfolio

## Transceiver speeds from 155 Mbps – 11.3 Gbps



# Stratix IV GT FPGA

- First 40nm FPGA available with 11.3 Gbps transceivers
  - Shipping today, both 230K and 530K equivalent LE (logic elements or 4 input look-up-table equivalent)
  - Up to 48 transceivers, 24 running at 11.3 Gbps
  - Superior signal integrity, meets XLAUI/CAUI, CEI-11G specifications
- Optimized to meet 40G/100G system requirements
  - Highest density with lowest power
  - Core performance to match 100G requirements
  - Interoperability testing with optical module vendors
  - Integrated transceivers, no external 10G PHY required
- IP & board solutions
  - Reliable 3rd party IP solutions available now
  - Signal Integrity board available for evaluation of transceivers
  - 100G demonstration platform available July, 2009

# Stratix IV GT FPGA Device Family

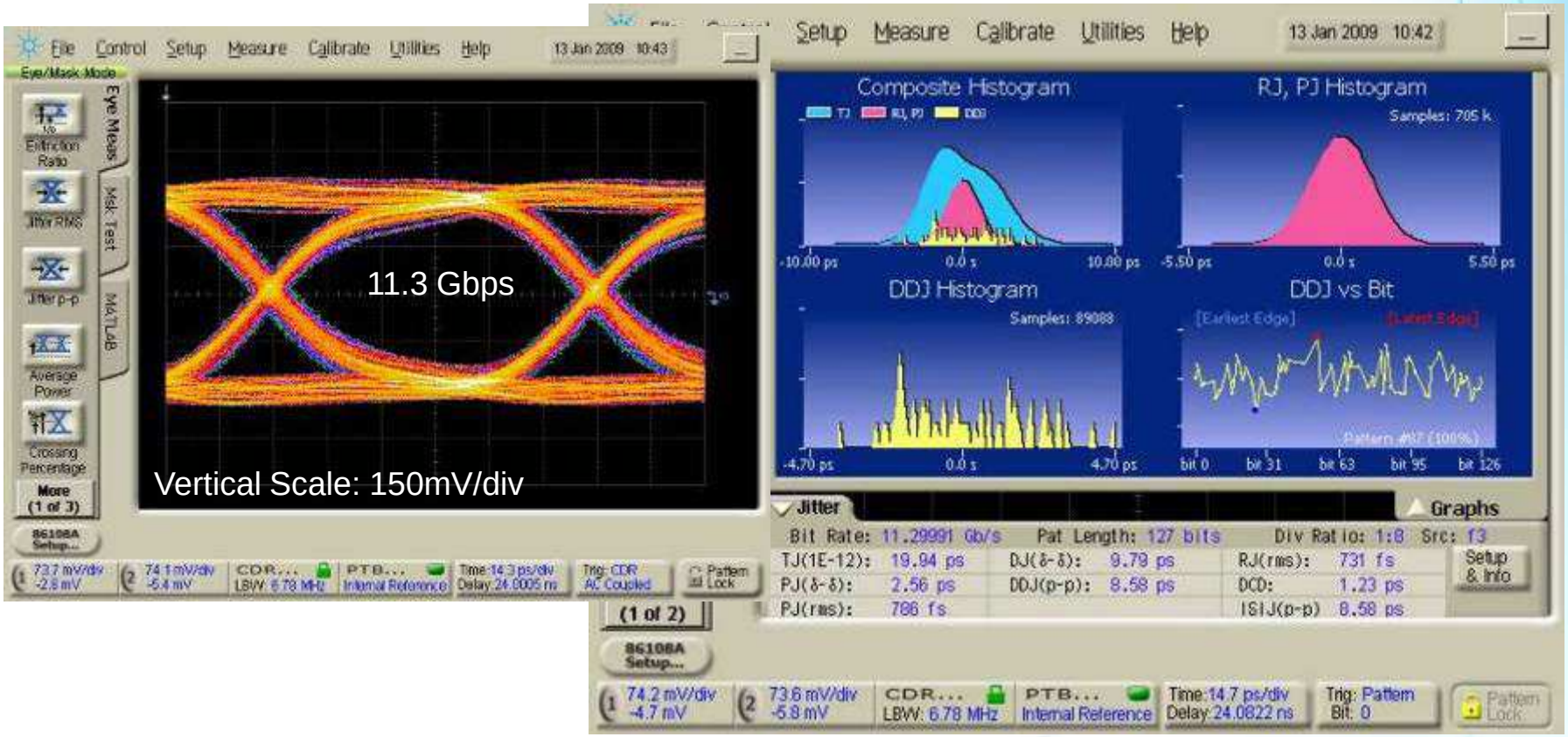
| Device | LEs | Transceivers 11.3, 8.5, 6.5 Gbps (Total) | LVDS | I/Os | Memory (Mbits) | Package[1] |
|---|---|---|---|---|---|---|
| **40G Devices** | | | | | | |
| EP4S40G2 | 230K | 12, 12, 12 (36) | 44 | 636 | 13.9 | F1517 |
| EP4S40G5 | 530K | 12, 12, 12 (36) | 44 | 636 | 20.3 | H1517 |
| **100G Devices** | | | | | | |
| EP4S100G2 | 230K | 24, 0, 12 (36) | 44 | 636 | 13.9 | F1517 |
| EP4S100G5 | 530K | 24, 0, 12 (36) | 44 | 636 | 20.3 | H1517 |
| EP4S100G3 | 290K | 24, 8, 16 (48) | 44 | 754 | 13.3 | F1932 |
| EP4S100G4 | 360K | 24, 8, 16 (48) | 44 | 754 | 17.7 | F1932 |
| EP4S100G5 | 530K | 24, 8, 16 (48) | 44 | 754 | 20.3 | F1932 |

**Note 1: Flip chip ball-grid array (BGA) with 1.0-mm pitch**
**H = Hybrid package**

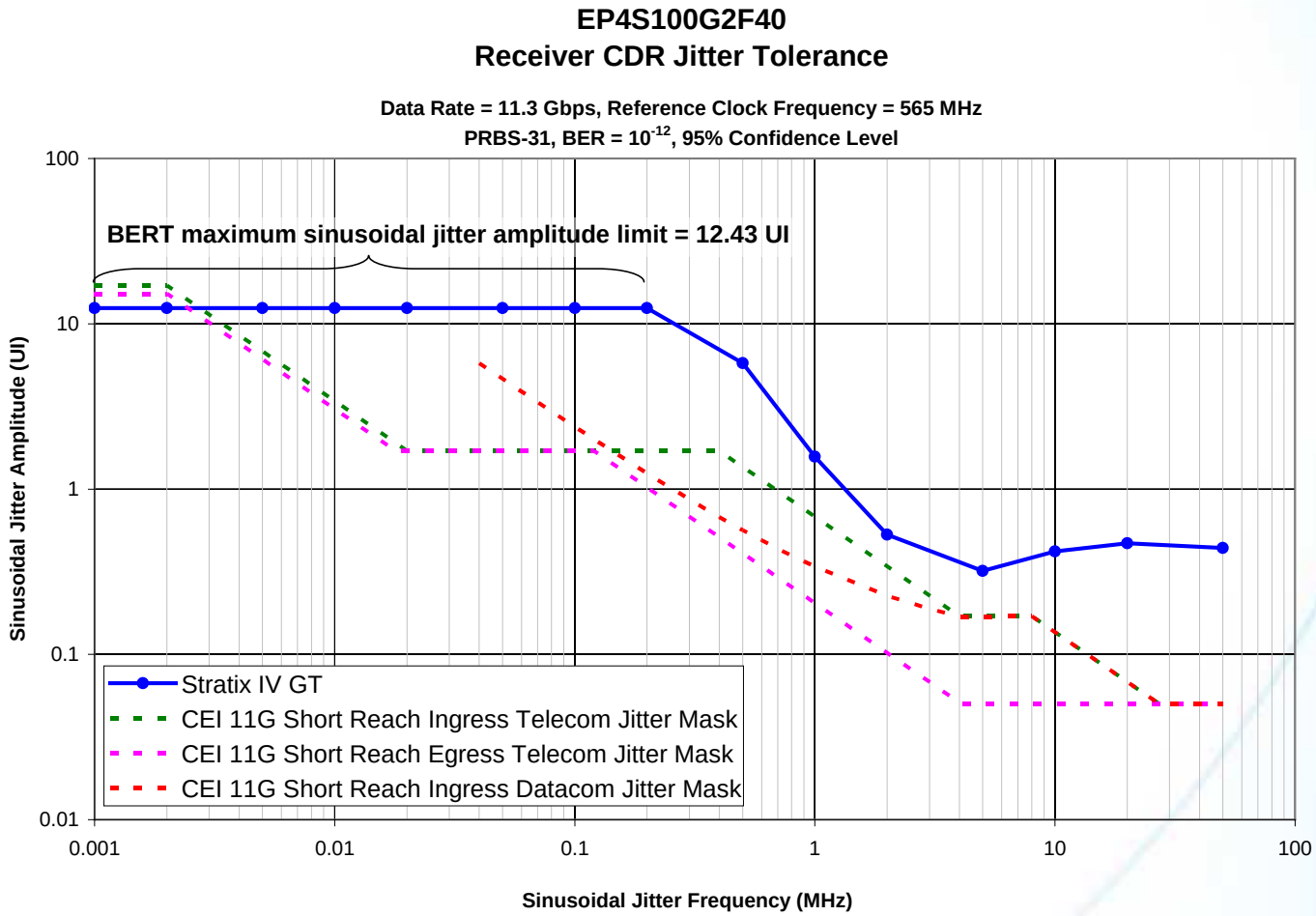
**Vertical migration**

# Stratix IV GT FPGA TX Eye Diagram, 11.3 Gbps

- Superior jitter performance
  - Wide open TX eye, 8 channels switching at 11.3 Gbps

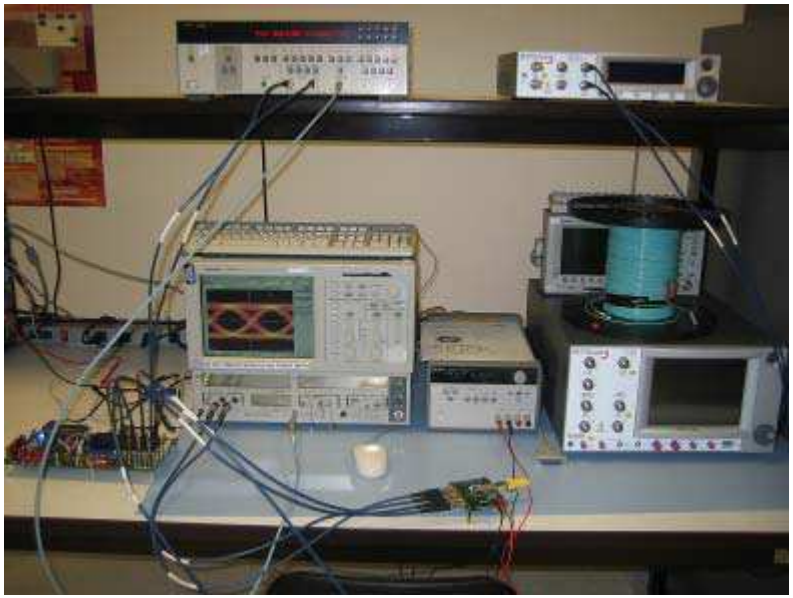


# Stratix IV GT FPGA Jitter Tolerance, 11.3 Gbps

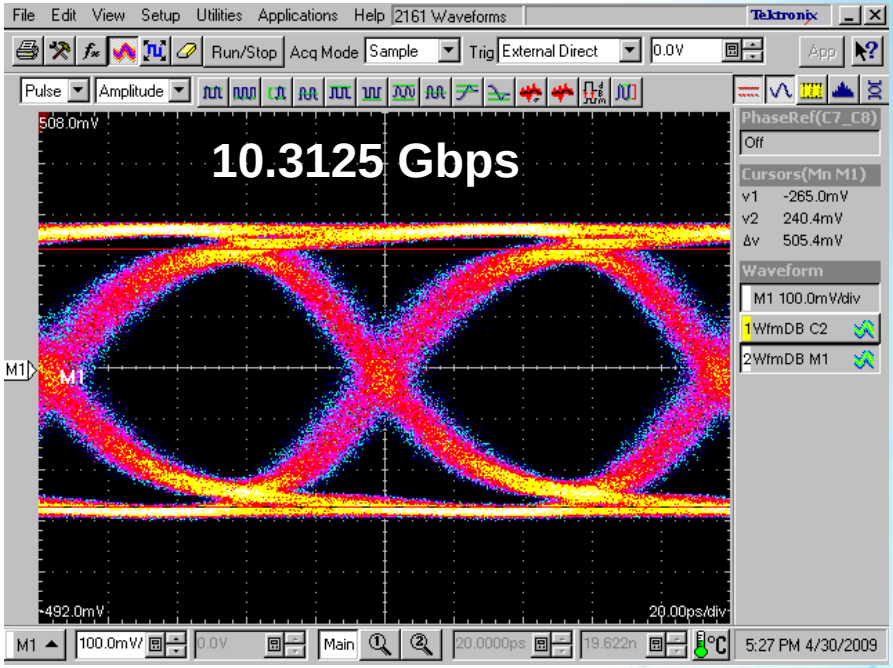



- Exceeding CEI-11G SR jitter tolerance with margin

# Showing SFP+ Module Interoperability



- EP4S100G2, ES1 device
- Room temperature
- 6 transceiver channels active
- 1 transceiver channel observed
- PRBS 31 data pattern
- Vod = 600mV
- Pre-emphasis setting = 5




- Far end eye-diagram, Avago SFP+ SR optical module, 10.3125 Gbps
- Eye wide open after 100m multi-mode fiber (MMF) optical loopback

# Stratix IV GT FPGA 10/40/100G Protocols

| Protocol | Interface | Number of lanes per side | Data rates |
|---|---|---|---|
| **10G independent channels** | | | |
| 10Gb Ethernet, 10Gb Fibre Channel | XFI, SFI *(1)* | 1-12 | 10.3, 10.7 Gbps |
| Sonet/SDH OC-192/STM-64, G.709 OUT-2 | XFI, SFI *(1)* | 1-12 | 9.9–11.3 Gbps |
| 10G Basic (Proprietary) | OIF/CEI-11G | 1-12 | 9.9–11.3 Gbps |
| **40G bonded channels** | | | |
| Interlaken | OIF/CEI-6G | 8-12 | 4.976–6.375 Gbps |
| SPAUI, DDR-XAUI | OIF/CEI-6G | 2-6 | 6.4 Gbps |
| 40G IEEE 802.3ba | XLAUI | 4 | 10.3125 Gbps |
| SFI-4.2 | SXI-5 | 5 | 2.488–3.125 Gbps |
| SFI-5.1 | SXI-5 | 17 | 2.488–3.125 Gbps |
| SFI-5.2 | OIF/CEI-11G | 5 | 9.9–11.3 Gbps |
| SFI-S | OIF/CEI-11G | 5 | 9.9–11.3 Gbps |
| **100G bonded channels** | | | |
| Interlaken | OIF/CEI-6G | 20-24 | 4.976–6.375 Gbps |
| SPAUI, DDR-XAUI | OIF/CEI-6G | 4-6 | 6.4 Gbps |
| 100G IEEE 802.3ba | CAUI | 10 | 10.3125 Gbps |
| SFI-S | OIF/CEI-11G | 11 | 9.9–11.3 Gbps |

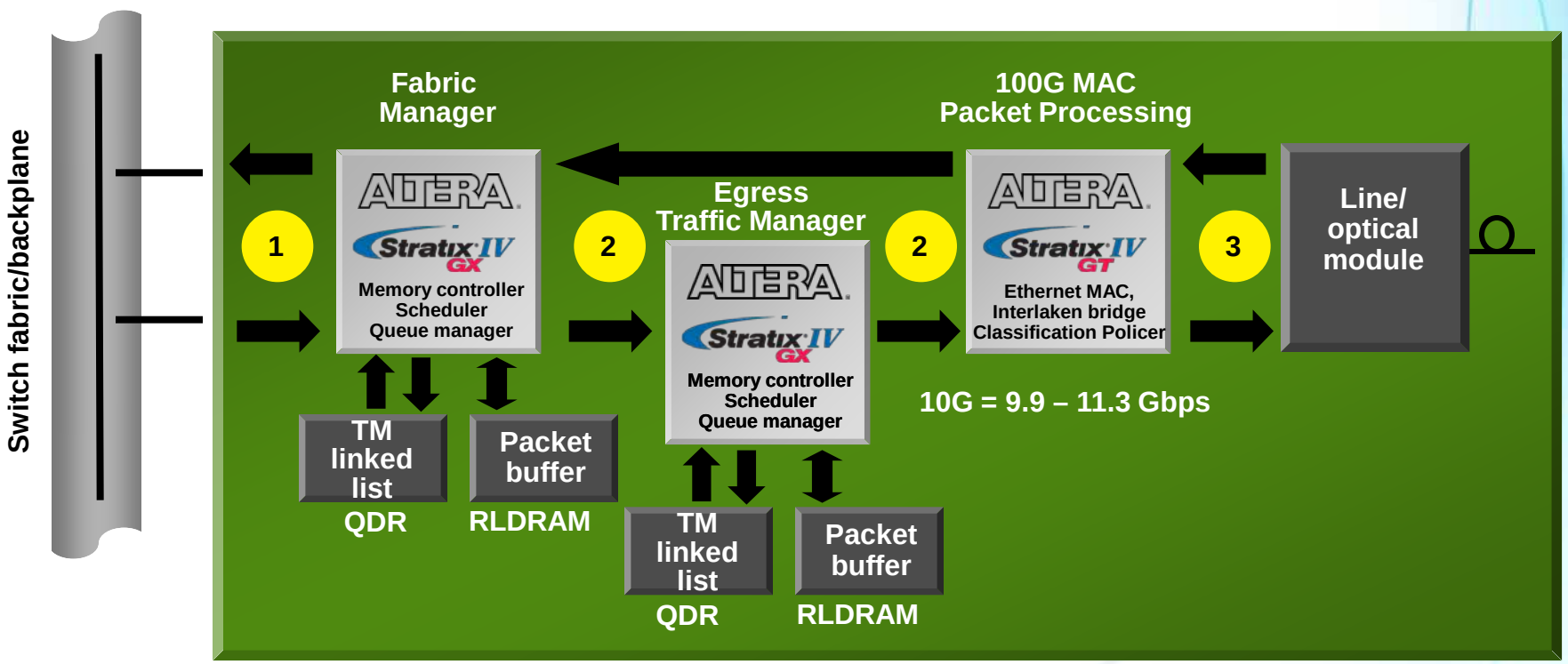
**Note 1. Support for SFI-S may require external signal conditioning (EDC) chip**

# Example: 100G Line Card

**1** 100G chip-to-backplane Example
SPAUI and DDR-XAUI

**2** 100G chip-to-chip Example
Interlaken 20-24 @ 6.375 Gbps

**3** 100G chip-to-module Example
CAUI (10 lanes @ 10G)

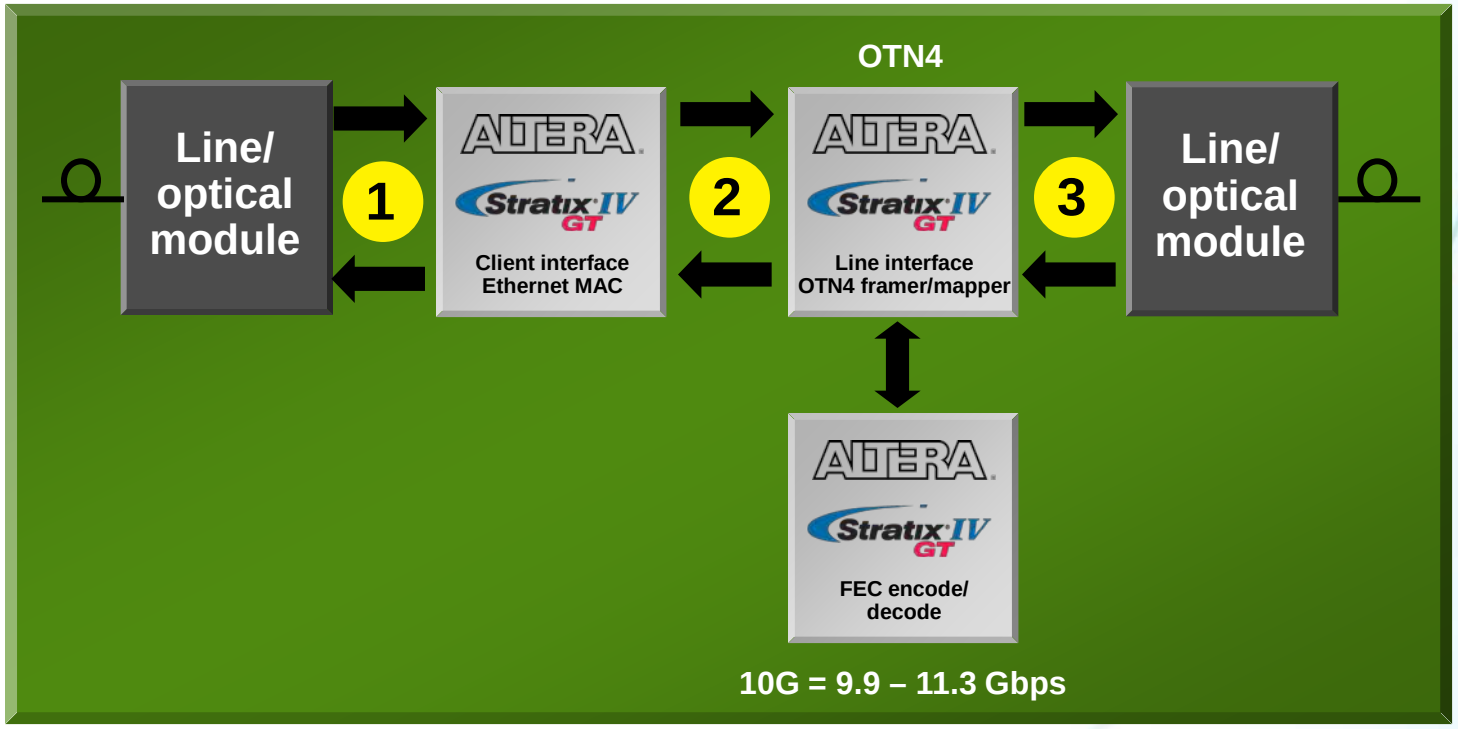


# Example: 100G OTN4

1. **100G Module Interface Example**
   **SFI-S/MLD (10 @ 11.3 Gbps)**

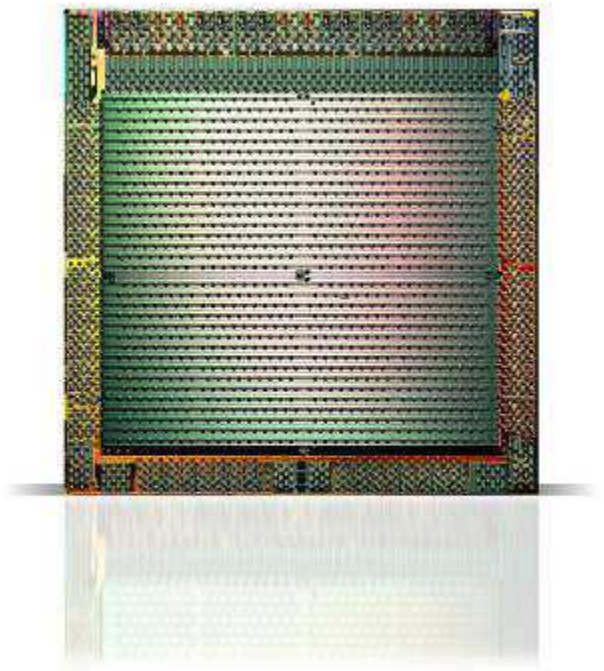
2. **100G Chip-Chip**
   **SFI-S @ 10 Gbps**

3. **100G Module Interface Example**
   **SFI-S/MLD (10 @ 11.3 Gbps)**



# Arria II GX FPGA – Low Cost Transceiver FPGA with High-End Capabilities

- Low cost
  - $15 entry price: EP2AGX20, 100K units in 2011
  - Half the price of competing high-end FPGAs
- High functionality
  - High-performance ALM-based fabric
  - High density - up to 260K LEs
  - Up to 16 transceivers @ 3.75 Gbps
  - Up to 12 Mbits of memory
  - Highest ratio of DSP-to-logic resources in its class
- Low power
  - Up to 50% lower power than competing high-end FPGAs
  - <100mW per transceiver channel @ 3.125 Gbps



# Arria II GX FPGA Family Plan

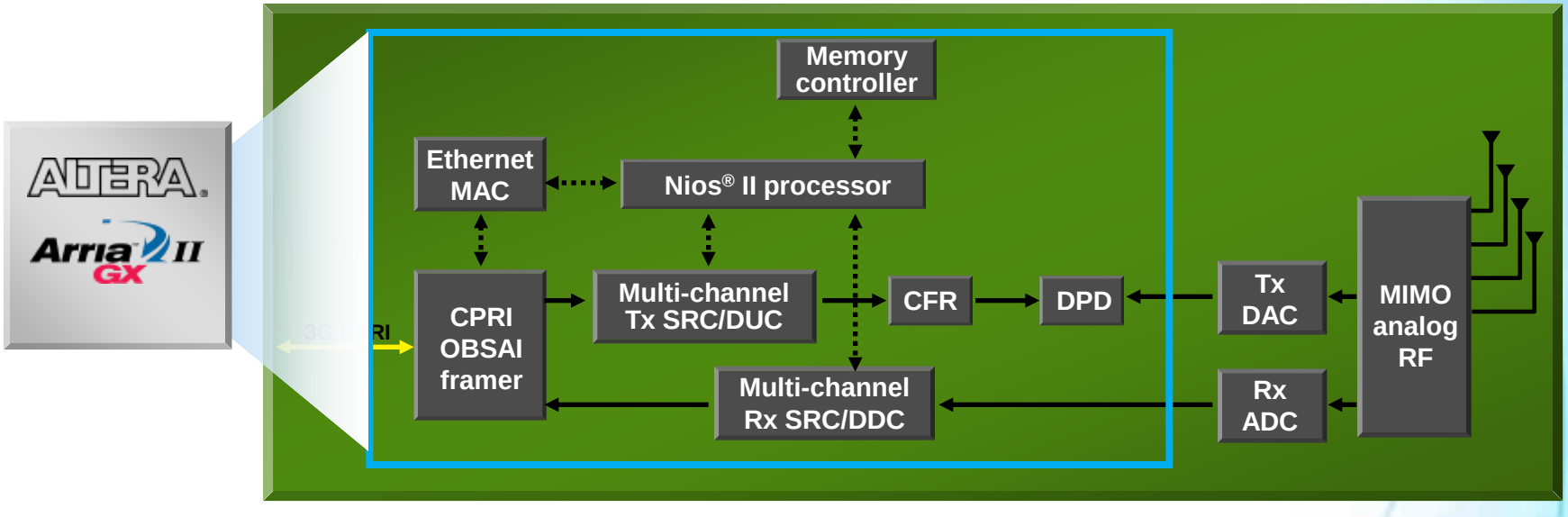
| Device | Equiv LEs | RAM Mbits/ M9K blocks | Total MLAB memory (Mbits) | 18 X 18 multipliers | Transceivers @ 3.75 Gbps | PLLs | Tx PLLs | Clks |
|---|---|---|---|---|---|---|---|---|
| EP2AGX20 | 16K | 0.7 / 87 | 0.4 | 56 | 4 | 4 | 2 | 32 |
| EP2AGX30 | 27K | 1.3 / 144 | 0.5 | 144 | 4 | 4 | 2 | 32 |
| EP2AGX45 | 45K | 2.9 / 319 | 0.6 | 228 | 8 | 4 | 4 | 32 |
| EP2AGX65 | 63K | 4.4 / 495 | 0.8 | 312 | 8 | 4 | 4 | 32 |
| EP2AGX95 | 94K | 5.5 / 612 | 1.2 | 448 | 12 | 6 | 6 | 40 |
| EP2AGX125 | 124K | 6.6 / 730 | 1.6 | 576 | 12 | 6 | 6 | 40 |
| EP2AGX190 | 190K | 7.6 / 840 | 2.4 | 656 | 16 | 6 | 8 | 40 |
| EP2AGX260 | 256K | 8.5 / 950 | 3.2 | 736 | 16 | 6 | 8 | 40 |

# Arria II GX FPGA Package Offerings

| Device | U358 | F572 | F780 | F1152 |
|---|---|---|---|---|
| | 0.8 mm<br>17 x 17 | 1.0 mm<br>25 x 25 | 1.0 mm<br>29 x 29 | 1.0 mm<br>35 x 35 |
| EP2AGX20 | 156 (32,4) | 252 (56,4) | | |
| EP2AGX30 | 156 (32,4) | 252 (56,4) | | |
| EP2AGX45 | 156 (32,4) | 252 (56,8) | 364 (84,8) | |
| EP2AGX65 | 156 (32,4) | 252 (56,8) | 364 (84,8) | |
| EP2AGX95 | | 260 (56,8) | 372 (84,12) | 452 (104,12) |
| EP2AGX125 | | 260 (56,8) | 372 (84,12) | 452 (104,12) |
| EP2AGX190 | | | 372 (84,12) | 612 (144,16) |
| EP2AGX260 | | | 372 (84,12) | 612 (144,16) |

Number of I/Os (LVDS, number of transceivers)

# Example: Remote Radio Head



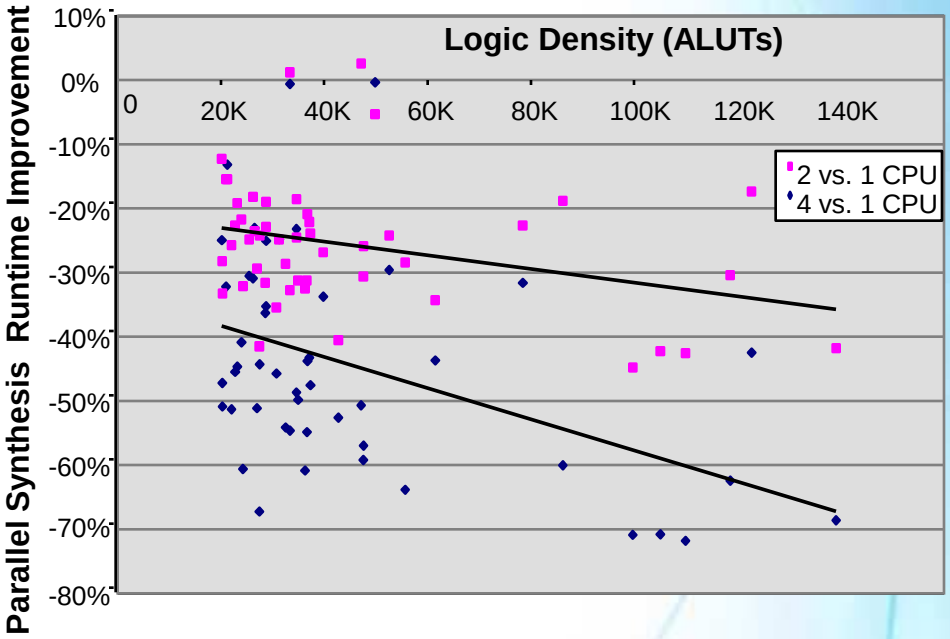

- Lowest power possible (<5W)
- 1-200K LEs
- 6-10 Mbits internal memory
- 500 18x18 multipliers
- ~250-MHz operating frequency
- Transceivers for CPRI and GE

# Quartus II Software Innovations

- Incremental compilation
  - Increase team productivity through support for team-based design flows using top-down or bottom-up methodologies
- Multi-processor support
  - Get faster compilation times (30% with 4 processors) with multi-processor systems
- TimeQuest timing analyzer
  - Close timing faster with the easy-to-use with SDC support
- PowerPlay technology
  - Automatically optimizing your design for low power
- SOPC Builder
  - Improve productivity with automatic integration of your intellectual property (IP) cores and user components
- SignalTap® II logic analyzer
  - Shorten verification cycles with in-system debugging of your design
- Low memory usage

# Example: Parallel Synthesis Speed-up

- Definition of parallel compilation
  - The use of multiple processors or multi-cores on a single computer during compilation
- Parallel synthesis during incremental compilation
  - Design must contain partitions (QIC)
    - Partitions are synthesized in parallel
  - *Off* by default




| | Map | | Total Flow | |
|---|---|---|---|---|
| # Processors | 2 | 4 | 2 | 4 |
| Compile Time Speed-up | 1.4x | 1.9x | 1.1x | 1.16x |
| Peak Working Set * | 1.6x | 2.3x | | |

** Set of memory pages recently touched by threads in the process*

# Summary

- Stratix IV GT FPGA = Highest Bandwidth
  - 11.3Gbps 48 transceivers
  - 1~1.6Gbps 900 user IO
  - 1,300 RAM blocks
- Arria II GX FPGA = Low-Cost Transceiver FPGA with High-End Capabilities
  - ½ Watt and $15.00
  - 3.75Gbps 16 transceiver
  - 800MHz 600 user IO
  - 950 RAM blocks