Ultra Low Power FPGA Fuels Faster Feature Evolution in Mobile Applications

John Birkner
VP, Strategic Marketing
SiliconBlue Technologies

Ultra-low power, Single-chip SRAM FPGA Targets Handheld Consumer Applications

PMP / Games

Netbooks

Pico Projectors

Smart Phones

DSC

Power?

Cost? New Features? Size?

Time to Market?

ePaper eBook

Smart Cards

MID

GPS

POS / iPDA

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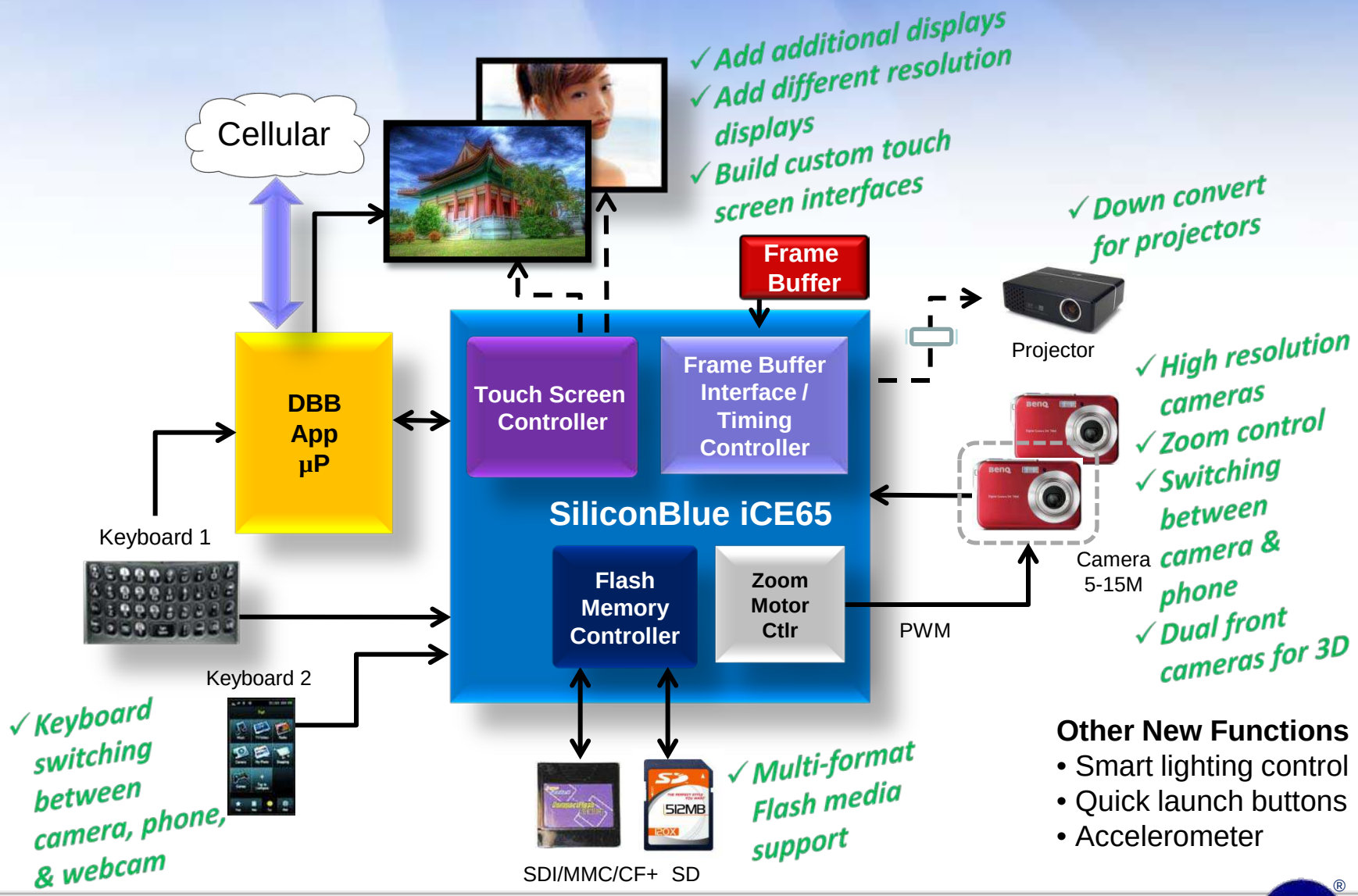
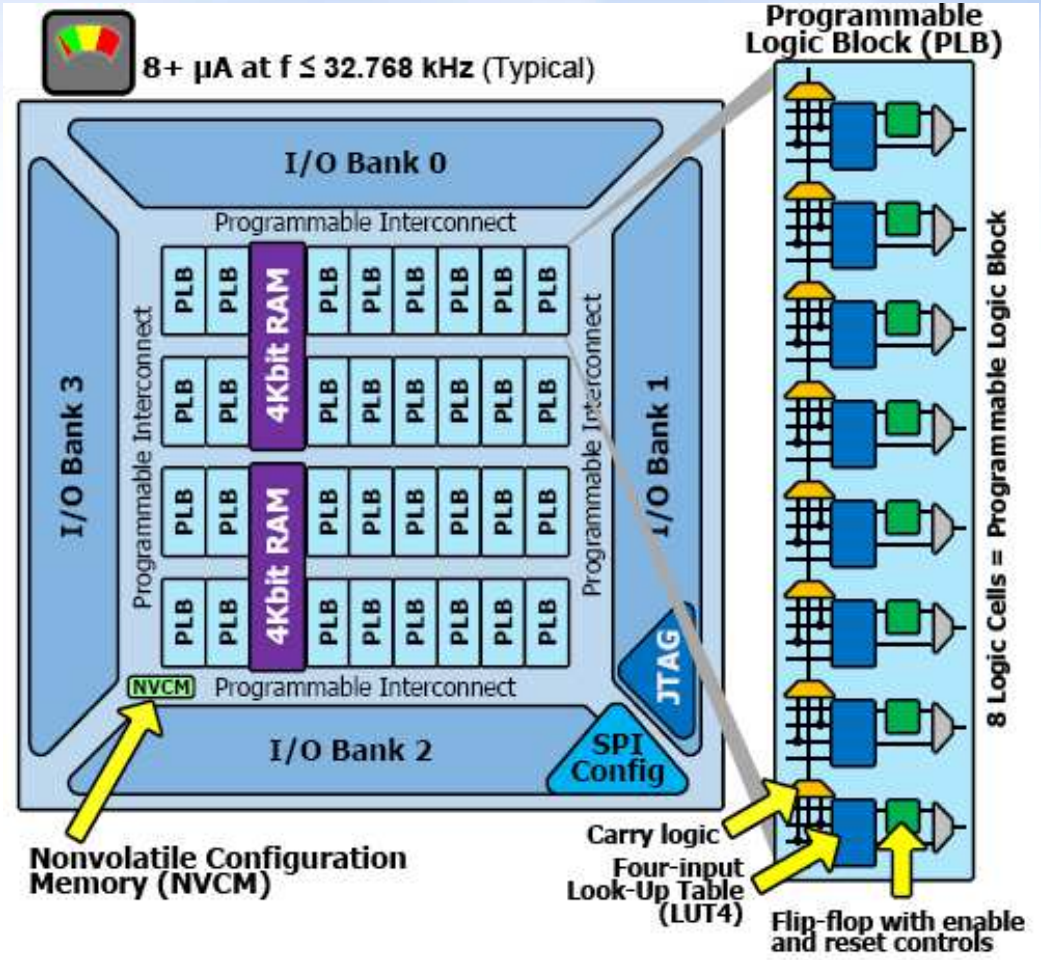
What Solutions does FPGA provide?



iCE65 FPGA Architecture



- Ultra low power
- Array of Programmable Logic Blocks (PLBs)
- Surrounded by four I/O Banks
- 4Kbit RAM Blocks
- Programmable interconnect
- Non-Volatile Configuration Memory (NVCM)
- SPI interface

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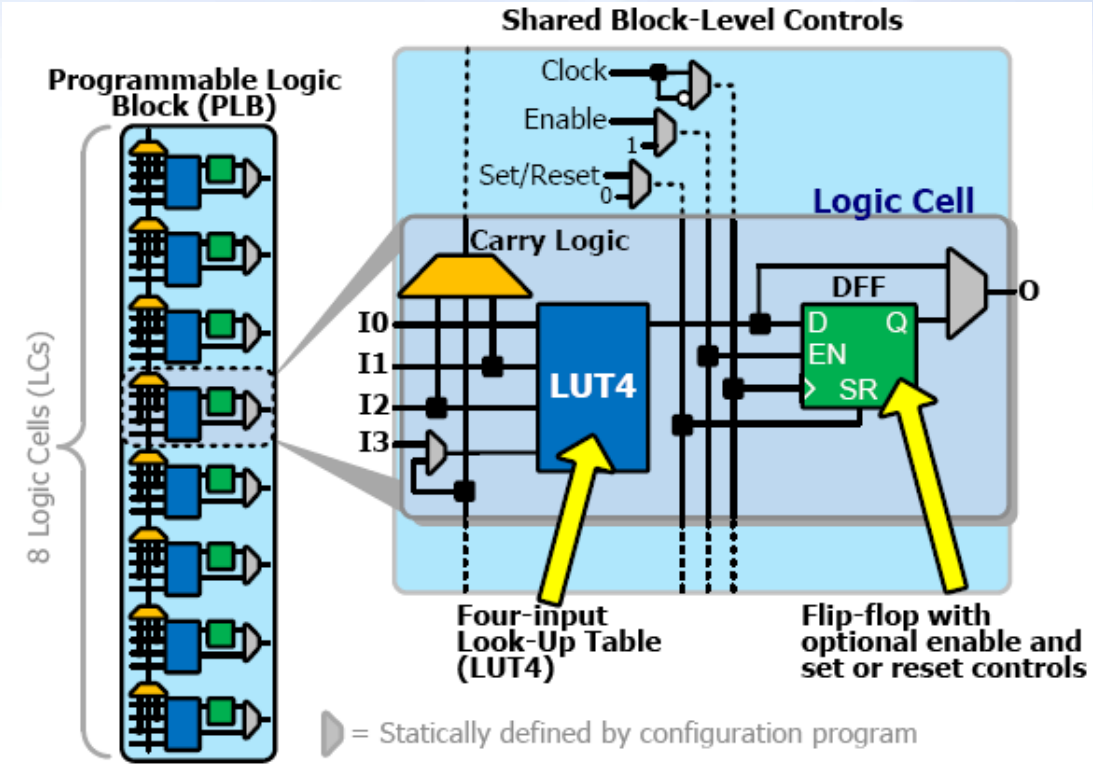
Programmable Logic Block (PLB)



- Eight 4-input Look-up Tables (LUT4)
- Eight ‘D’ flip-flops with shared clock, clock enable, set/reset control
- Fast carry logic
- Familiar, well supported by logic synthesis tools

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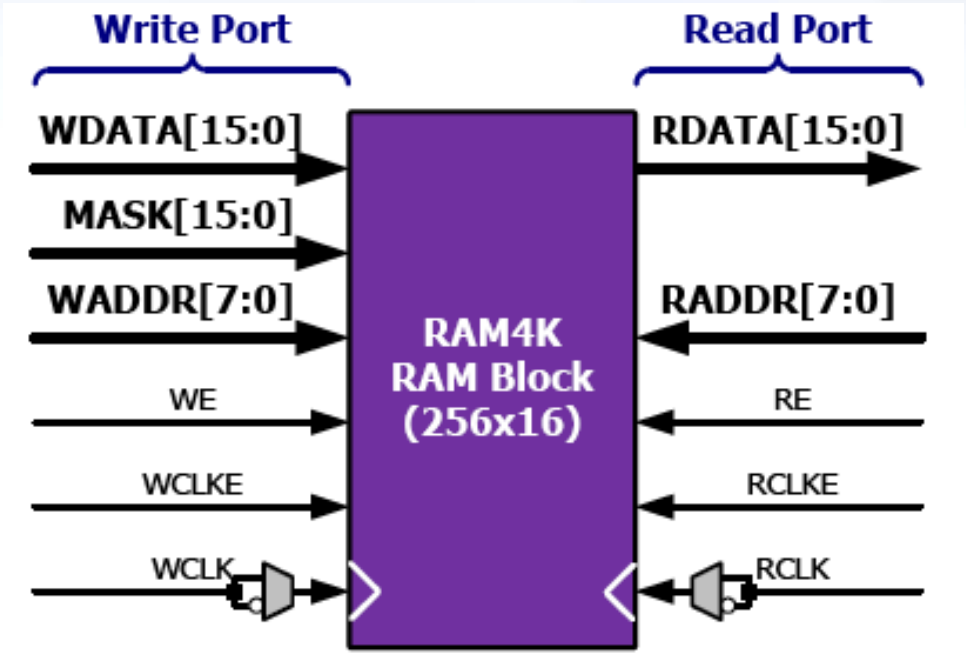
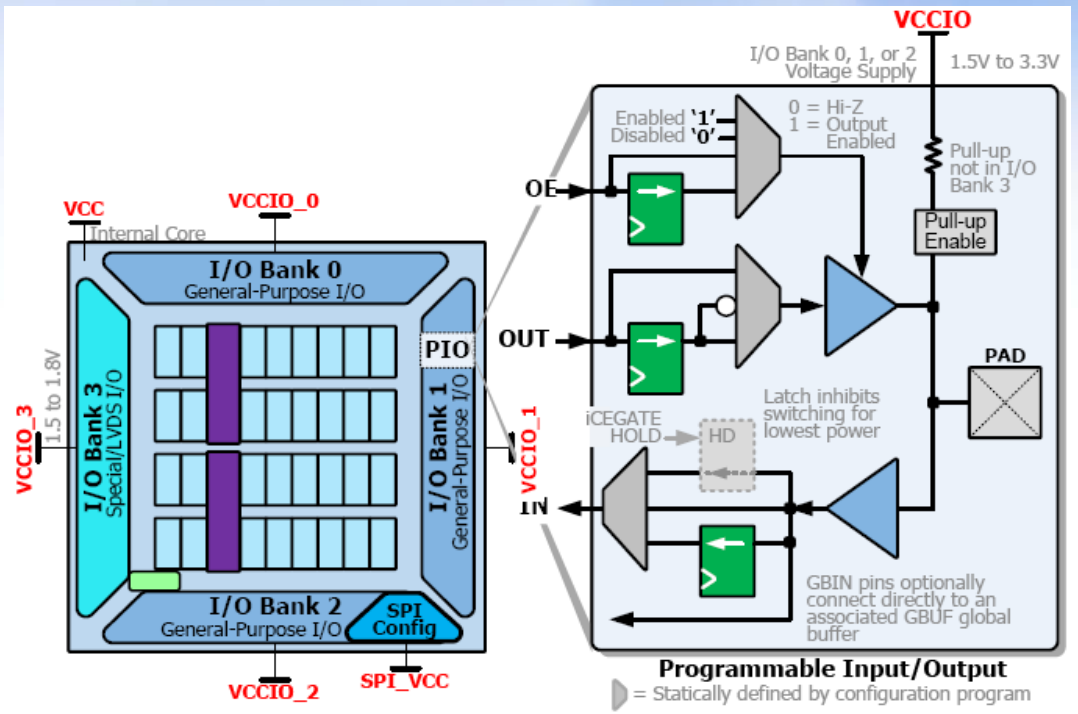
RAM 4K Memory Block



- Implements variety of functions:
  - Random-access memory (RAM)
  - Single-port RAM with a common address, enable, and clock control lines
  - Two-port RAM with separate read and write control lines, address inputs, and enable
  - Register file and scratchpad RAM
  - First-In, First-Out (FIFO) memory for data buffering applications
  - Circuit buffer
  - 256-deep by 16-wide ROM with registered outputs, contents loaded during configuration
  - Sixteen different 8-input look-up tables
  - Function or waveform tables such as sine, cosine, etc.
  - Correlators or pattern matching operations
  - Counters, sequencers

Programmable Input/Output (PIO)



I/O Standards:

LVCMOS33	LVCMOS25, LVDS	LVCMOS18
LVCMOS18	SubLVDS	LVCMOS15
SSTL25	SSTL18	MDDR

Bank	Device Edge	Supply Input	3.3V	2.5V	1.8V	1.5V
0	Top	VCCIO_0	Yes	Yes	Yes	Outputs only
1	Right	VCCIO_1	Yes	Yes	Yes	Outputs only
2	Bottom	VCCIO_2	Yes	Yes	Yes	Outputs only
3	Left	VCCIO_3	No	Yes	Yes	Yes
SPI	Bottom Right	SPI_VCC	Yes	Yes	Yes	No

- Connects external components to the PLBs and RAM4K blocks via programmable interconnect
- Individual pins grouped into 1-of-4 I/O banks
  - Multi-functions
- I/O Bank #3 has add'l functionality
  - LVDS differential I/O
  - Mobile DDR memory interface

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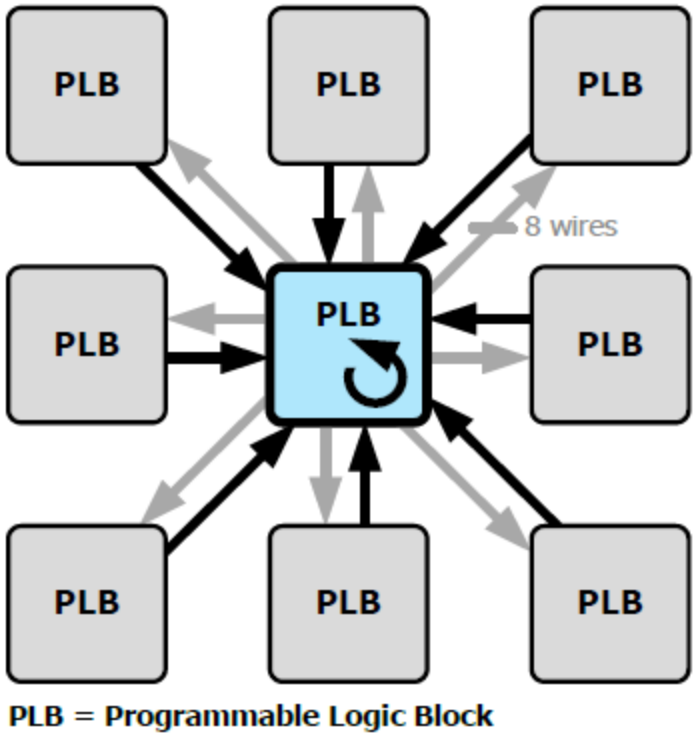
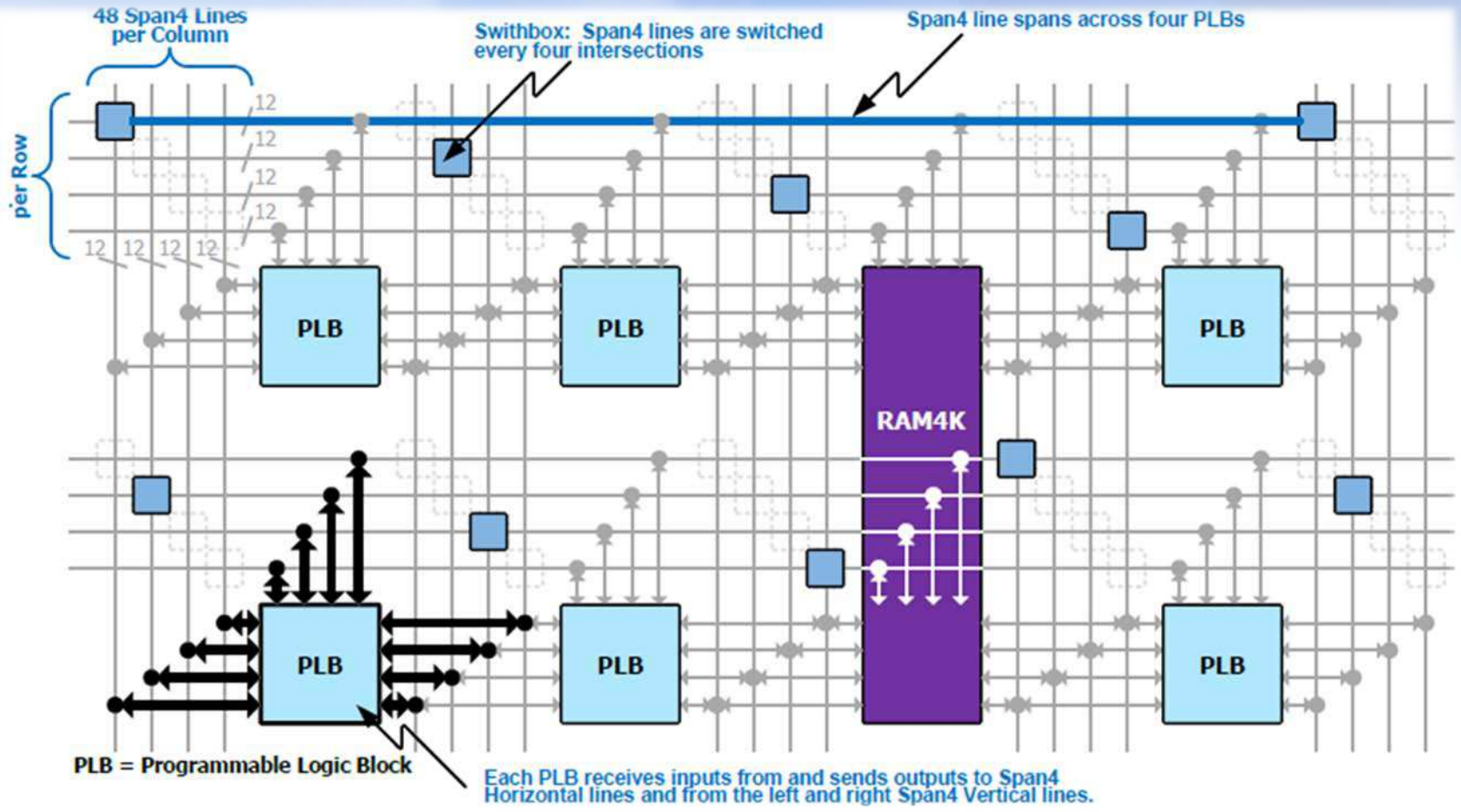
Programmable Interconnect

- Hierarchy of resources:
  - Nearest Neighbor Connections between a PLB and its surrounding neighbors
  - Span4 Connections & switchboxes
  - Span12 Connections & switchboxes



Span4 Connection Resourses



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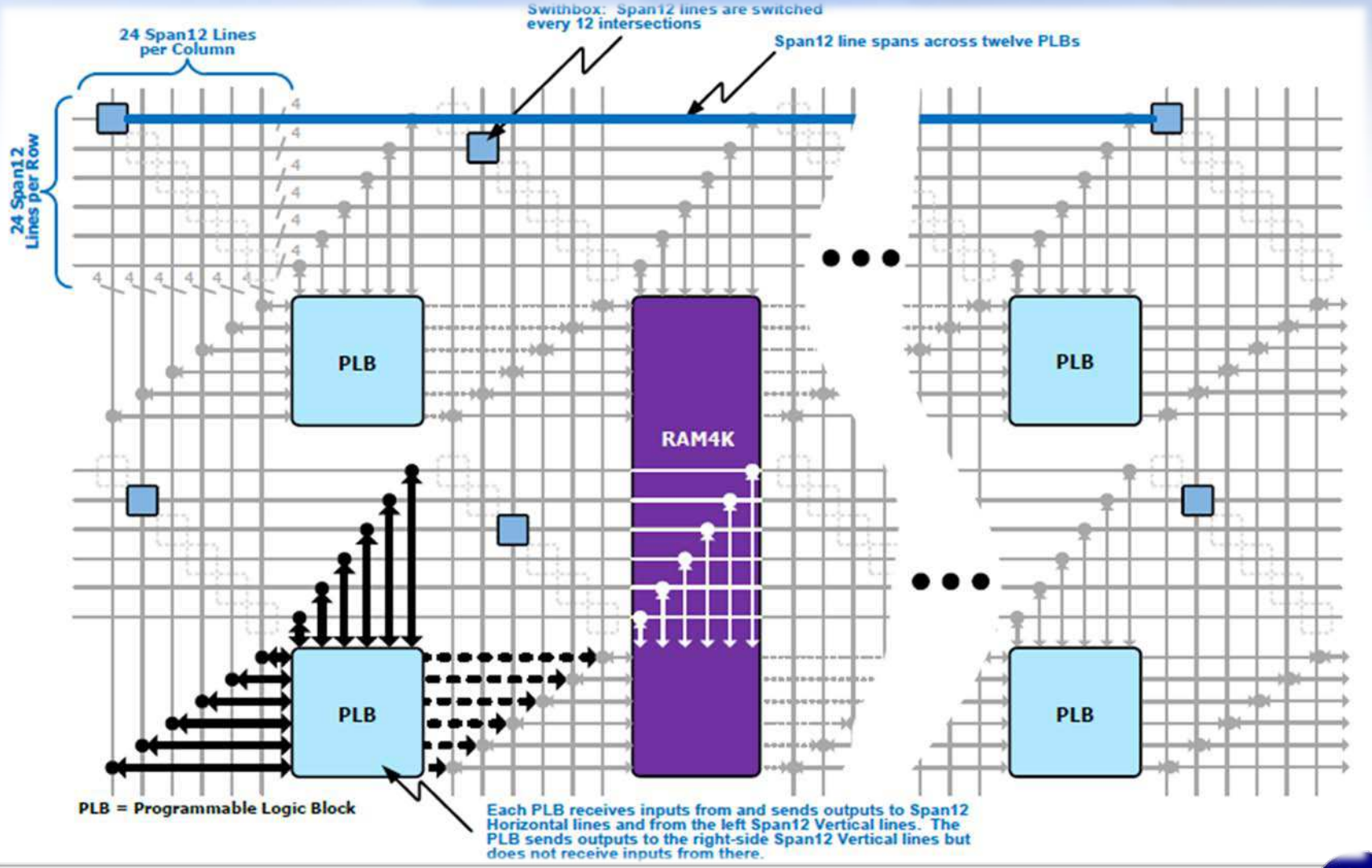
Span12 Connection Resources



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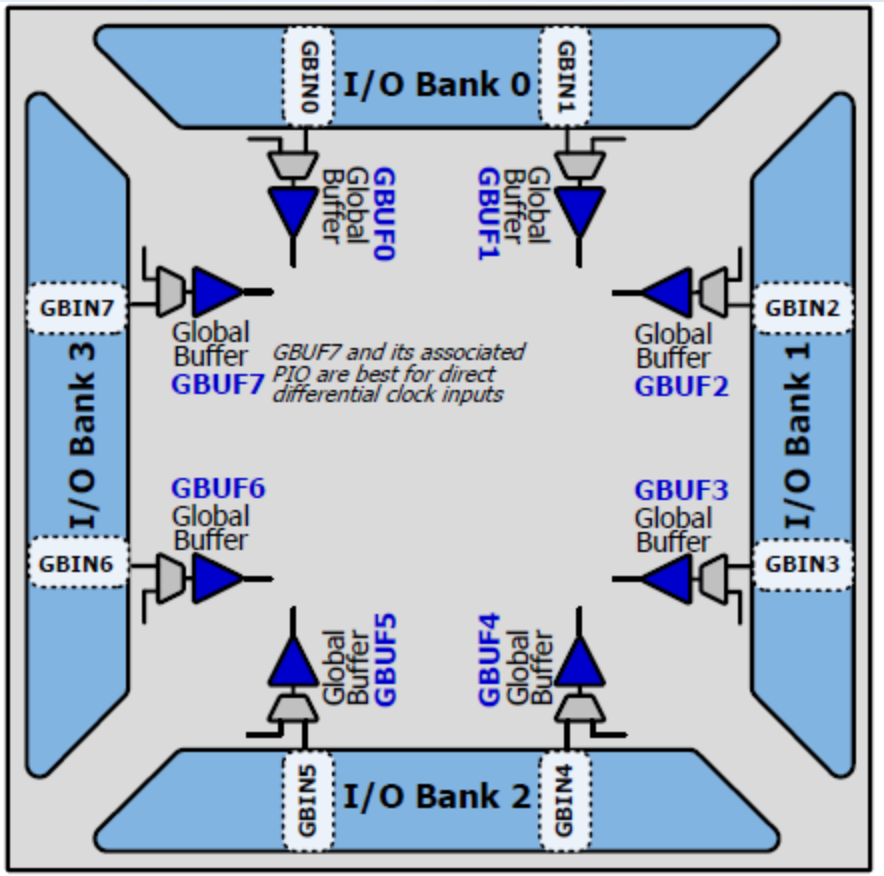
Global Routing Resources



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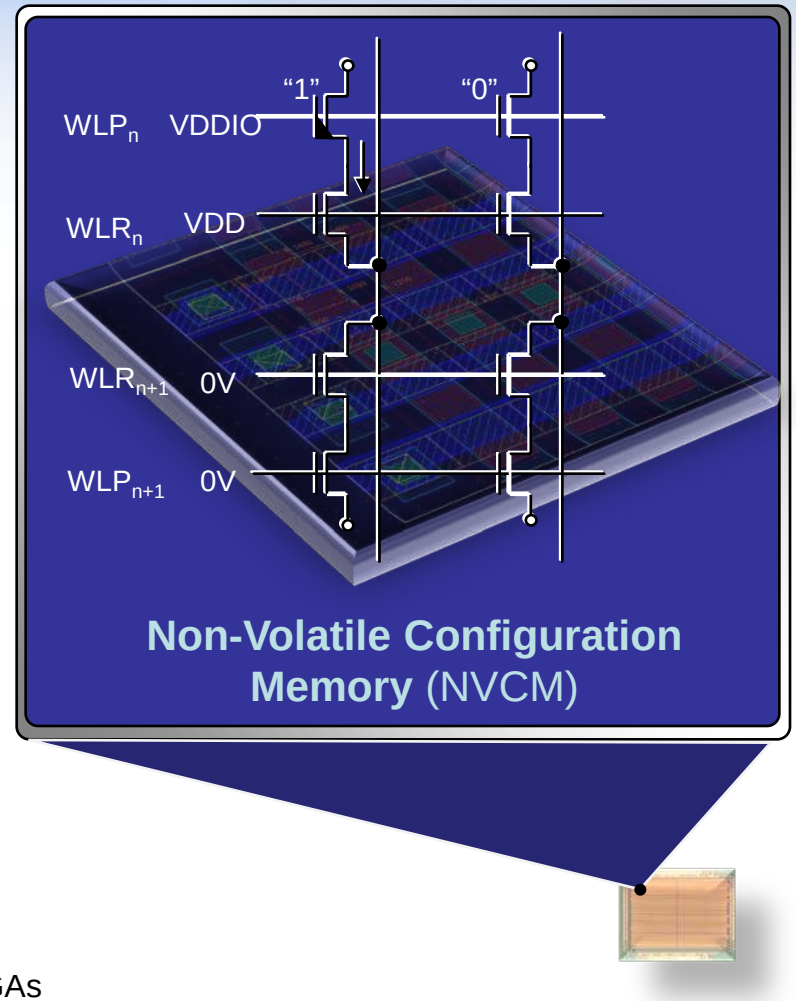
Unique Self-Configuration Option (NVCM)

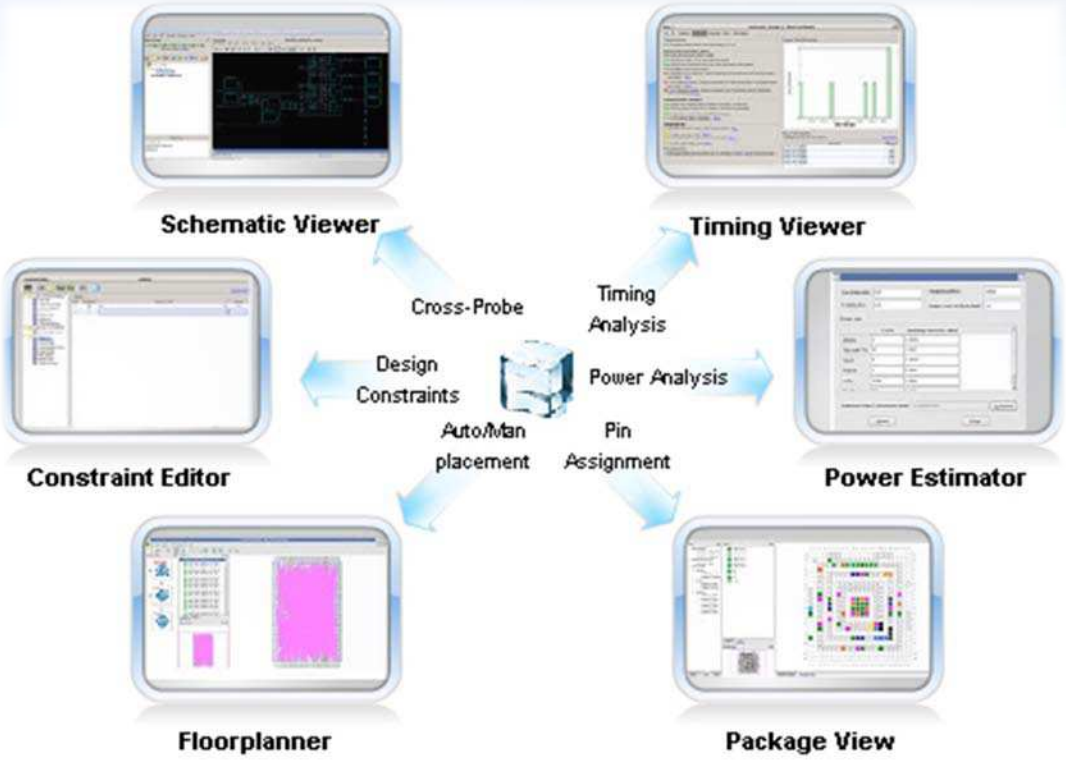
- Industry's only single chip, SRAM FPGA
  - Reprogrammable, reconfigurable as any SRAM FPGA thru SPI port in milliseconds
  - NVCM configures on power up
  - Secure
- Uses TSMC 65LP[1] standard CMOS process
  - Smallest die, lowest cost
  - Rapidly ramp volume



Note 1. Two generation competitive lead versus Flash FPGAs

iCEcube Design Tool Suite

- Verilog & VHDL
- Timing driven physical synthesis Magma tools
- Windows or Linux
- Power Analysis & Management tools



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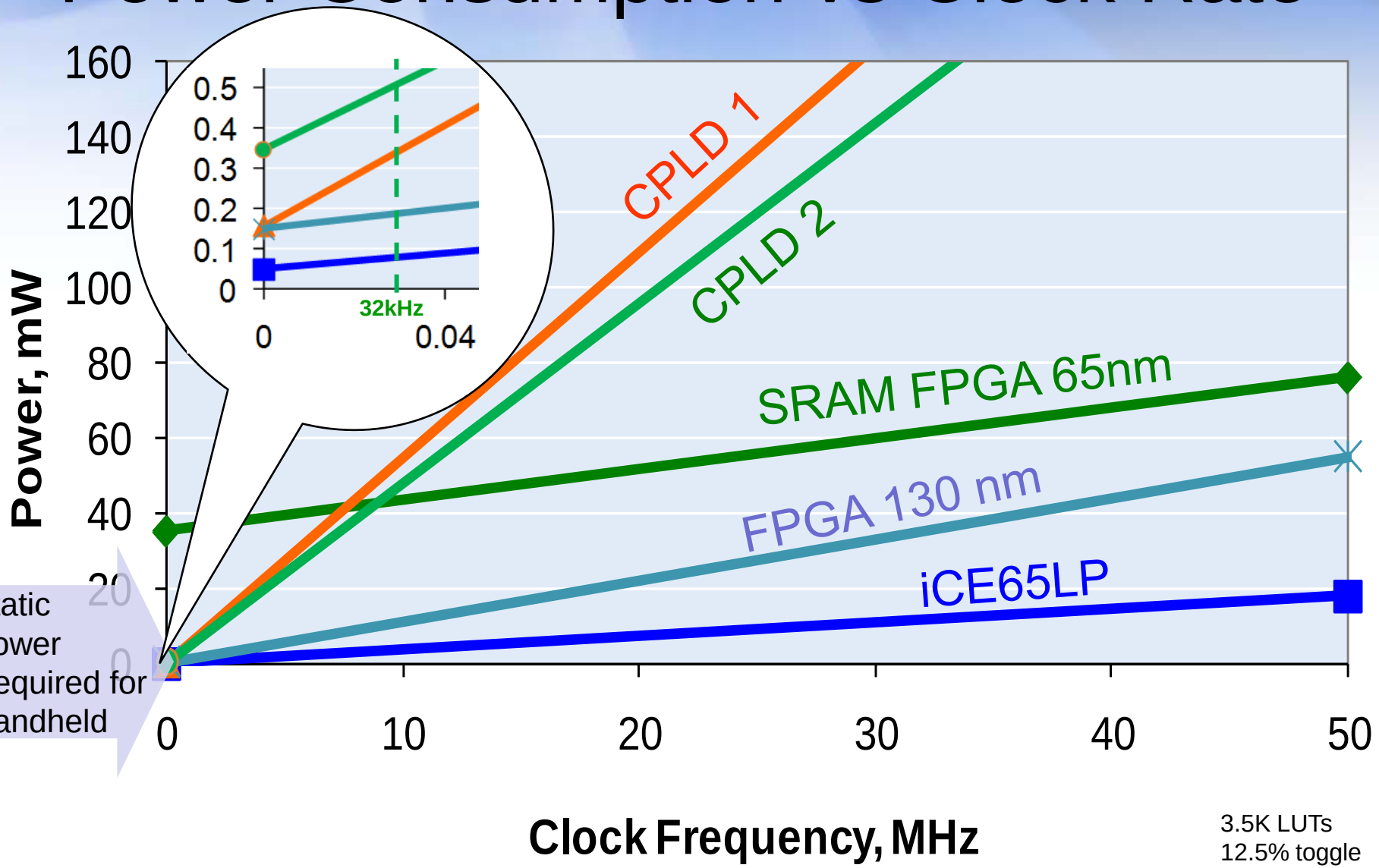
Power Consumption vs Clock Rate



3.5K LUTs
12.5% toggle

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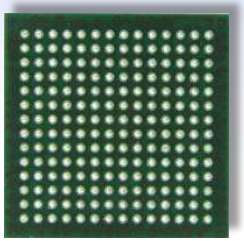
iCE65 mobileFPGA™ Family

Features	iCE65L02	iCE65L04	iCE65L08	iCE65L16
FPGA System Gates	~100K	~200K	~400K	~800K
Logic Cells	1,792	3,520	7,680	16,896
Programmable I/O (max I/O / LVDS channels)	128/18	176/20	222/25	384/54
Embedded RAM Bits	64K	80K	128K	384K
Sleep current (0 KHz, Vcc=0.8V)	3 µA	5 µA	11 µA	50 µA
Dynamic current (32 KHz)[1]	8 µA	15 µA	30 µA	75 µA
Dynamic current (32 MHz)[1]	3 mA	6 mA	12 mA	24 mA
Availability	NOW	NOW	NOW	2010

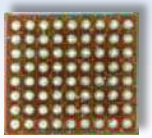
iCE65 Small Form Factor Solutions

CB196
L04, L08
(150/18)



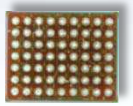
.5 mm pitch
8x8 mm

CC72
L08 (55/8)



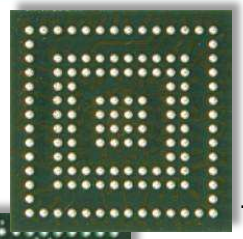
.5 mm pitch
4x5 mm

CS63
L04 (48/4)



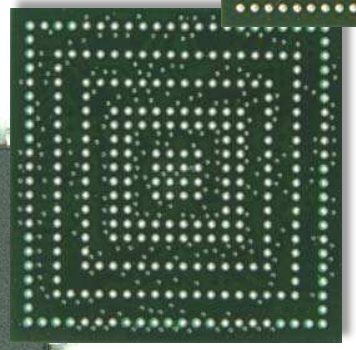
.4 mm pitch
3x4 mm

CB132
L02, L04
(95/11)



.5 mm pitch
8x8 mm

CB284
L04, L08, L16
(222/25)



.5 mm pitch
12x12 mm

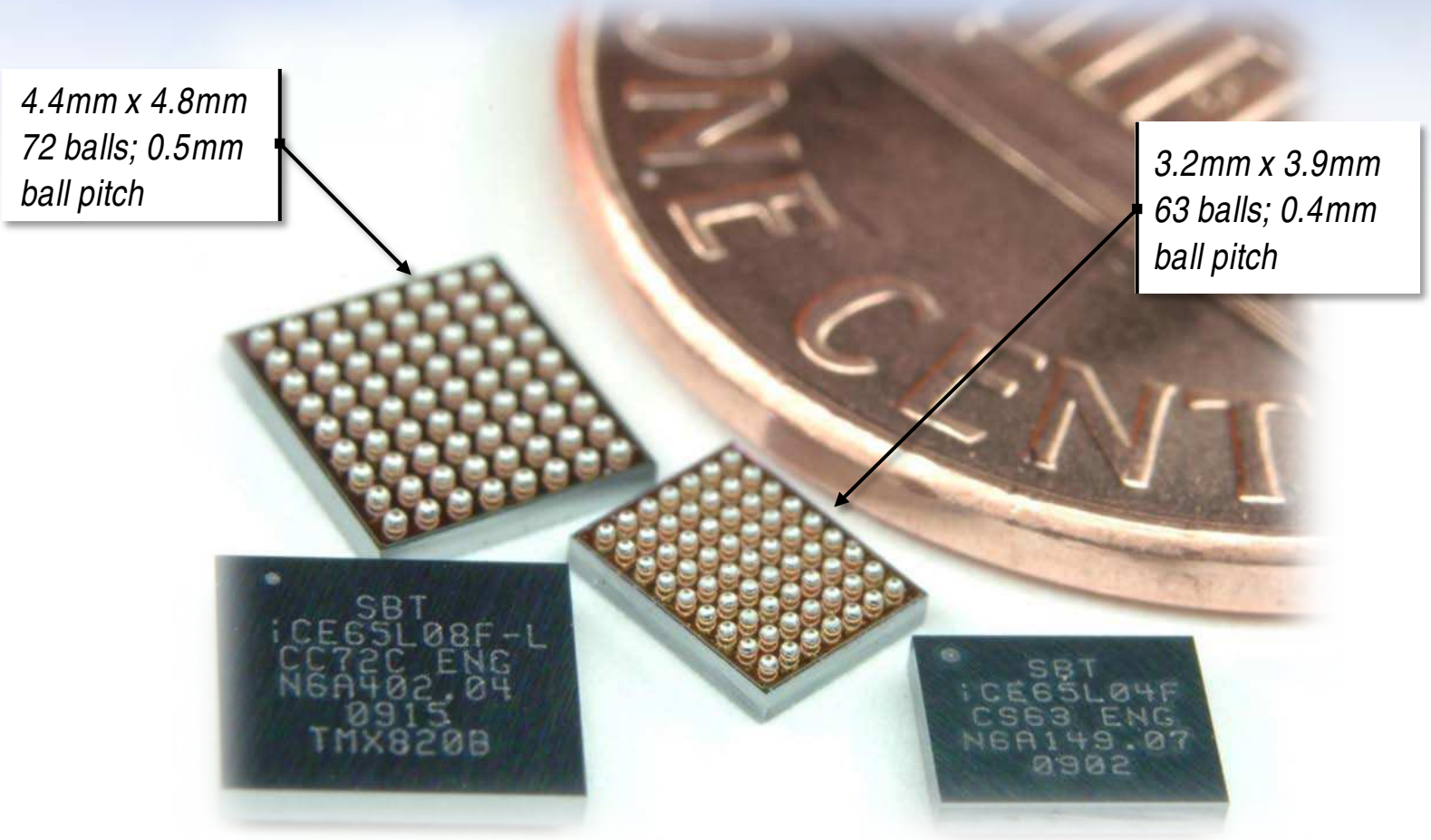
VQ100
L04
(72/9)[1]

.5 mm pitch
14x14 mm

[1](Max I/O / Diff Pairs)

Wafer Level Chip Scale Packages

Optimized for Small Handheld Products



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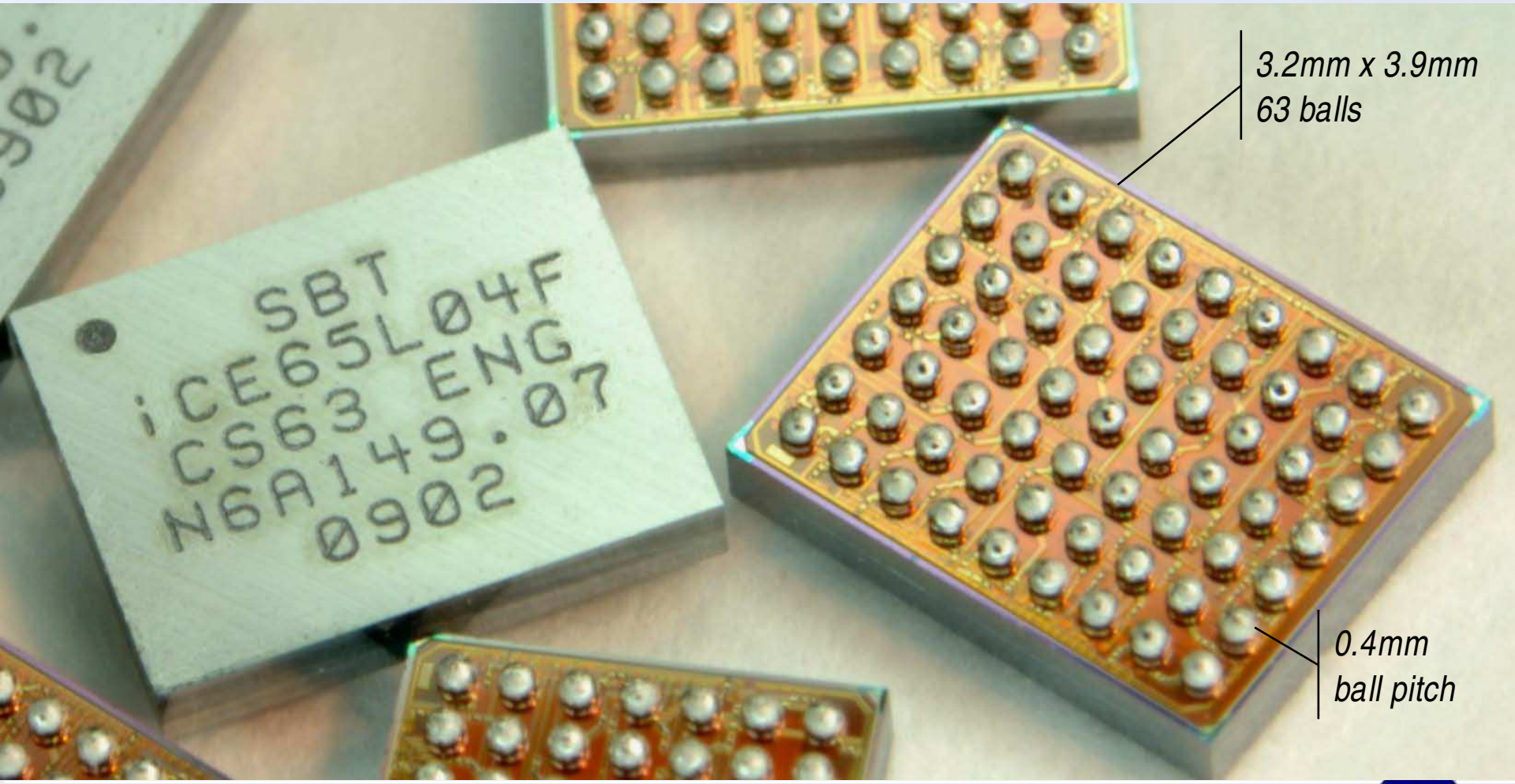
Small Form Factor WLCSP: .4mm pitch

Key Features:

- ~200K System Gates
- 48 I/Os; 4 diff pairs
- Icc0 $_{sleep}$ = 5µA
- Icc32K = 15µA @ 32KHz



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iCE65L04 & iCE65L08 FPGAs Known Good Die

iCE DiCE™: iCE65L08 Ultra Low-Power FPGA Known Good Die

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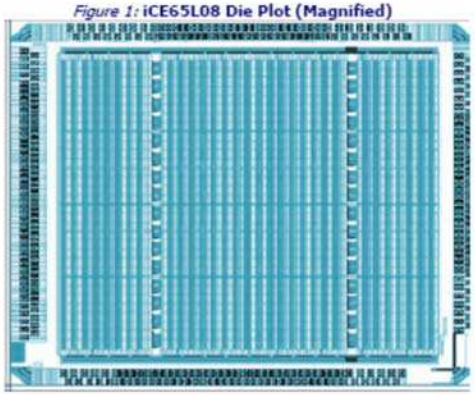
March 23, 2009 (1.0.3) — **Advance Information (SUBJECT TO CHANGE)**

Features

- **First ultra low-power programmable logic family specifically designed for hand-held applications and long battery life**
  - Less than 30 µA typical standby current (-U); no special power down modes required
  - Lowest active power consumption of any comparable programmable logic family
  - Lowest heat dissipation on power-sensitive applications
- **Known Good Die (KGD)**
  - Ideal for System-in-Package (SiP), stacked-die, or multi-chip module applications
  - Ideal for Chip on Board (COB) mounting in low-cost consumer products
  - Various temperature range, thickness, and delivery method options
- **Reprogrammable from a variety of sources**
  - Self-loading from secure, internal Nonvolatile Configuration Memory (NVCM)
    - Superior design and intellectual property (IP) protection; no exposed configuration data
    - Single-chip programmable solution
    - Low-cost, high-volume configuration source
  - Self-loading from external, commodity SPI serial Flash PROM
  - Downloaded by processor using SPI-like serial interface
- **Built on proven, high-volume 65 nm, low-power CMOS technology delivering lowest possible power and cost**

Figure 1: **iCE65L08 Die Plot (Magnified)**



- **Up to 200+ MHz internal performance**
- **Flexible programmable logic and programmable interconnect fabric**
  - Over 7,600 four-input look-up tables (LUT4) and flip-flops
  - Low-power logic and interconnect
- **On-chip, 4Kbit RAM blocks; 32 per device**
- **Flexible I/O blocks to simplify system interfaces**
  - 222 programmable I/O pads
  - Four independently-powered I/O banks support 3.3V, 2.5V, or 1.8V voltage standards
  - Differential LVDS I/O pairs

iCE DiCE™: iCE65L04 Ultra Low-Power FPGA Known Good Die

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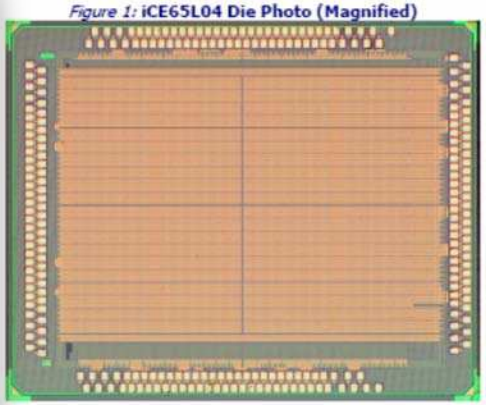
Preliminary (SUBJECT TO CHANGE)

Figure 1: **iCE65L04 Die Photo (Magnified)**



(IP)

- **Up to 200+ MHz internal performance**
- **Flexible programmable logic and programmable interconnect fabric**
  - Over 3,500K four-input look-up tables (LUT4) and flip-flops
  - Low-power logic and interconnect
- **On-chip, 4Kbit RAM blocks; 20 per device**
- **Flexible I/O blocks to simplify system interfaces**
  - 176 programmable I/O pads
  - Four independently-powered I/O banks support 3.3V, 2.5V, or 1.8V voltage standards
  - Differential LVDS I/O pairs

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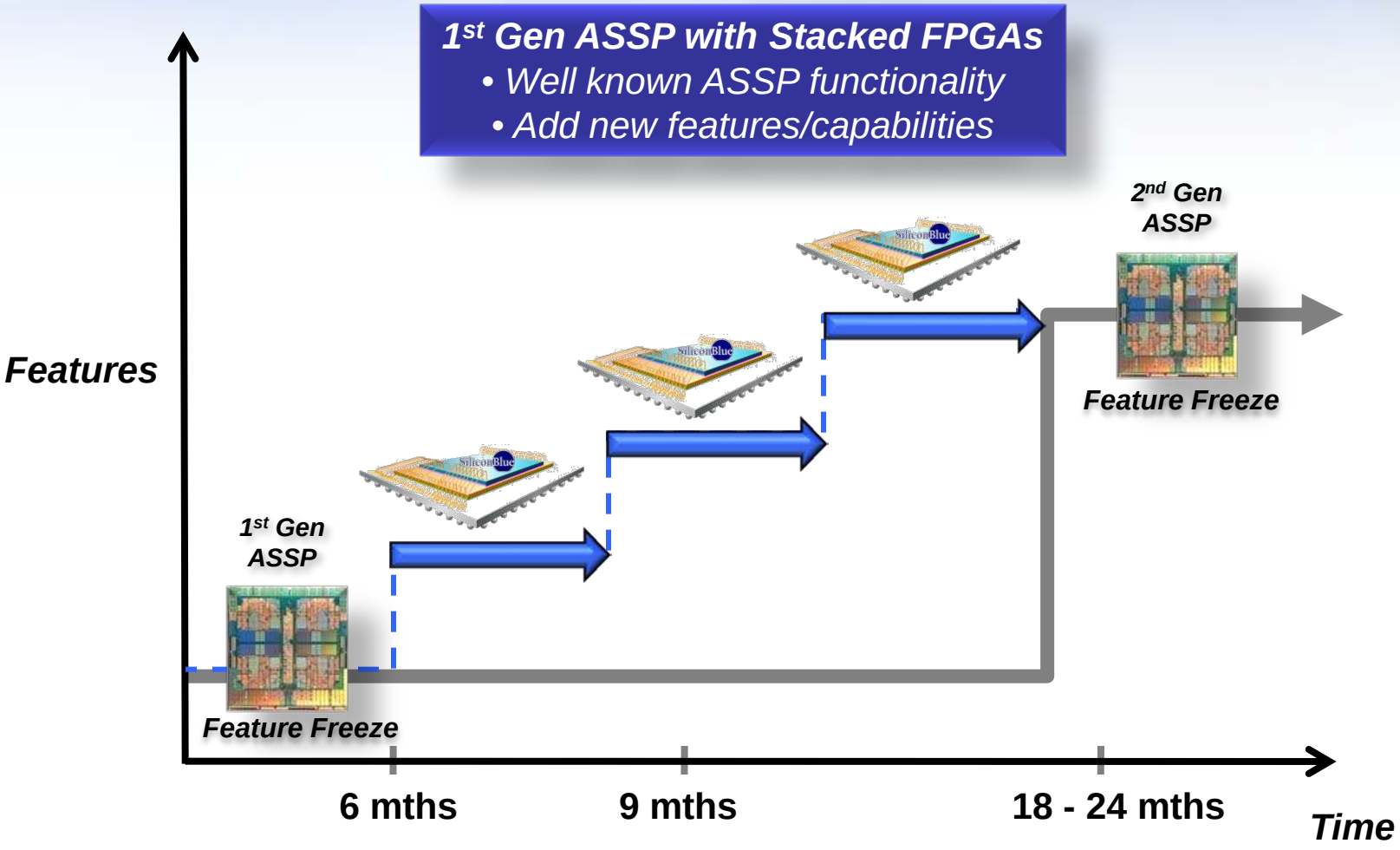
New Products, New Features, More Revenue



Example SiliconBlue IP: Smartphone

Turn-Key Solutions	Resources FFs	LUTs	IOs	RAMs
48 Channel PWM Controller with I2C Interface	230	416	66	3
Backlighting Controller with Ambient Light Awareness	138	223	53	0
I2C Port Expansion Demo	74	251	66	0
Decoded Keyboard Output Display on Character LCD	891	891	76	0
Digital Picture Frame with Touch Screen	365	1254	47	5
Interactive Control of Tri-Color LEDs with PWM	90	143	63	0
48 Channel PWM Controller with SPI Interface	199	369	68	3
Voltage Level Translation Demo	0	0	7	0
SPI Port Expansion Demo	33	79	68	0
Processors				
8051 Processor	In Development*			
Embedded Processor Configuration	In Development*			
Interfaces				
I2C Master	98	196	15	0
I2C Slave	34	84	19	0
IrDA Fast	225	542	41	2
IrDA Standard	38	81	6	0
SPI Master	218	402	31	2
SPI Master for OMAP	217	401	30	2
SPI Slave	33	7	36	0
UART	140	345	30	2
Voltage Level Translation	0	0	16	0
LVDS Serializer	In Development*			
LVDS De-Serializer	In Development*			

Peripherals	Resources FFs	LUTs	IOs	RAMs
I2C to GPIO Port Expander	34	84	19	0
Keyboard Matrix Decoder	41	126	23	0
Multi-Function Port Expander	667	1565	54	8
PWM Generation	25	47	6	0
SPI to GPIO Port Expander	33	71	36	0
SPI to UART Port Expander	143	244	174	0
Touch Screen Controller	80	146	17	0
UART to UART Port Expander	10	18	28	0
Audio Data Buffer	In Development*			
Capacitive Button/Slider Controller	In Development*			
MDDI Controller	In Development*			
MP3 Decoder	In Development*			
Storage				
MemoryStick Pro Interface	101	230	33	0
SD Interface and Controller	508	1180	45	8
SDIO Interface and Controller	507	1167	45	8
SD to SD Card Copy	In Development*			
SD Full Featured Controller	In Development*			
Displays				
Graphics LCD Controller (320x240, 18-bit color)	133	415	63	0
Capacitive Touchscreen Controller	In Development*			
CMOS Imager Interface	In Development*			
Dual Display Controller	In Development*			
Preview/Review Display Controller	In Development*			
SVGA Frame Buffer	In Development*			
Memories				
Cellular RAM Controller	305	753	96	2
NAND Flash Interface	4	20	16	0
MDDR Controller	In Development*			
SL to ML NAND Flash Converter	In Development*			
MLC NAND Flash Controller	In Development*			

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Summary: Best FPGA for Consumer Handheld

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mobileFPGA™

- **"Green" solution**
- **Ultra-low power**
- **High density**
- **Smallest footprint**
- **Low price**
- **Single chip**
- **Maximum design flexibility**

Key Functions

- *Interfaces*
- *Controllers*
- *Peripherals*
- *Glue logic*
- *More…..*

High Value Benefits

- *Quickly customize off-the-shelf chips*
- *Create end product differentiation*
- *Simplify functional "convergence"*
- *Improve time-to-market*