

**HotChips21**  
**Session Six : SoCs + Clocking**

***SoC for Car Navigation Systems  
with a 53.3 GOPS Image Recognition Engine***

Aug. 25. 2009

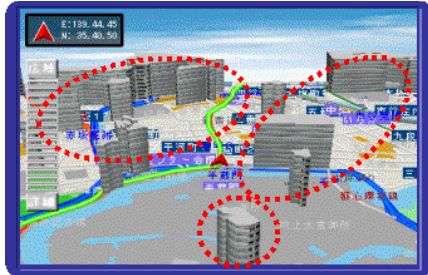
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# Contents

1. Car Navigation Systems Requirement and New SoC
2. New Image Recognition Engine (IMP-X)
3. Practical Application with IMP-X
4. Summary

## Navigation



Driver friendly user interface and graphics

## Safety



Object recognition  
Passive/Active safety



## Amusement



Digital TV display



Audio playback

Advanced car navigation systems will supply multi applications assisting and entertaining our driving



## Integrated 1-Chip Solution

# Demanded Technology for Advanced Car Navigation Systems

## **Navigation**

High Performance and various graphic processing technology

GPS technology

## **Safety**

High performance embedded image recognition technology

Connection with vehicle-control technology

## **Amusement**

Multimedia interface technology

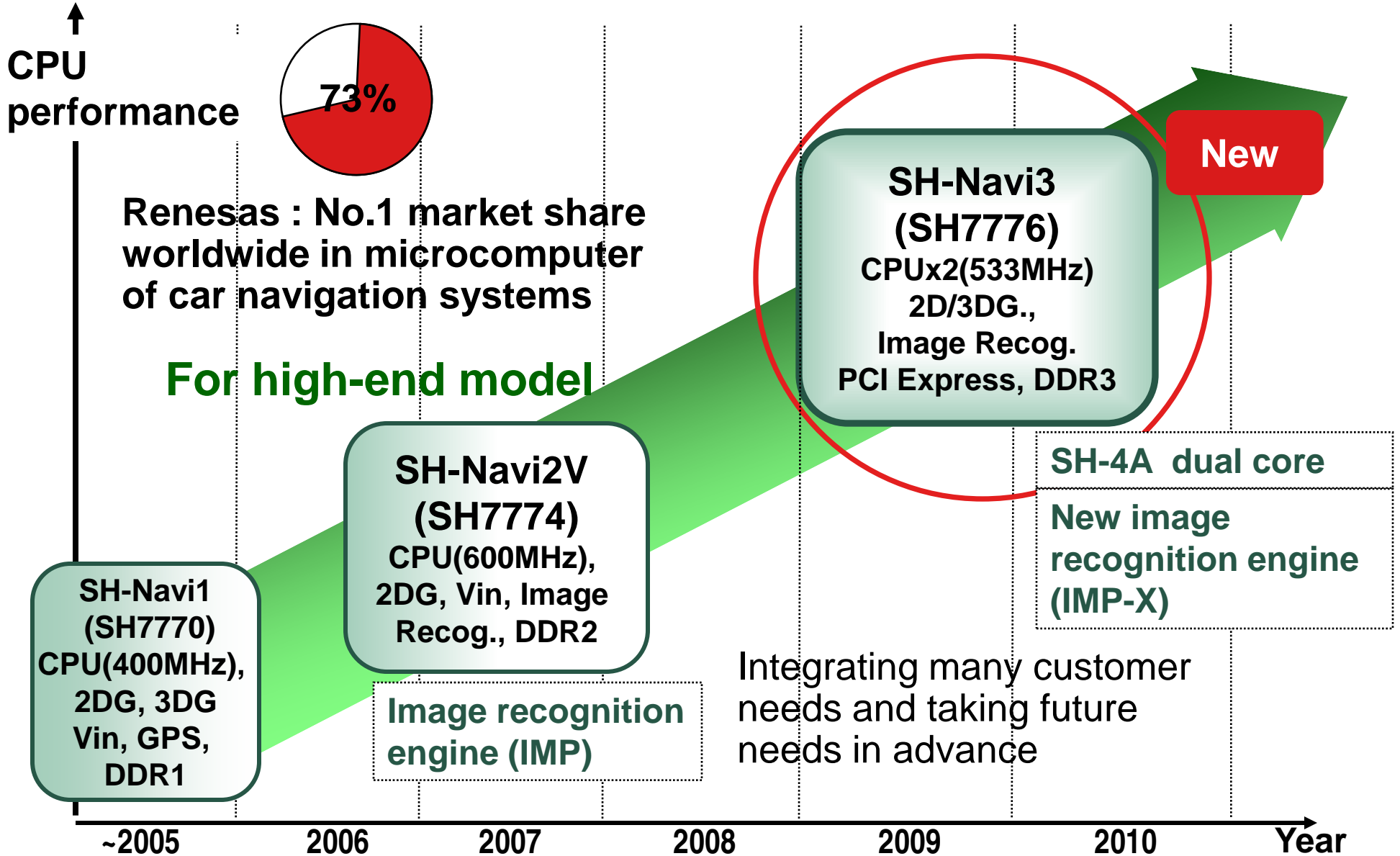
Audio / video processing technology



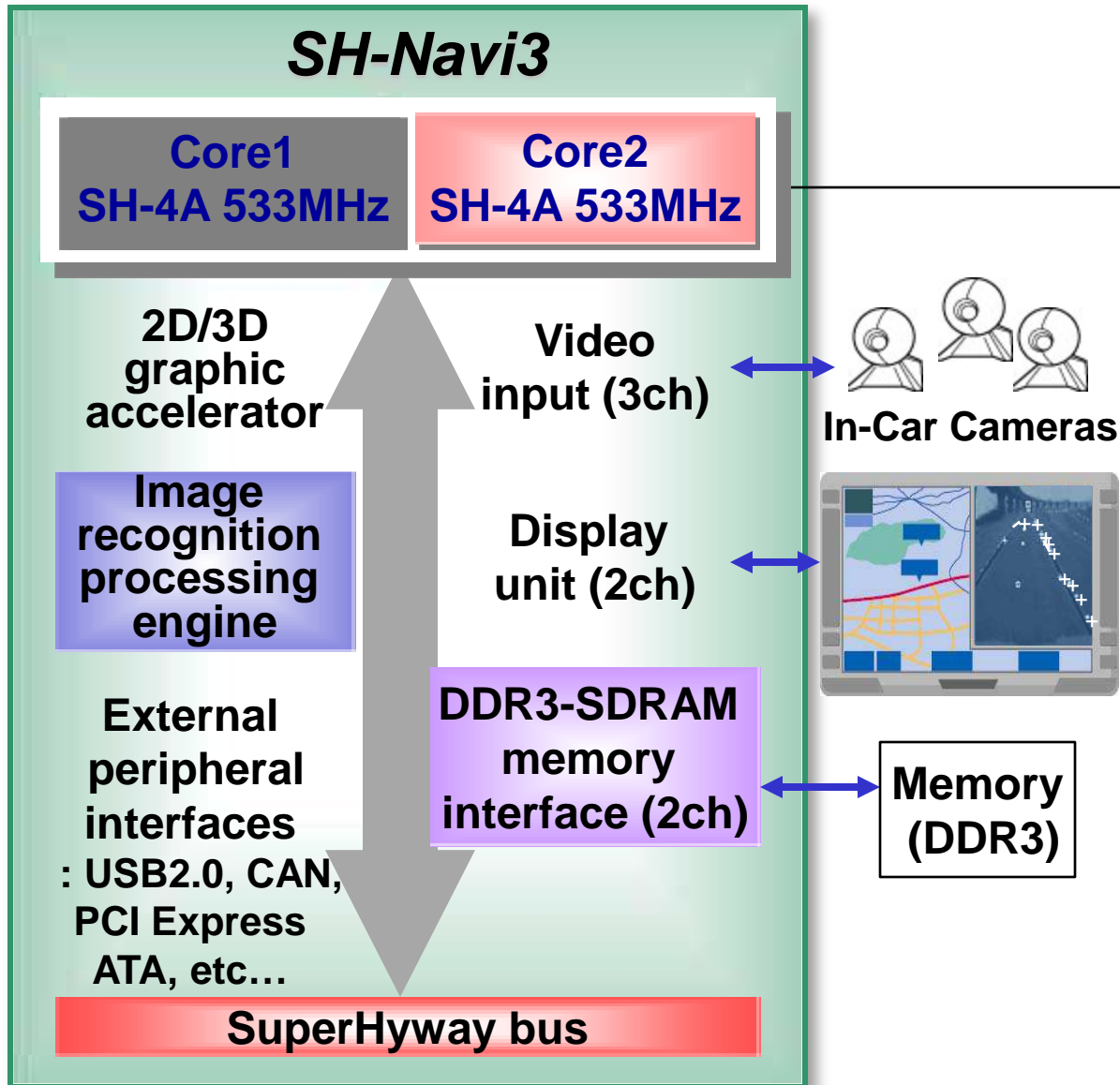
**fundamental technology**

- High-performance processor
- High speed bus and data I/O technology
- Multi-application support technology

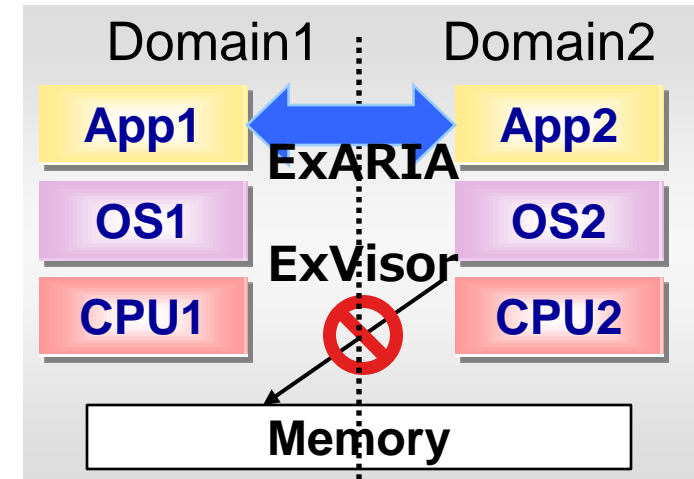
# Products Lineup for 1-Chip Embedded Car Navigation Systems



# Next Generation 1-Chip Solution : SH-Navi3



- For multi-core system
- Support AMP and SMP
- EXREAL Platform™
  1. ExVisor : inter-OS prevention technology (Domain Separation)
  2. ExARIA : inter-OS communication interface (Domain interoperation)



# Specification of SH-Navi3

	<b><i>SH-Navi2V (SH7774)</i></b>	<b><i>SH-Navi3 (SH7776)</i></b>
Technology	90nm	65nm
CPU	SH-4A 600MHz (1080MIPS) FPU : 4.2 GFLOPS	<b>SH-4A x 2</b> <b>533MHz x2 (1920MIPS)</b> FPU : 7.46 GFLOPS
Cache	I : 32KB, D : 32KB	I:32KB,D : 32KB,L2 : 128KB
Image recognition engine	38.4 GOPS engine	<b>53.3 GOPS engine</b> <b>Distortion correction module</b>
Graphics IP	2D accelerator	<b>2D/3D accelerator</b> <b>PowerVR SGX *</b>
Video in /Display unit	2ch / 1ch	3ch / 2ch
Temperature range	-40 ~ 85° C	-40 ~ 85° C
External memory	DDR2 (DDR600)	<b>DDR3 (DDR1066) 2ch</b>
Transistor count ratio	1.0	2.16

\* Imagination Technology Ltd.



## Current demands

### Object recognition for avoidance of traffic accident

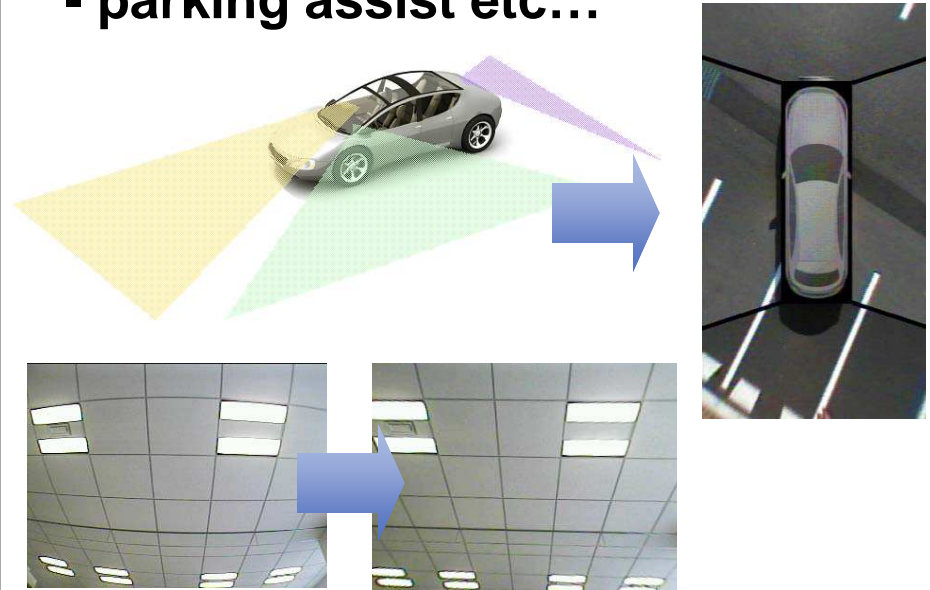
- vehicle, pedestrian, traffic sign, lane, etc...



vehicle

pedestrian

### Making more understandable images - parking assist etc...



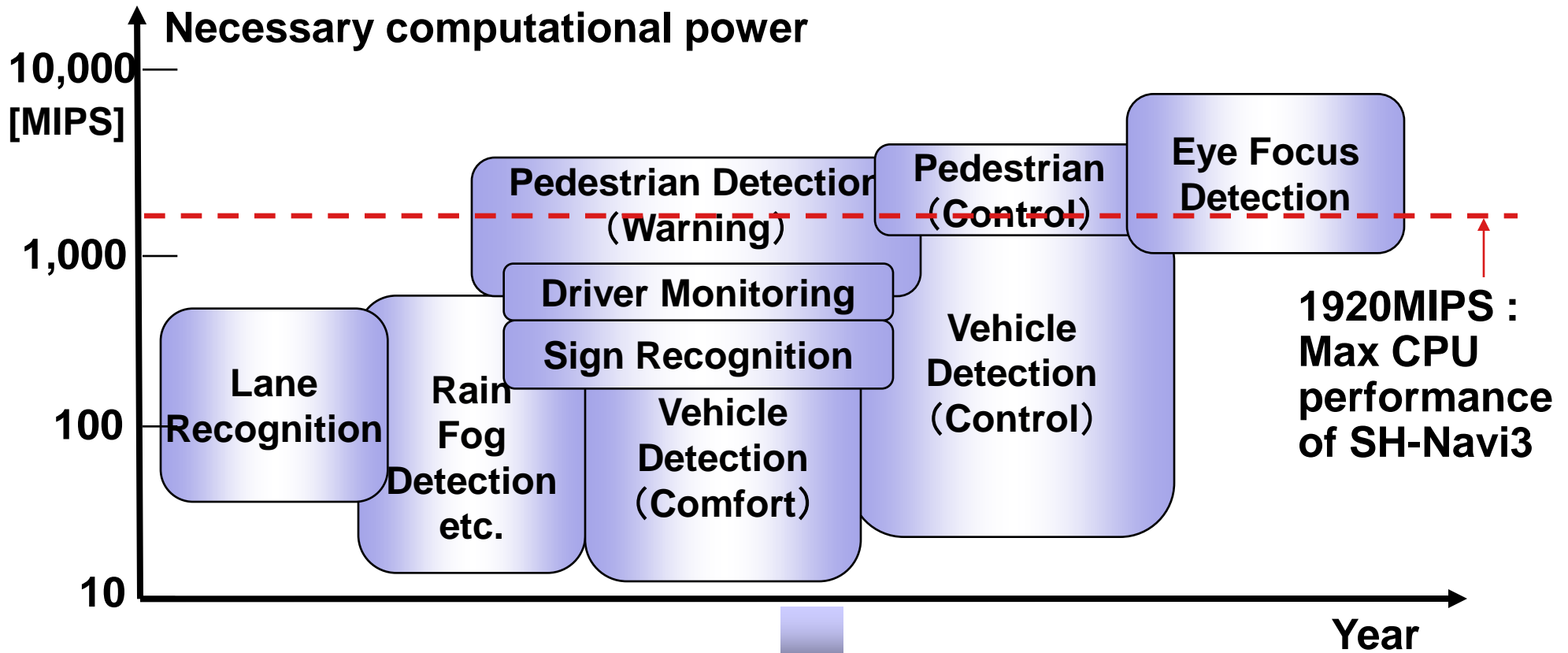
changing view point with distortion correction

**These applications have to be processed in real-time**



# 1-Chip Solution's Problem with Image Recognition

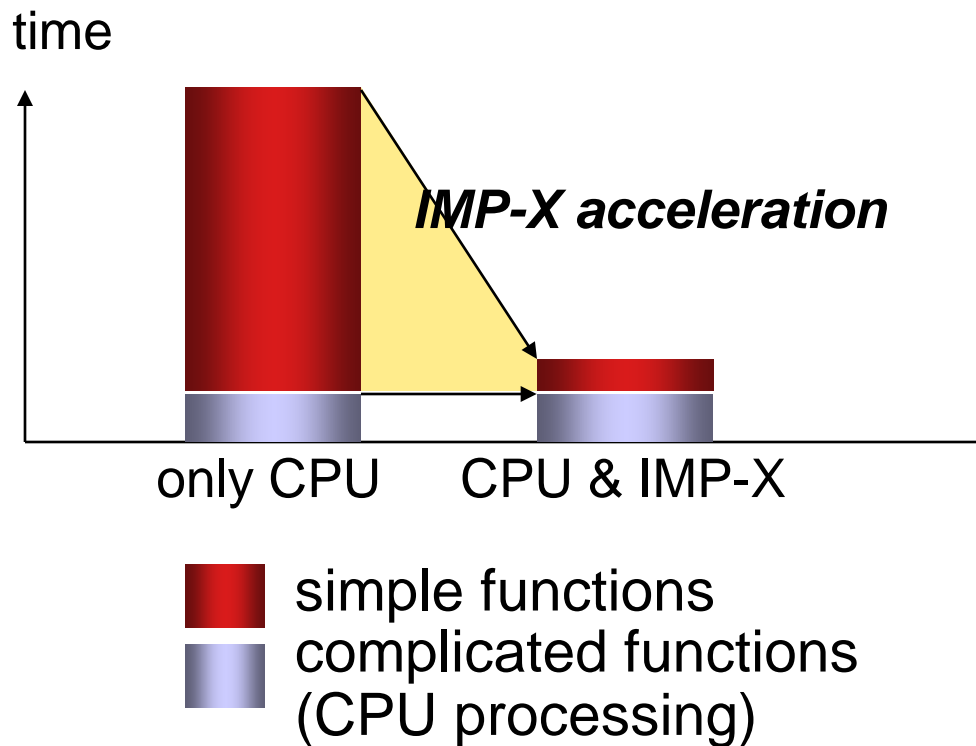
- Real time application with image recognition consumes a lot of computational power



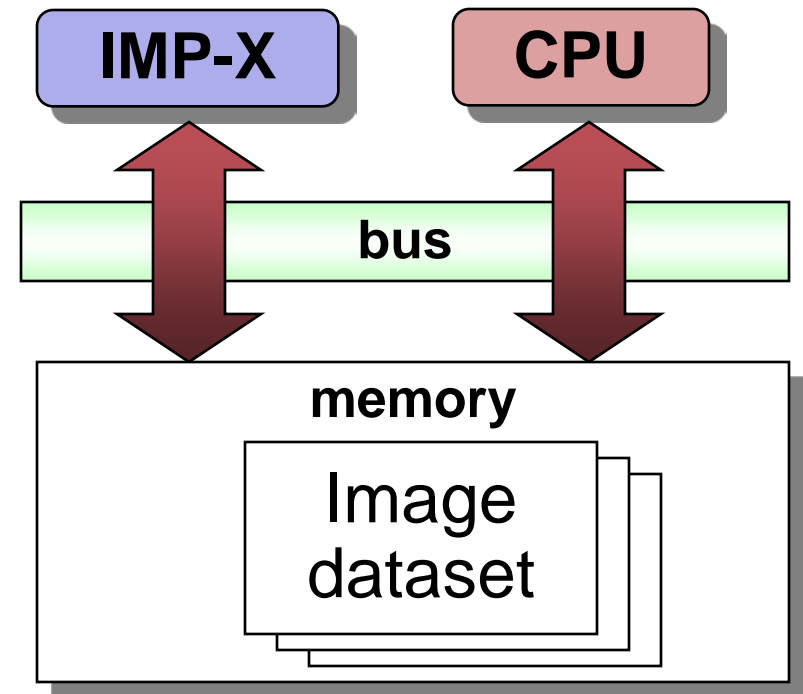
**Solution : Embedded Image recognition accelerator (IMP-X)**

# Concepts of Image Recognition Accelerator (IMP-X)

- IMP-X accelerates frequency-used and simple functions
- CPU calculates the others or complicated functions
- IMP-X & CPU access same image memory region with same distance

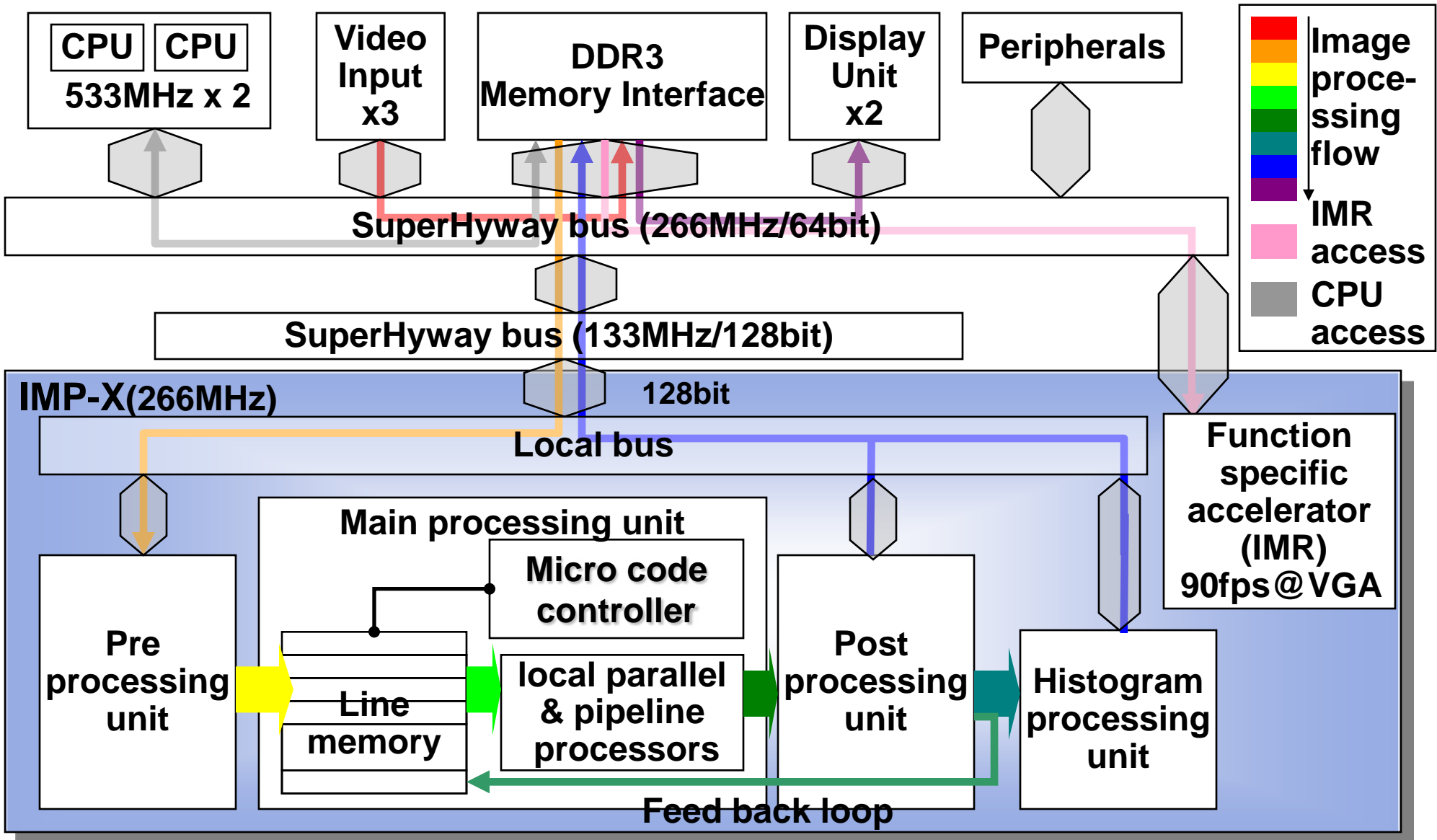


Process time distribution of image recognition application



Relationship of between IMP-X, CPU, bus, and image memory region

# Process Flow of Image Recognition



## ■ For High-speed processing

- Various image functions  
- up to 53.3 GOPS



- Local parallel processing
- Pipeline processing

- Distortion correct,  
changing view point



- Function specific  
accelerator (IMR)

## ■ For Integration into SoC

## ■ For Versatile processing



- Compact Architecture
- PIPE (Programmable  
Image Processing  
Extensions)

## What functions does IMP-X accelerate ?

- Image Affine Transformation
- Pixel Transformation
- Inter Pixel Arithmetic Calculations
- Inter Pixel Logical Calculations
- Binary Image Shape Transformation
- Convolution → **0.66ms@VGA**

- Minimum/Maximum Filter
- Rank Filter
- Labeling
- Gray Scale Image Characteristics
- Binary Image Characteristic Extraction → **1.18ms@VGA**

- Memory Access
- Binary Pipeline Filter
- Pipeline Control
- YUV Color Processing
- Binary Matching Filter
- Optical flow
- Template Matching  
(SAD, Normalized Correlation etc)
- Matrix operation
- FFT
- etc...

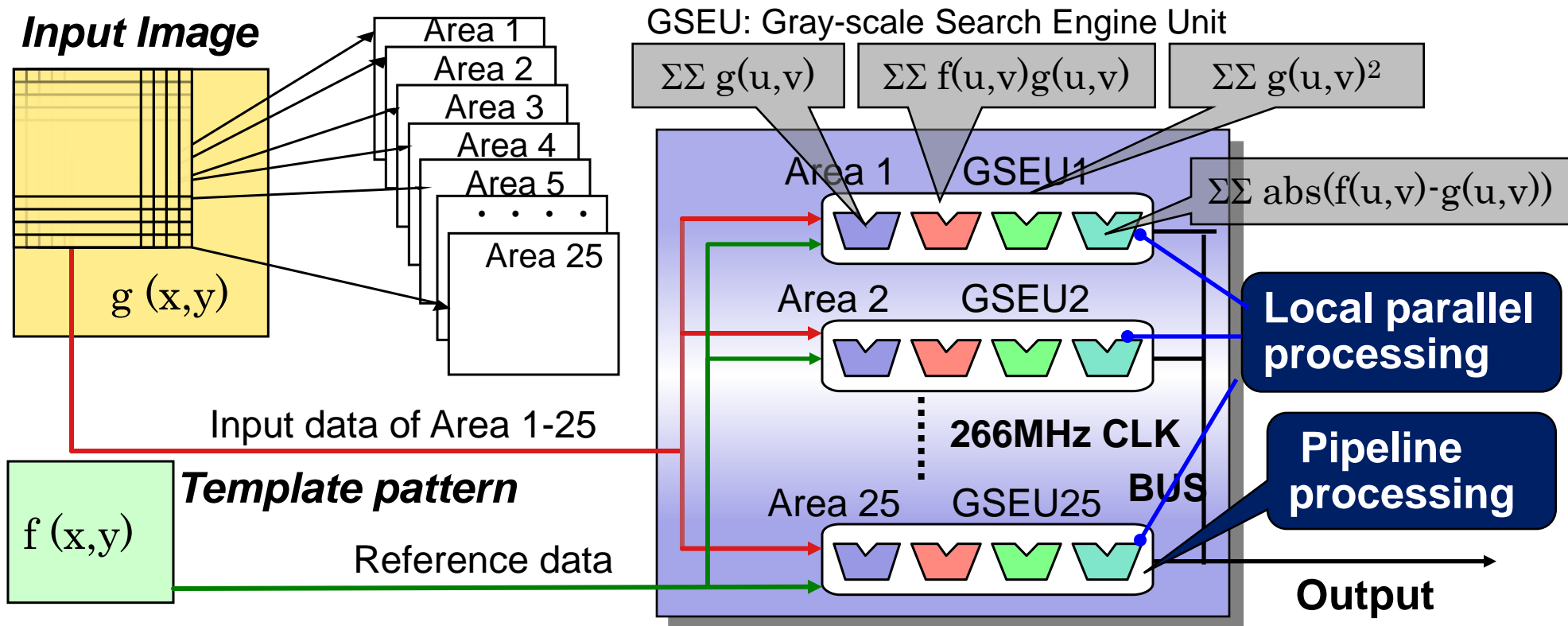
Normalized correlation  
is operated at **53.3 GOPS**  
(Max performance of IMP-X)

# For High-speed Processing : Template Matching

- Calculate similarity between template pattern( $f$ ) and part of image( $g$ )

**Normalized Correlation** = 
$$\frac{\sum \sum (f(x, y) - \bar{f})(g(x, y) - \bar{g})}{\sqrt{\sum \sum (f(x, y) - \bar{f})^2} \times \sqrt{\sum \sum (g(x, y) - \bar{g})^2}}$$

- Total Processing: (1+2+2+3) Operations \* 25 GSEUs \* 266 MHz = **53.3GOPS**

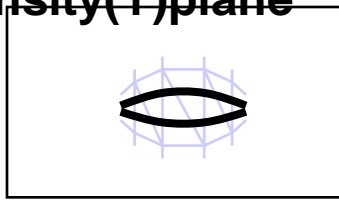


# For High-speed Processing : Distortion Correction

- Generating image pattern for distortion correction, rotation, zoom out/in
  - Control by flexible triangle mesh with vertex data set
- YUV image format (combination/independent), Gray-scale format (8bpp)
- Hi-Speed drawing engine at **90fps with VGA**

Raw image from camera

Intensity(Y)plane



Color(UV)plane

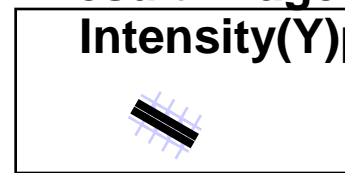


Rotation,  
Zoom-Out

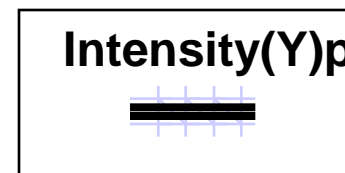
Distortion  
Correction

Result image

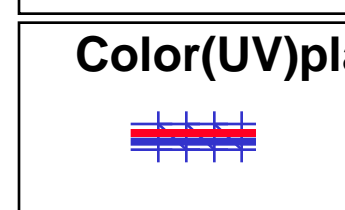
Intensity(Y)plane



Intensity(Y)plane



Color(UV)plane



Function specific  
accelerator (IMR)

Image  
Recognition

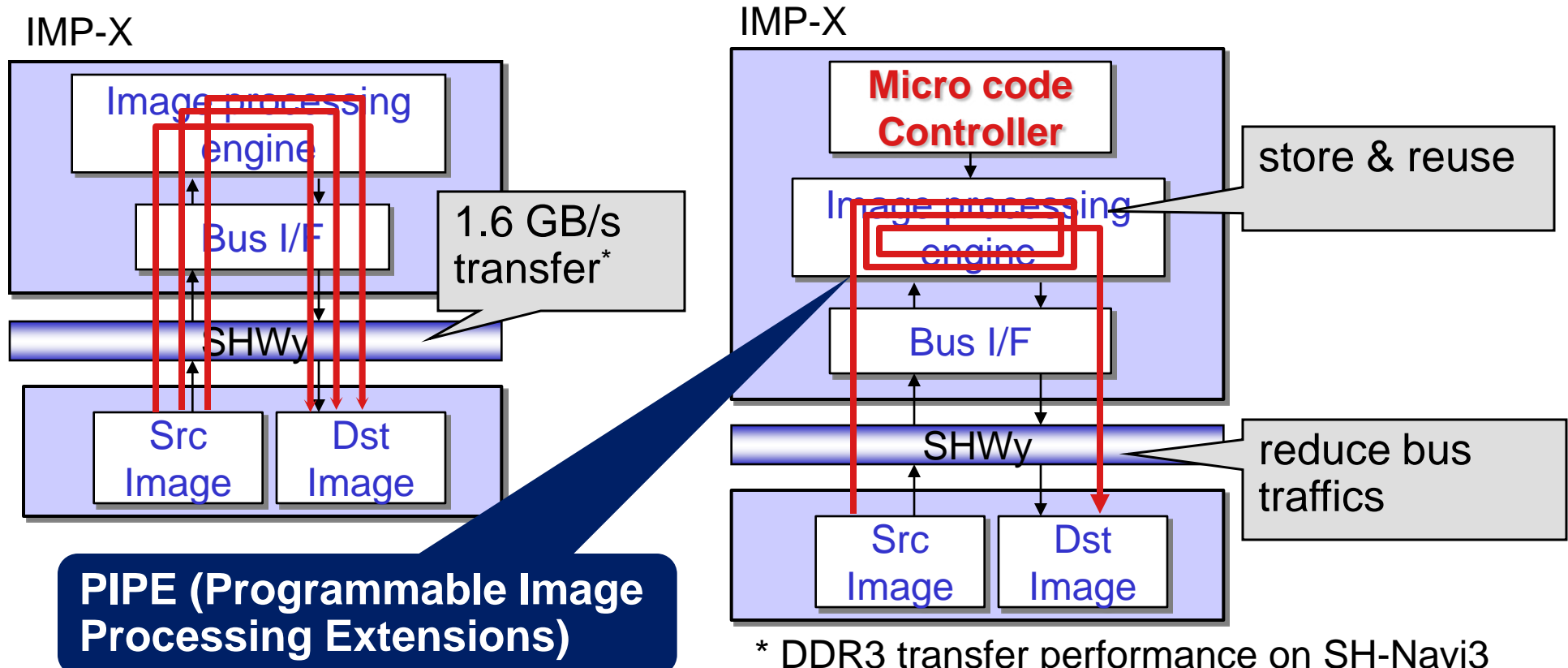
Color Graphic



# For Integration into SoC and Versatile Processing

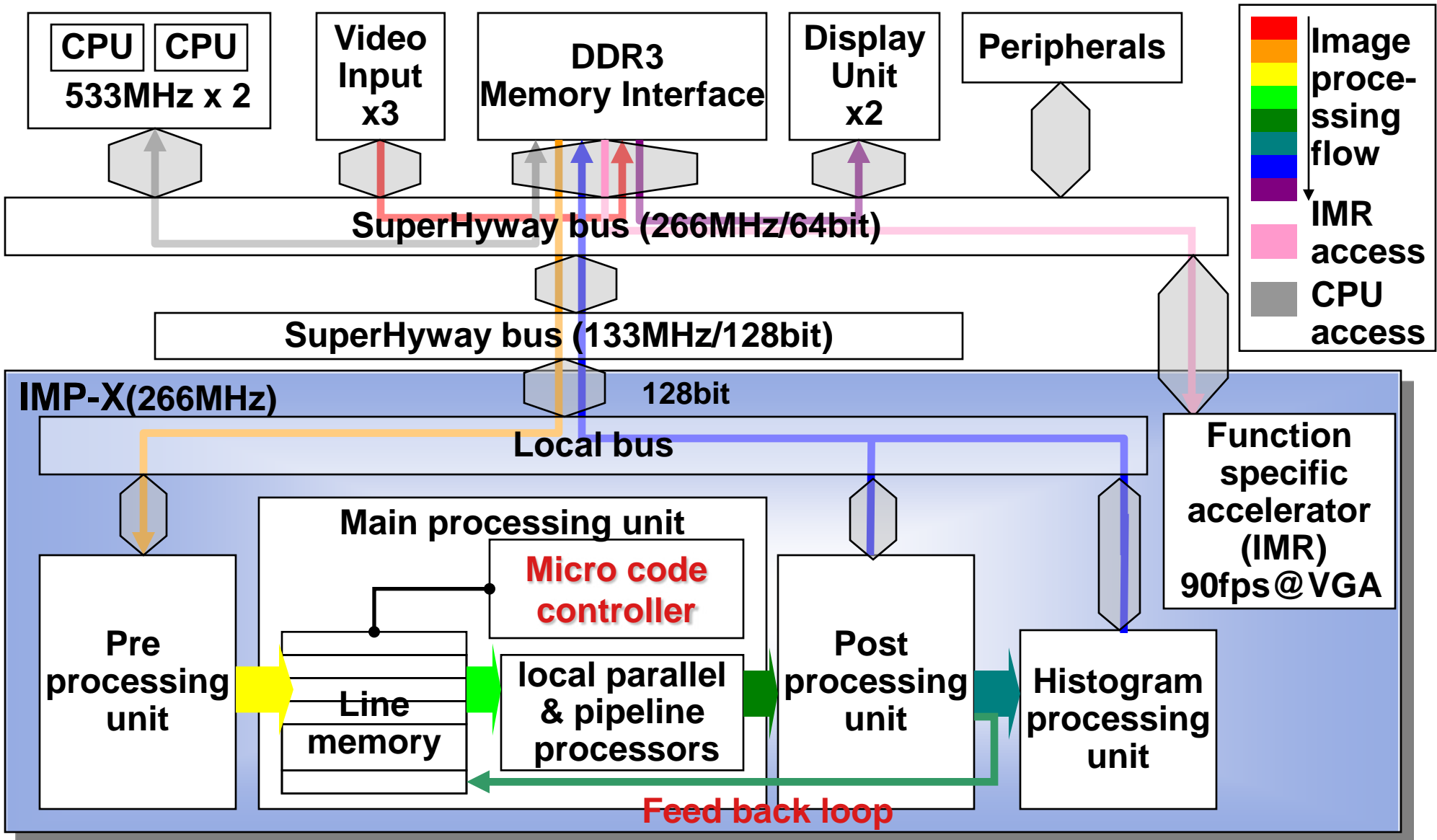
- **Programmable processing** at each line with micro-code control
- **Reducing data traffic** between IMP-X and memory by store and reuse of processed data in IMP-X

## Comparison of 3 image-functions behavior between non-PIPE and PIPE



\* DDR3 transfer performance on SH-Navi3  
: up to 4.27GB/s

# Process Flow of Image Recognition



# Evaluation for Bus traffic reduction

## Harris corner detector requires 14 functions

$$H = \begin{bmatrix} \sum I_x^2 & \sum I_x I_y \\ \sum I_x I_y & \sum I_y^2 \end{bmatrix} = \begin{bmatrix} a & b \\ b & c \end{bmatrix}$$

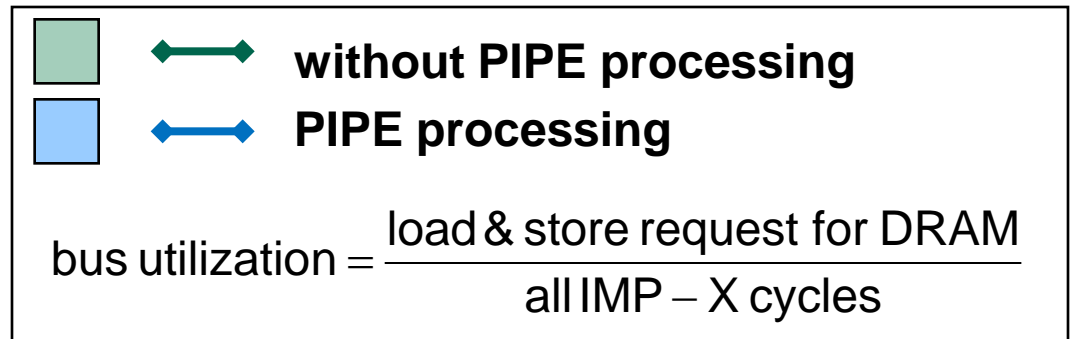
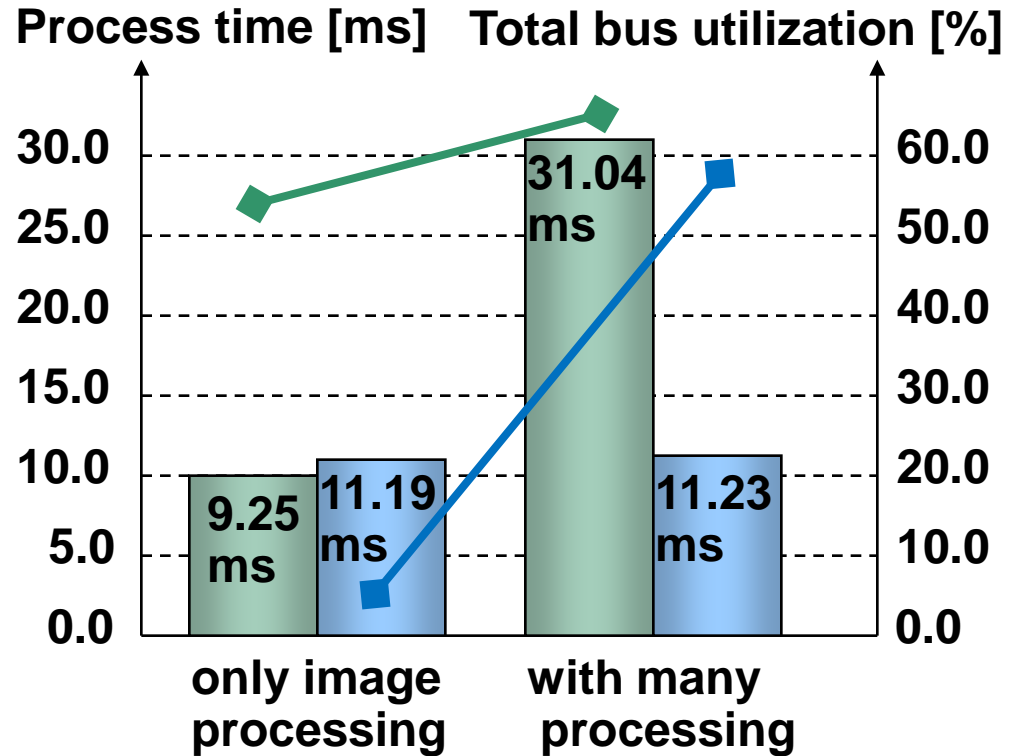
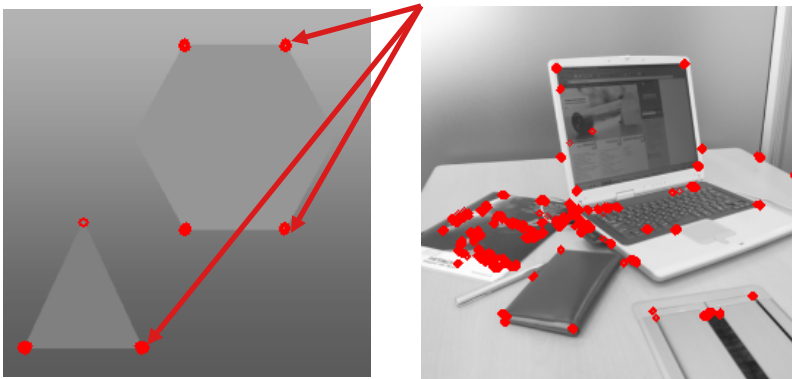
where  $I_x = \frac{\partial I}{\partial x}$ ,  $I_y = \frac{\partial I}{\partial y}$

$$\det(H) = ac - b^2$$

$$\text{Trace}(H) = a + c$$

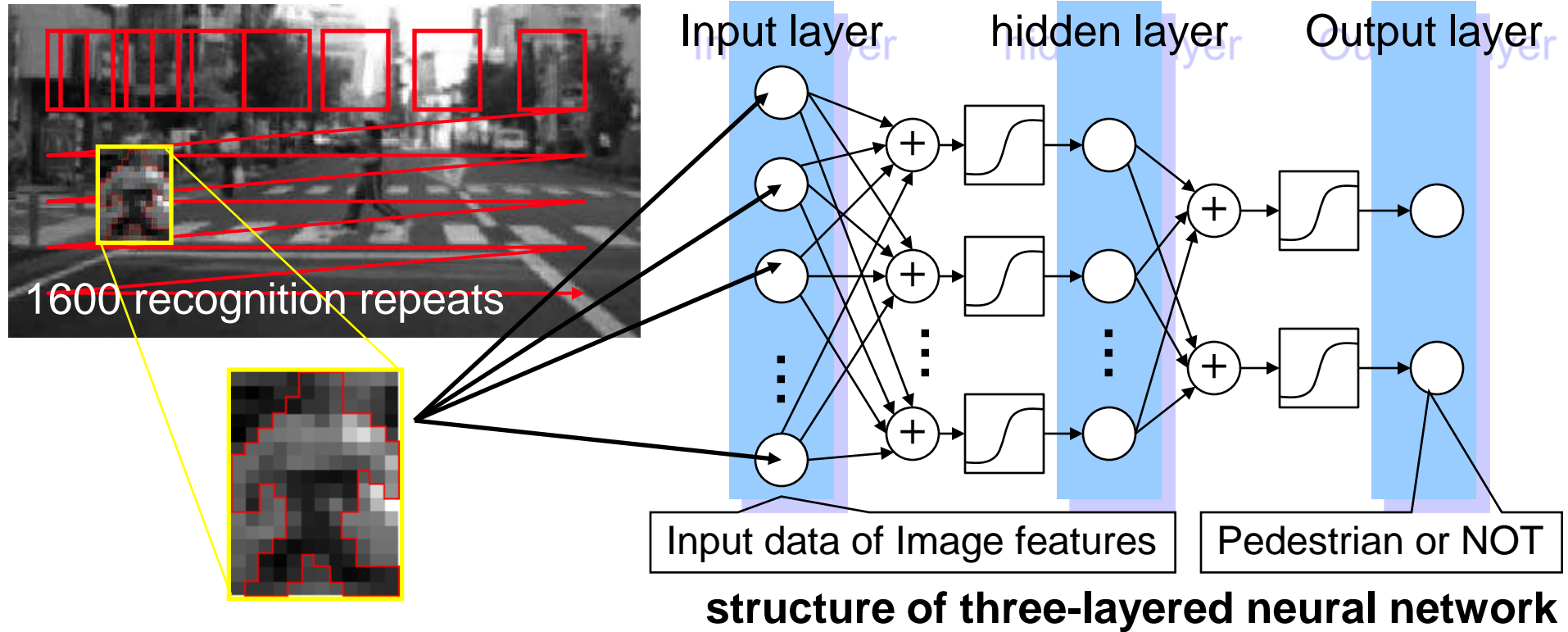
$$R = \det(H) - k\text{Trace}(H)^2$$

### Corner



# Practical Application : Pedestrian Detection with Neural Network

- Pedestrian Detection is one of the important applications for safety system
- Three-layered neural network is used for recognizing pedestrian pattern

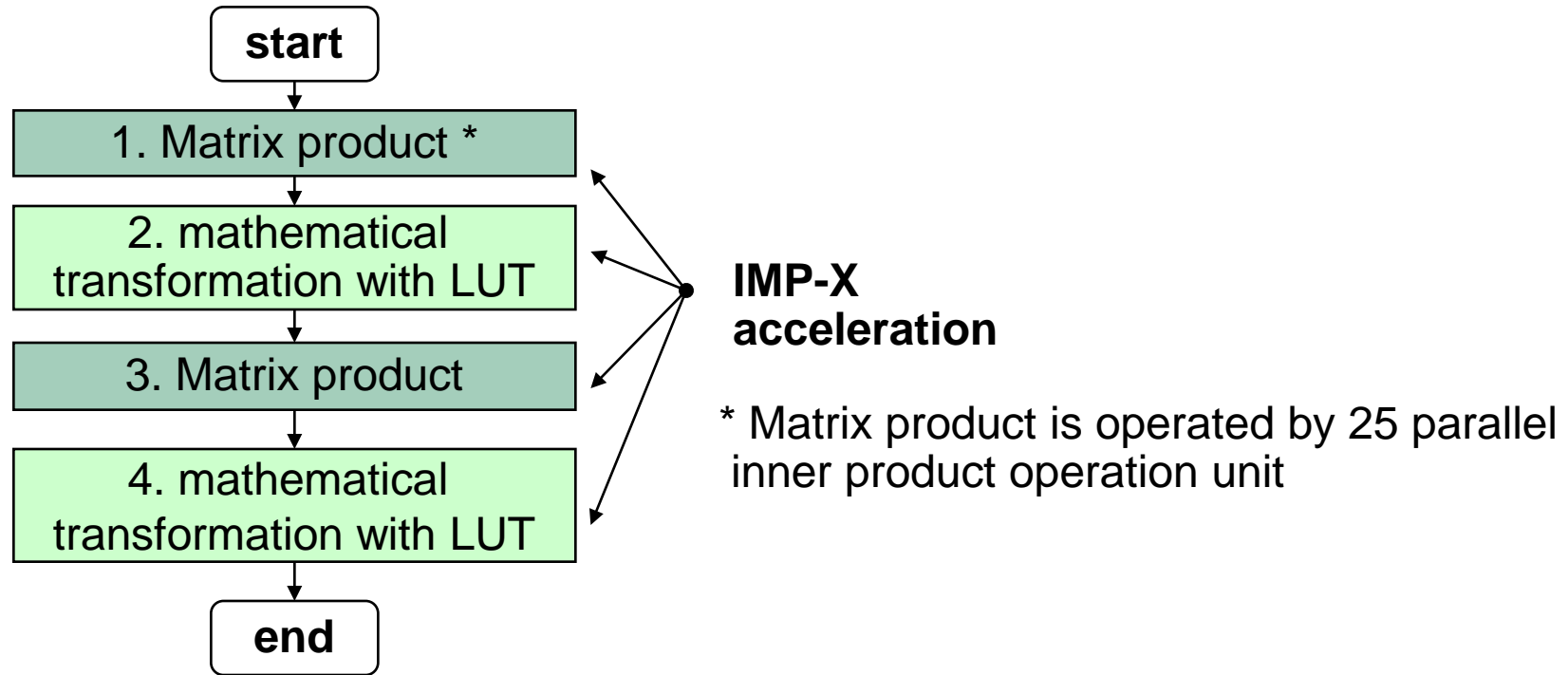


With CPU ...

- 1600 times of neural network processing time : **204ms**
- Total pedestrian detection application processing time : **233 ms**

# Practical Application : Acceleration of Neural Network

- The neural network consists of two **matrix product operation** stages (1,3) and several **mathematical transformation** stages (2, 4).



With IMP-X ...

- 1600 times of neural network processing time : **204ms** → **8.9 ms**
- Total pedestrian detection application processing time : **233 ms** → **29.4 ms**

## SH-Navi3 embeds

- High performance dual RISC processors (1920 MIPS)
- 2D/3D graphic accelerators
- Image recognition engine
  - High-speed processing (up to 53.3GOPS) :  
parallel processing + pipeline architecture + function specific accelerator
  - Bus traffic reduction & Line programmability :  
PIPE architecture



**Achieves a 1-Chip solution  
for Next-Generation  
Car Navigation Systems**



**HITACHI**  
Inspire the Next

**RENESAS**