



Technology scaling at an inflection point

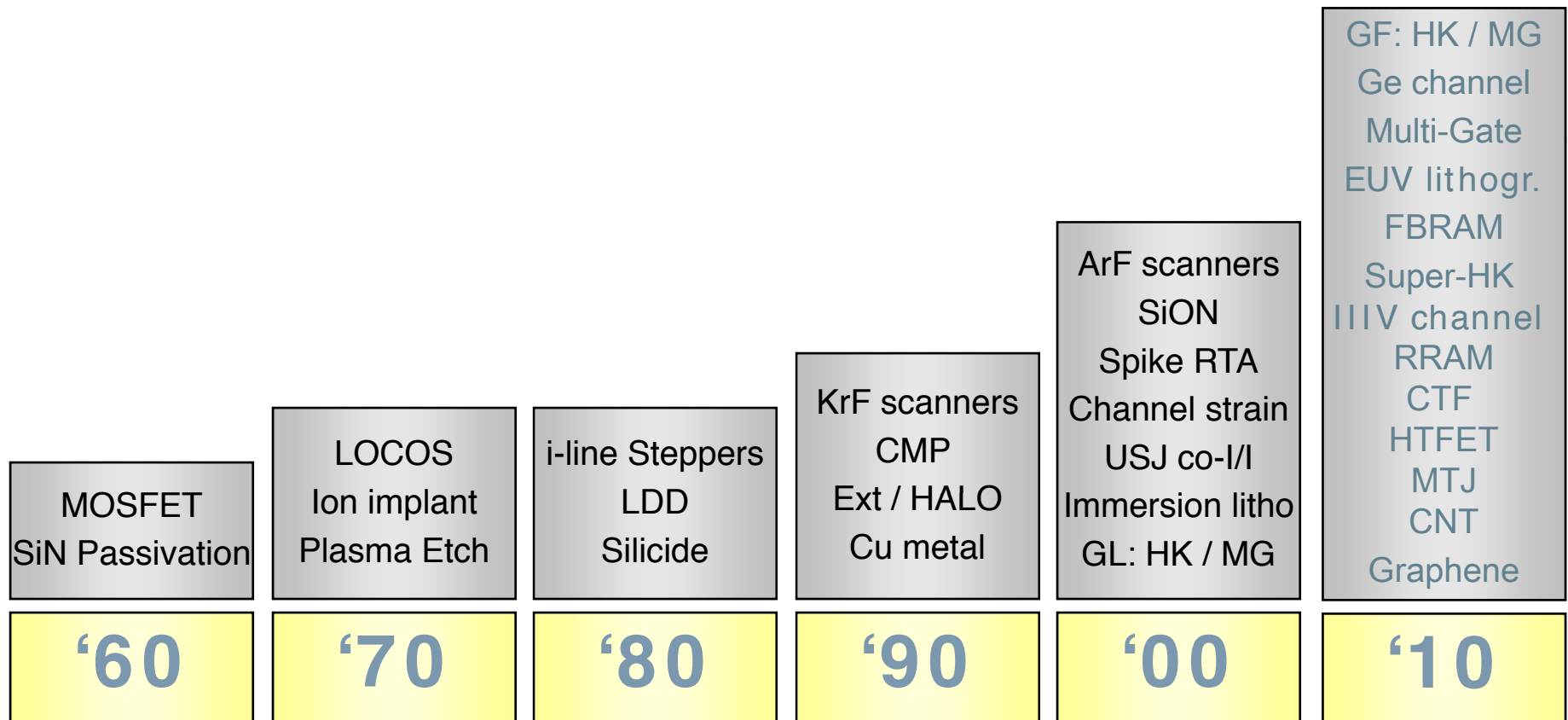
WHAT'S NEXT?

Lode Lauwers, IMEC

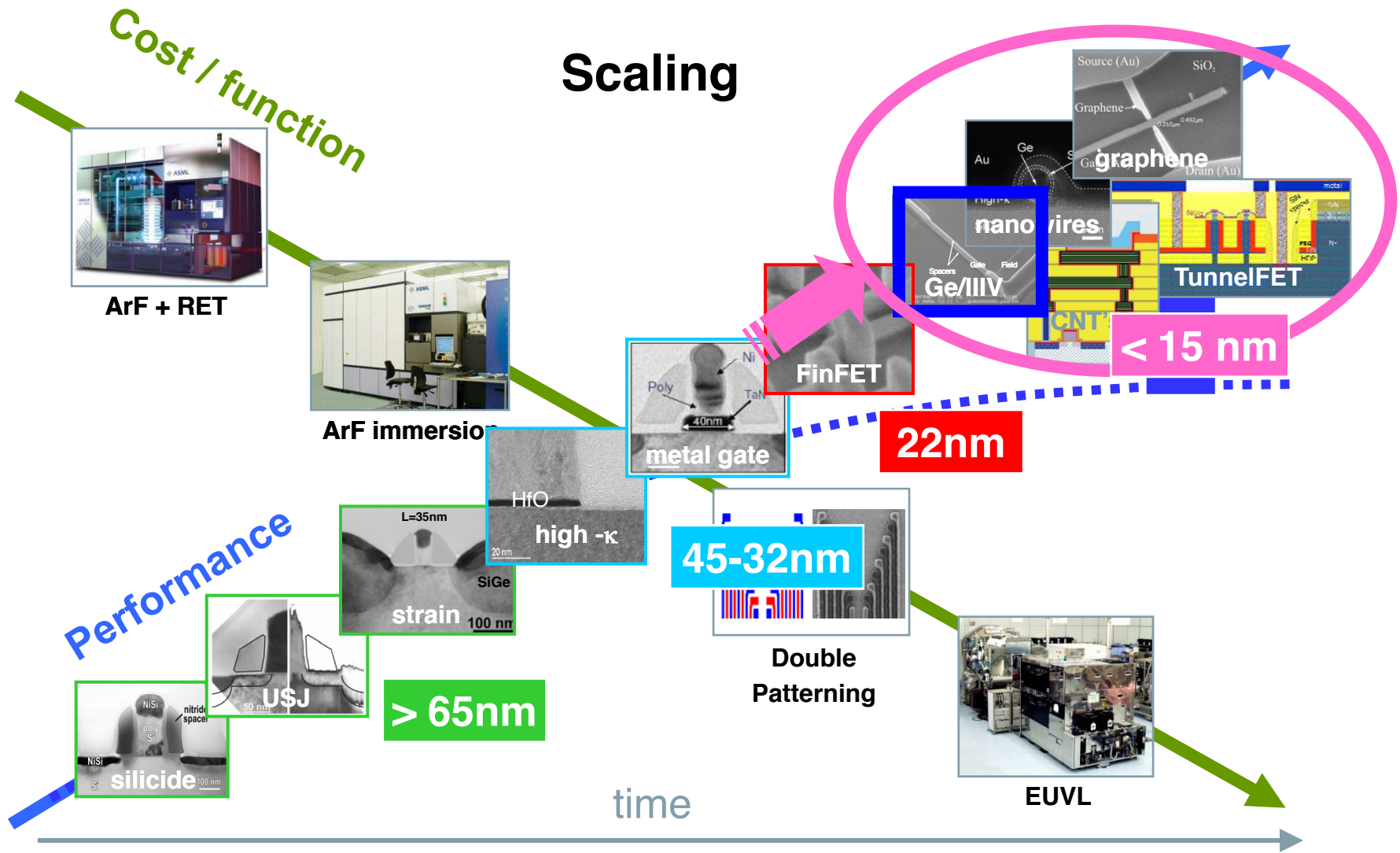


Research challenges

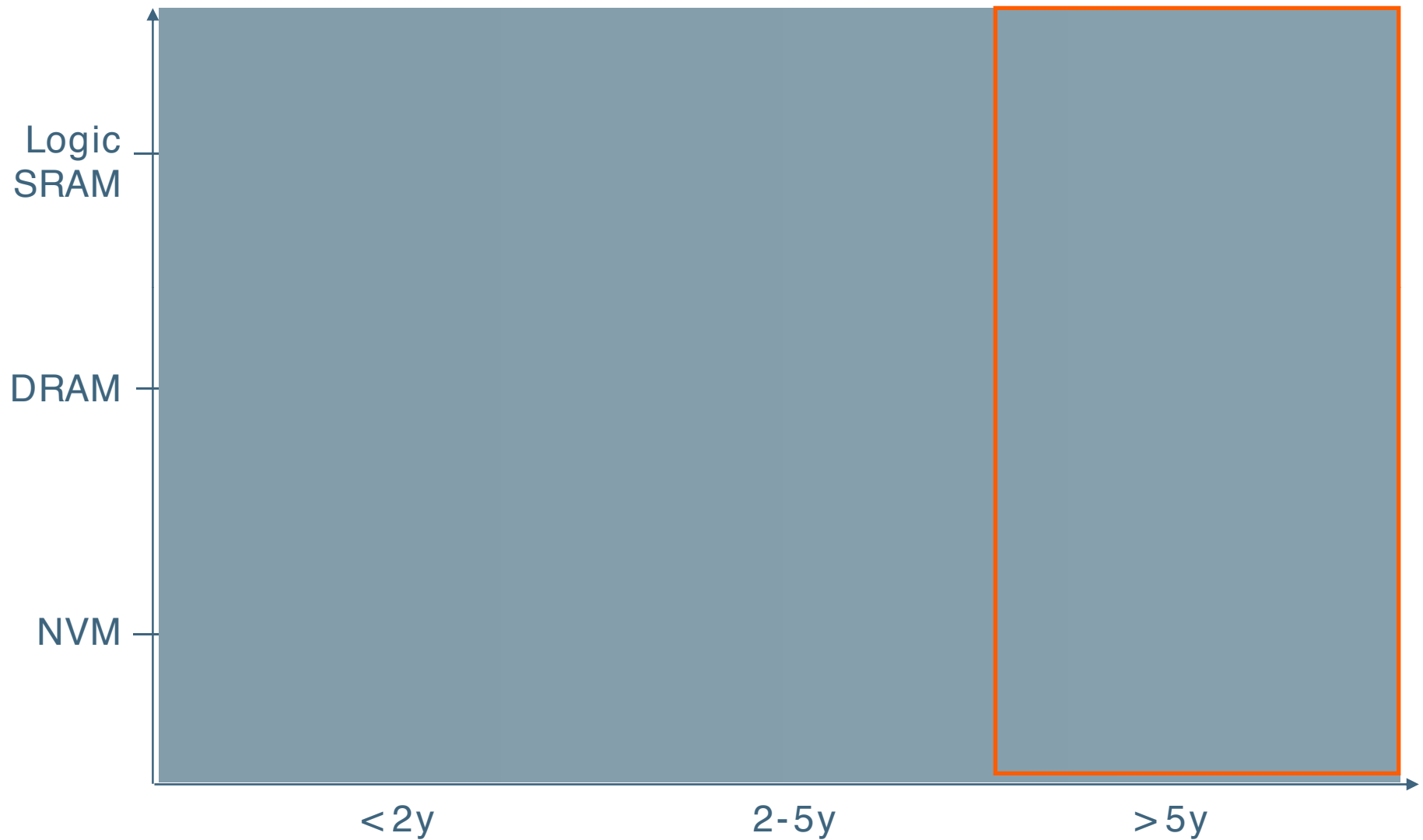
Technology complexity increases



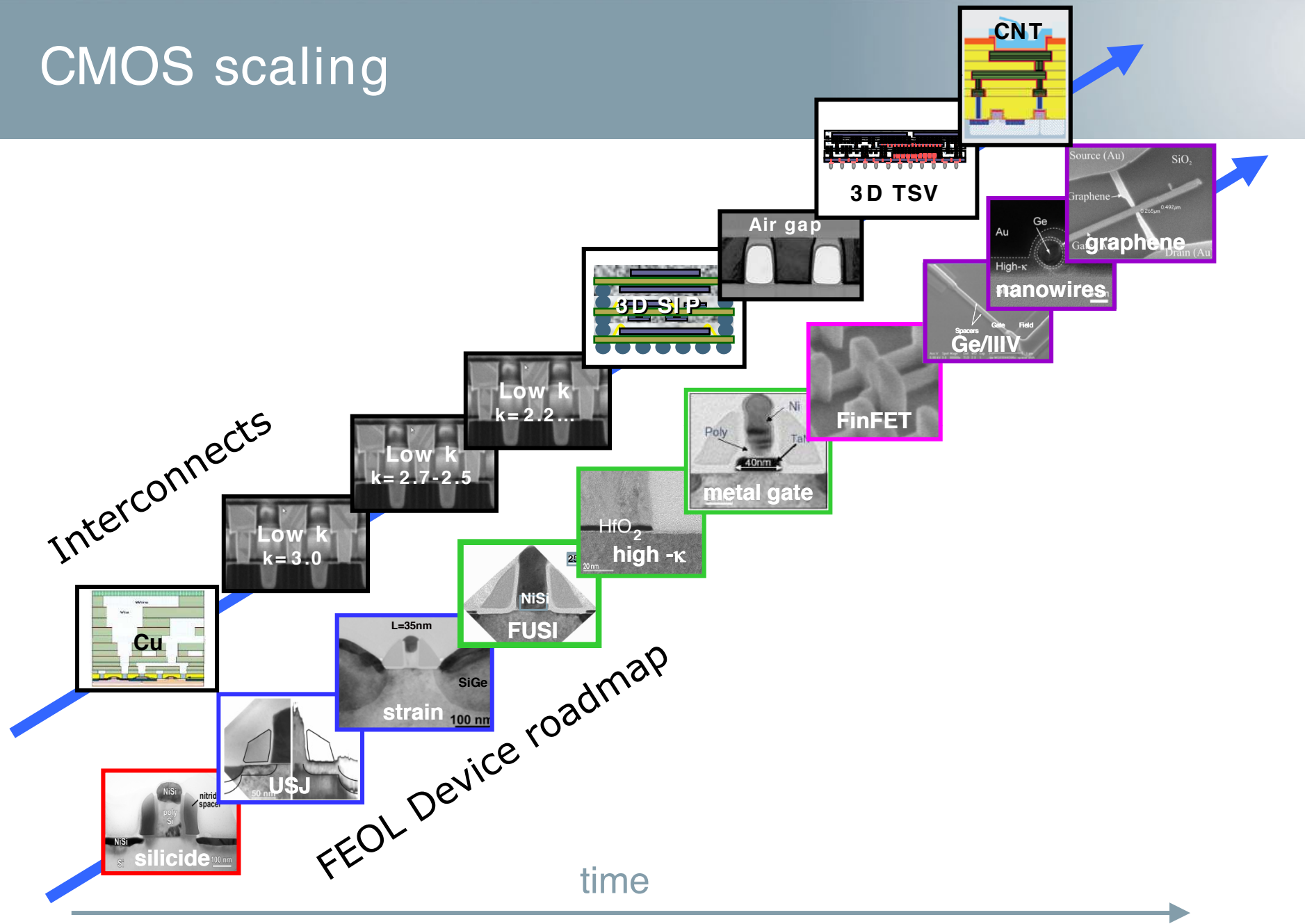
CMOS scaling roadmap



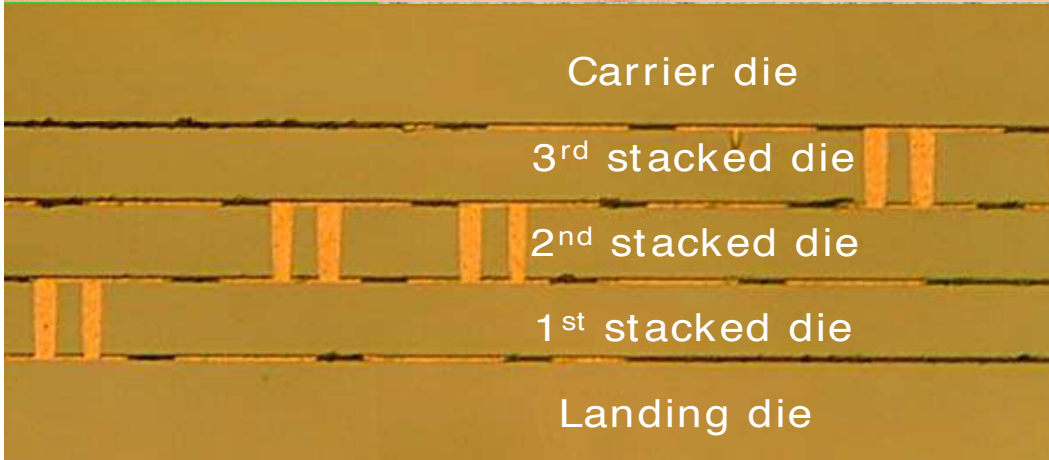
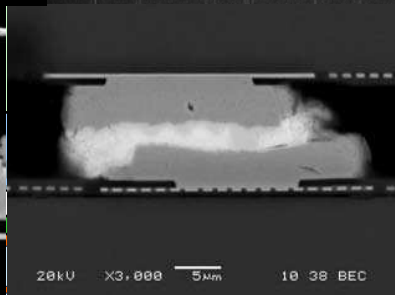
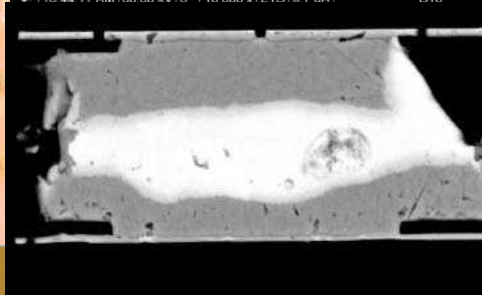
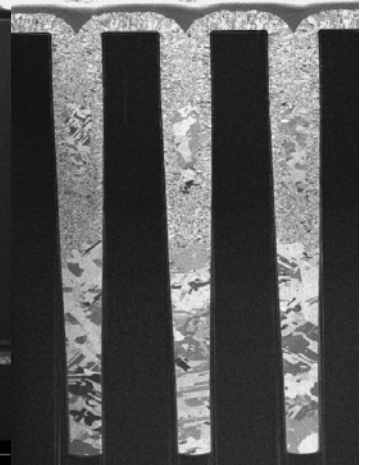
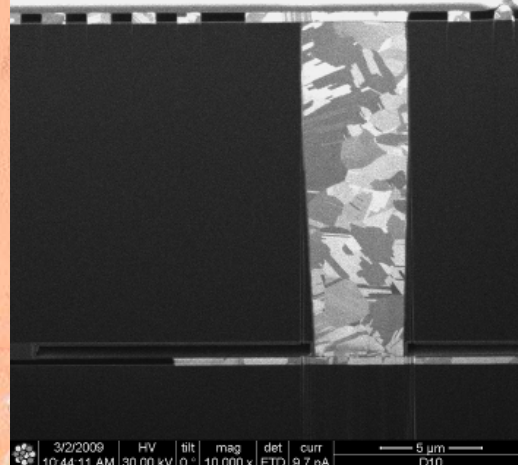
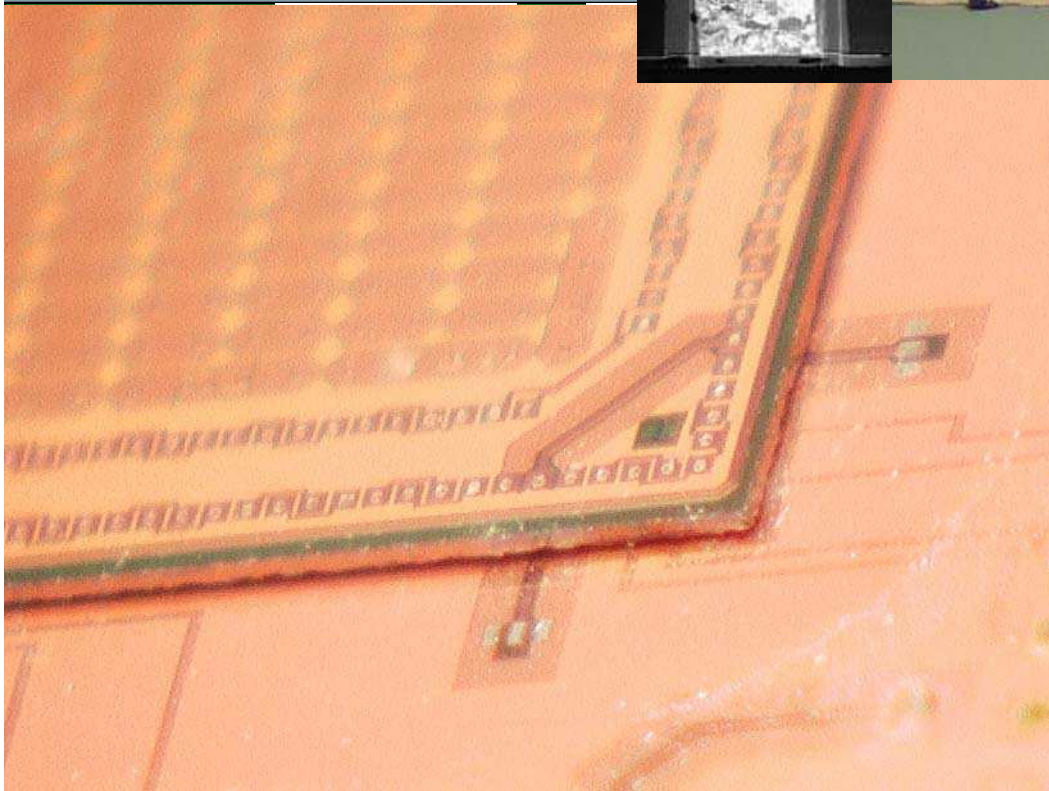
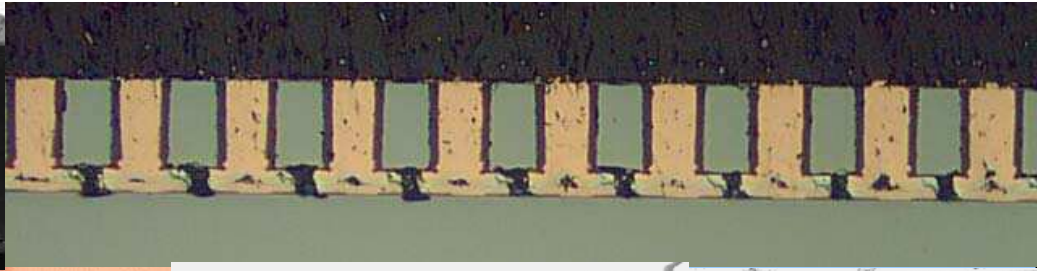
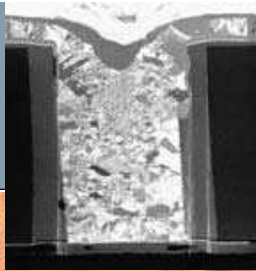
IMEC FEOL Research Topics & Roadmap



CMOS scaling



3D @ IMEC



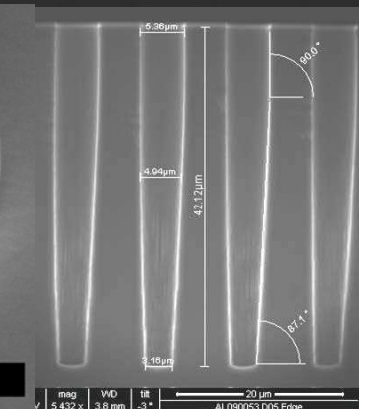
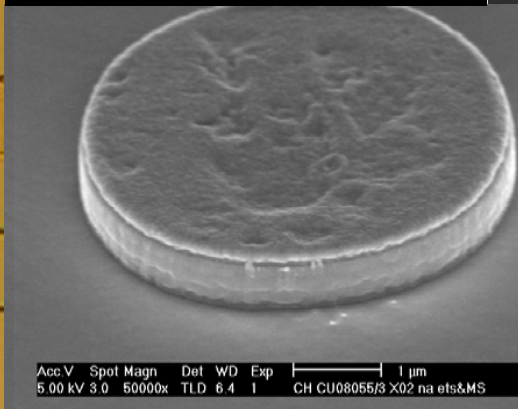
Carrier die

3rd stacked die

2nd stacked die

1st stacked die

Landing die

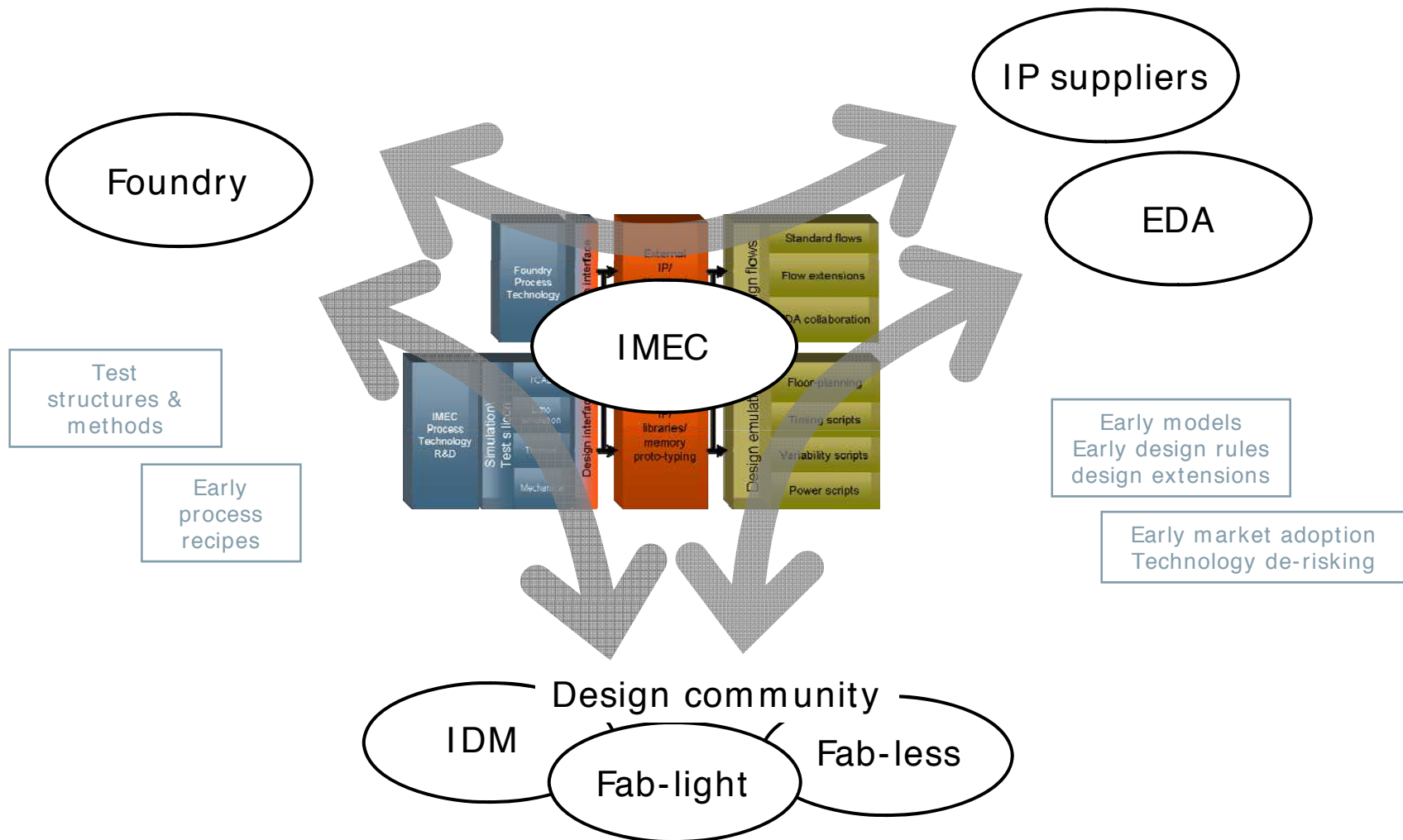


Acc V Spot Magn Det WD Exp | 1 μm
5.00 kV 3.0 50000x TLD 6.4 1 CH CU08055/3 X02 na els&MS

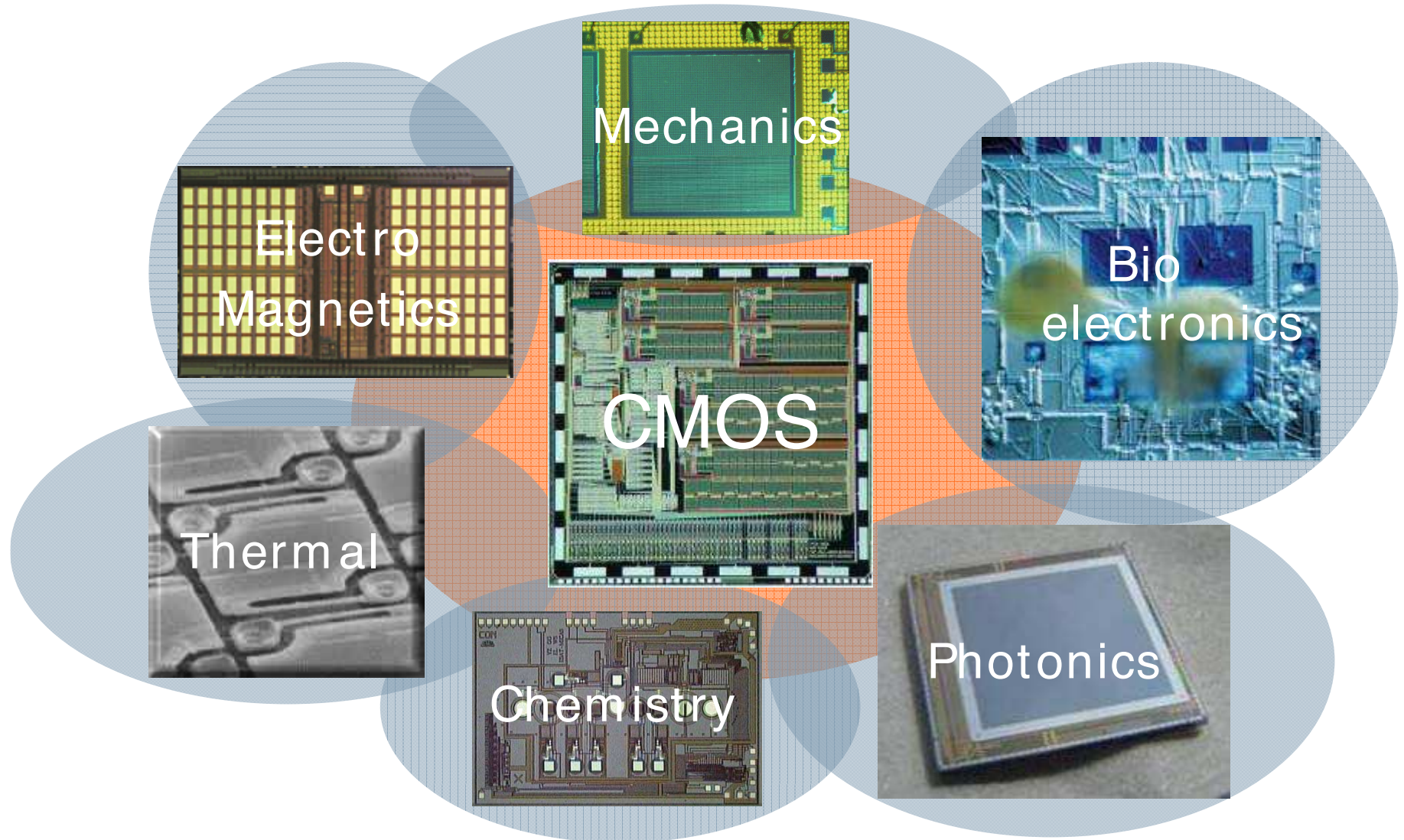
mag VID tilt | 20 μm
5.432 x 3.8 mm -3° AL090053 D05 Edge

Growing interest in ECO-system

(with dedicated "INSITE" program for system houses)



Technology options on advanced CMOS: sensors & actuators, connectivity...





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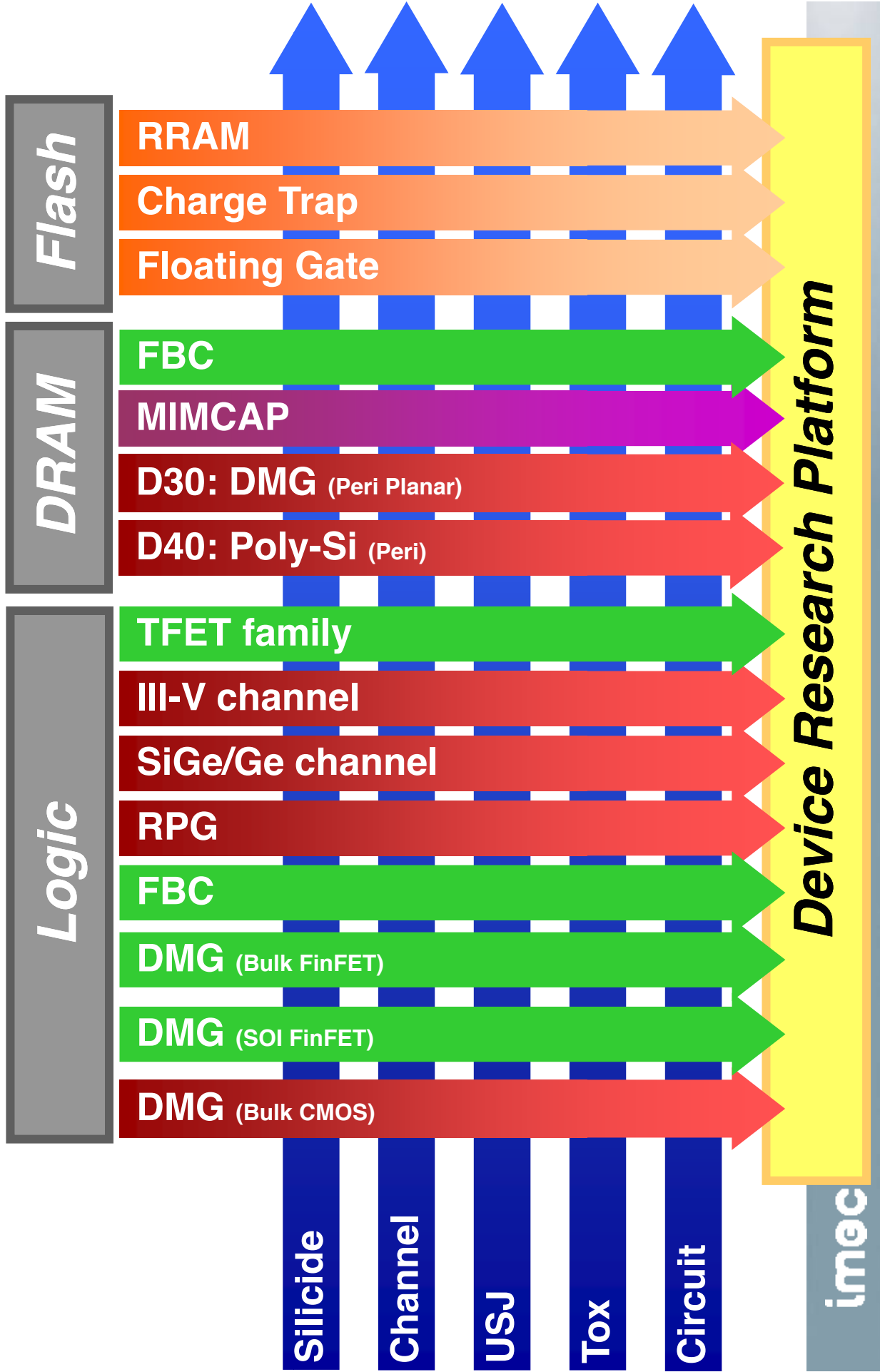
Years of Making
Technology Fly

200/300mm Pilot Line

Routes optimized for:

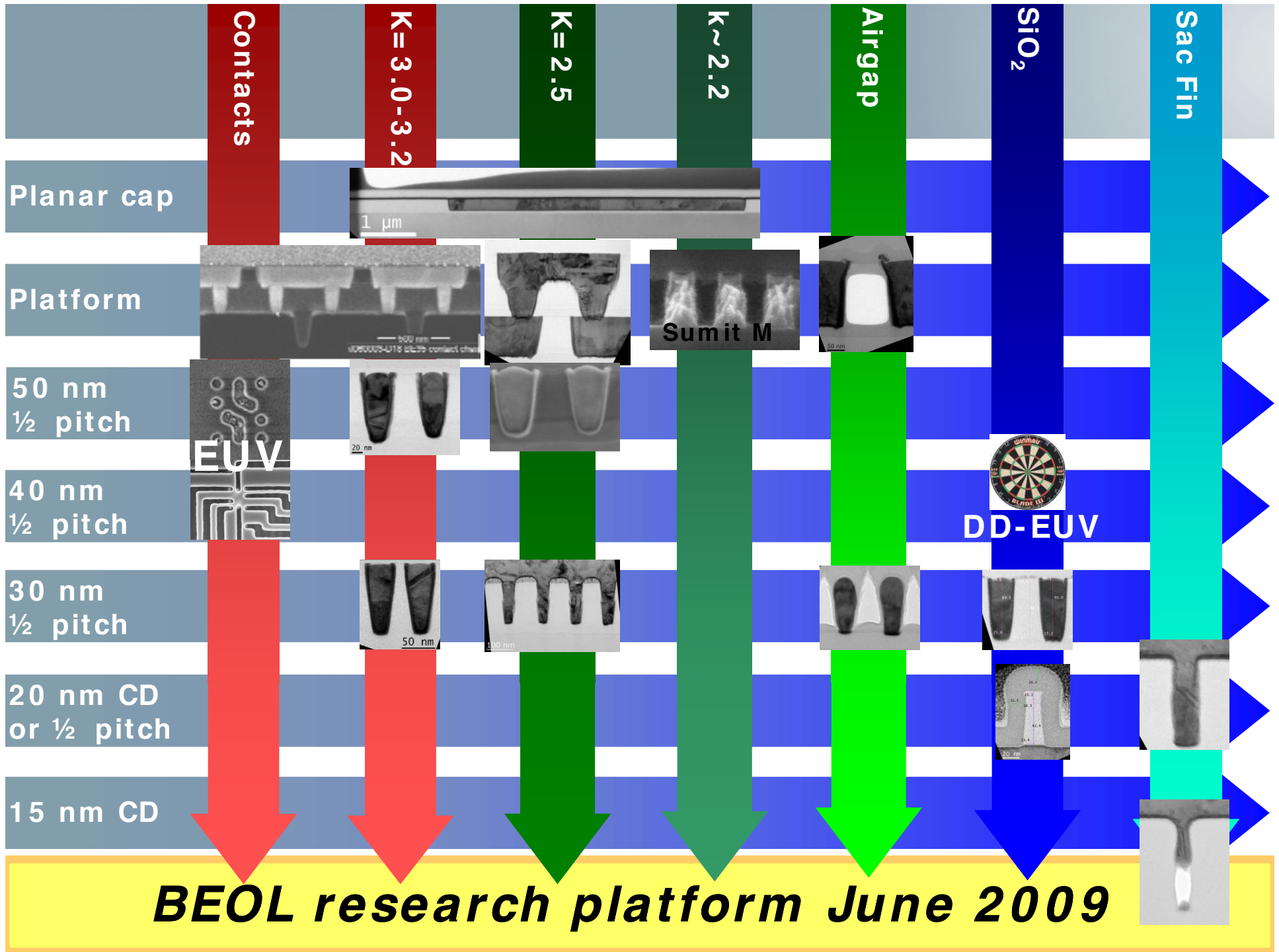
- Flexibility (materials, devices)
- Cycle time
- Quality of Processing

FEOL Device Strategy Map



Device Research Platform

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Increasing link Technology-design

