OMAP4430 Architecture and Development

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OMAP 4430

- Requirements and challenges of building a "class of 2009" application processor
- What did we want to build?
- How did we build it?
- How does it fit in a system?
- Summary/Questions..



Application processor – class of 2009

- Process Technology
 - 45nm LP 7LM with a very thick top layer -
 - See next couple of foils of challenges with application processors..
- Package technology
 - 12mm x 12mm 0.4mm pitch BGA flip-chip with POP flash/DRAM -
- Memory technology
 - LPDDR2 400MHz
- Power/performance/Area/Schedule
 - 600mW to 100uW max to min..
 - 1Ghz 2p A9 processors with 1MBL2 + lots of other multi-media accelerators and high speed peripherals..
 - As small as possible and/or it had better fit in the package
 - It is 2009 so it is "imminent"



BOILER PLATE – Advanced Process and Leakage



UMIENTIS

BOILER PLATE – We are not just digital guys anymore





What did we want to build and why ?

- Processors and memory
 - Highest possible performance with SMP ARM Processors
 - Distributed processing and control Gstreamer/OPENMAX
 - High speed memory optimized for bandwidth and Latency
- Multi-media
 - Best in class Image/video/display
 - 2D/3D graphics with vertex shading
 - Flexible/low power audio 100 hour playback++
- Interconnect and Peripherals and Protection
 - High performance/flexible interconnect
 - Multiple standard parallel/serial interfaces
 - Flexible method to allow sharing memory and peripherals with different external modems and accelerators
 - Trust zone, Secure RAM/ROM, firewalls, crypto accelerators with secure DMA
- S/W and H/W mechanisms that enable only blocks that need to be powered to be powered for key use cases..
 - le be best in class in everything we run between 600MW and 100uW..
 - At the system level not just the OMAP level..
- All of this to enable a wide variety of applications to be always on always connected and that will fit in your pocket...



Processors

- Highest performance processor + L2 + memory system
 - 2p Cortex A9 core 32KBi/32KBD
 - 1MB L2 cache
 - 1GHz+ max clock
- Real time task offload processors
 - 2p cortex M3 @ 200MHz with unified cache/backing SRAM
 - Fast L2 reload 3 cycles on miss
 - Offloading image/display/video codecs
 - Fast real time response not subject to main processor HLOS overhead and task switch latency
- General purpose DSP processor
 - 64x-lite DSP @ 466Mhz with 32KB L1 / 128KB L2
 - Fast L2 reload 5 cycles on miss
 - General purpose pre and post processing task
 - Low power audio codec
 - Large enough L2 to prevent flash/DRAM access in low power mode



Memory system and backplane

- 2x LPDDR2 for OMAP4430
- 400MHz operating frequency
 - i.e. OMAP4430 SDRAM BW budget ~5x OMAP3430
 - 2 x32 channels map to 200Mhz 128 bits OCP 2.2 interconnect..
 - Image, video and display IPs are 2D aware
- 2x-LPDDR2 mapped as 2 interleaved channels for OMAP4
 - Transparent for both SW and HW modules
 - Direct path from processor cluster to memory controllers
- Powerful DRAM Memory Manager (DMM) for BW optimization
 - 2D-Tiling Rotation Interleaving Virtual memory management for all HW operators



Multimedia – image and display

- Image engine
 - Internal proprietary HW/SW/Accelerators mix
 - Enables 200Mpixels/second raw data rate
 - 1000 plus operations/pixel at that data rate..
 - Multiple different camera inputs
 - Usual suspects
 - Defect Pixel correction/Lens distortion correction
 - Gamma correction/color filter adapter/color space conversion
 - Noise filters / Resizers
 - Optimized path 2D path to/from LPDDR2 frame buffer
- Display engine
 - Multiple parallel video and 3D graphics paths
 - Horizontal/vertical filters
 - Programmable overlaps/alpha blending/color space conversion with hardware rotation
 - Optional "snapshot" path to capture and feedback blended images
 - Primary/secondary DSI outputs + HDMI
 - Very low power modes with intelligent display fetch...



OMAP4 image/display HW/SW paths..





Low power audio

- Leverage flexibility of existing ARM/DSP codecs
- Minimize everything that needs to be on for MP3 playback
 - Chip wide Only 1 DPLL active [out of 10..]
 - Chip wide only 1 power domain always on [out of many..]
 - Minimize ARM/DSP on time so they are 95% off
 - Build one programmable mixer/buffer for final stage to I/O
 - Optimize all I/O to/from this one small block
 - Optimize external drive/power amplifier to speakers.
- Results on MP3..
 - Battery level for 1000mamp-hr = 100 hours of playback



HW/SW power/use case example

- Different voltage domains
 - Blue/orange/yellow
- Different clocks/power
 - Blocks called out
- Unique connections
 - Wires optimized
 - Master/slave protocol
- Use case
 - Given at "application level
 - Can be SW or HW or mixed control..
 - Blocks can "watch for activity" a in absence remove power/clock and wait..
 - Optimization -
 - Shut anything off not needed
 - Balance wakeup time to off time
 - Application must tell O/S
 - O/S tells middleware and HW/SW



Example say

- 1 capture image/compress display
- 2 Listen to MP3 while doing above
- 3 minimize power unless wakeup..



Efficient Chip2Chip communication

- External modems
 - Need low latency path to memory
 - Expensive to replicate entire memory
 - Expensive modem+apps chip
 - Modems and apps move at different rates
- Solution
 - Use LPDDR2 signaling
 - Dedicated links to/from
 - Direct path to LPDDR2
 - Access with protection to all other blocks
 - Side by side placement
 - As efficient as larger package





OMAP4430 Block Diagram



Summary

- OMAP 4430
 - State of the art application processor
 - Best in class power/performance
 - All the fundamental IP blocks are major upgrades from the OMAP 3430 [state of the art in 2007..]
 - All the supporting devices ready and waiting -
 - Power management/Audio chips
 - Clock distribution chips
 - WLAN/GPS/BT/Fm radio + S/W integration
 - Modem integration
- If interested contact your local TI representative..



Thank you And thanks to WW OMAP 4430 team -

