

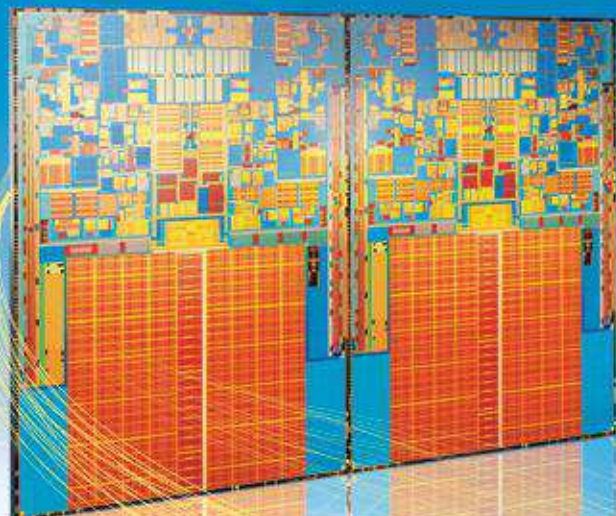


Larrabee: A Many-Core x86 Architecture for Visual Computing

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Larrabee Chief Architect**

Hot Chips 20

August 26, 2008



Agenda

Architecture Convergence

Larrabee Architecture

Graphics Pipeline

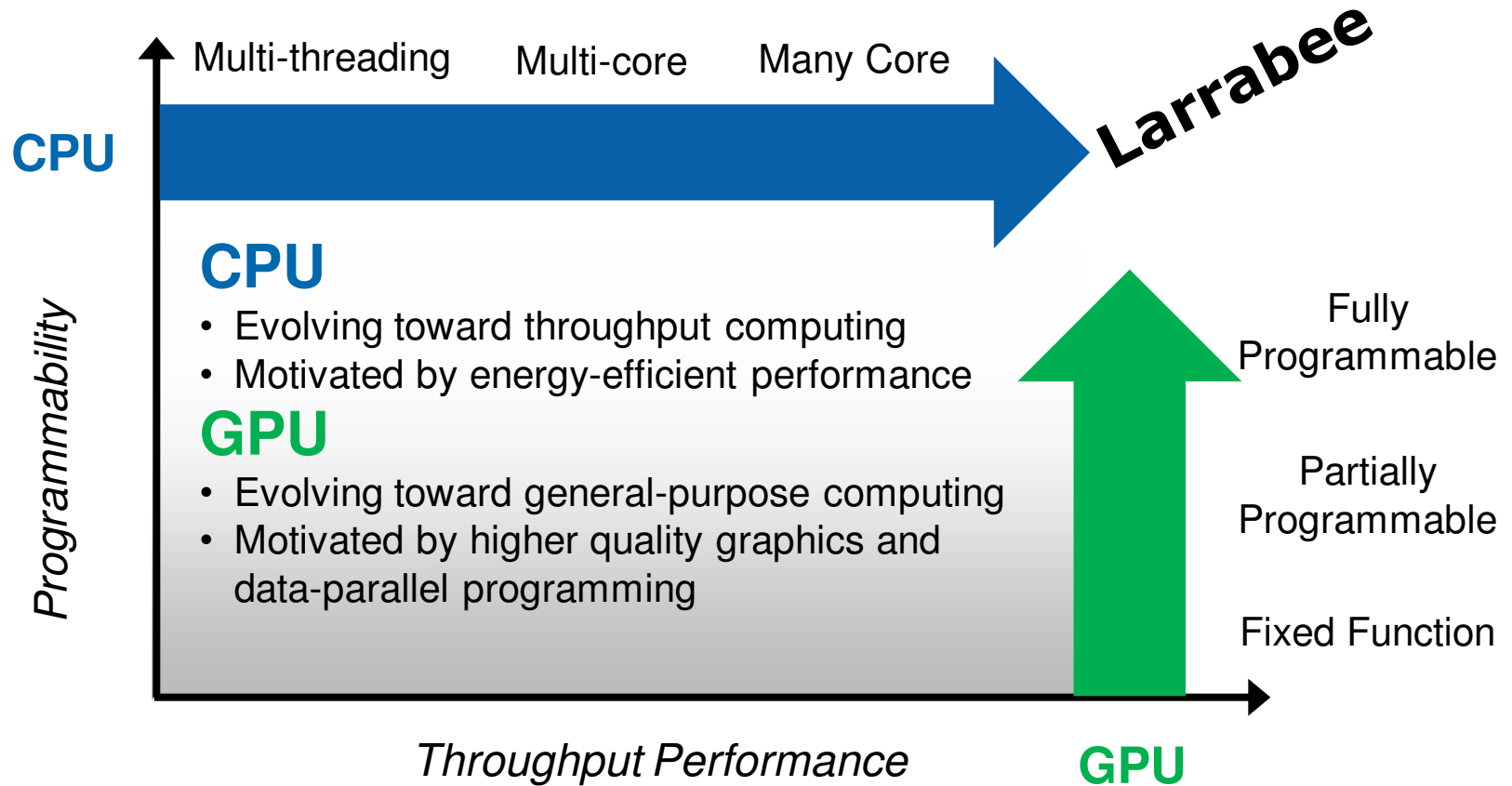
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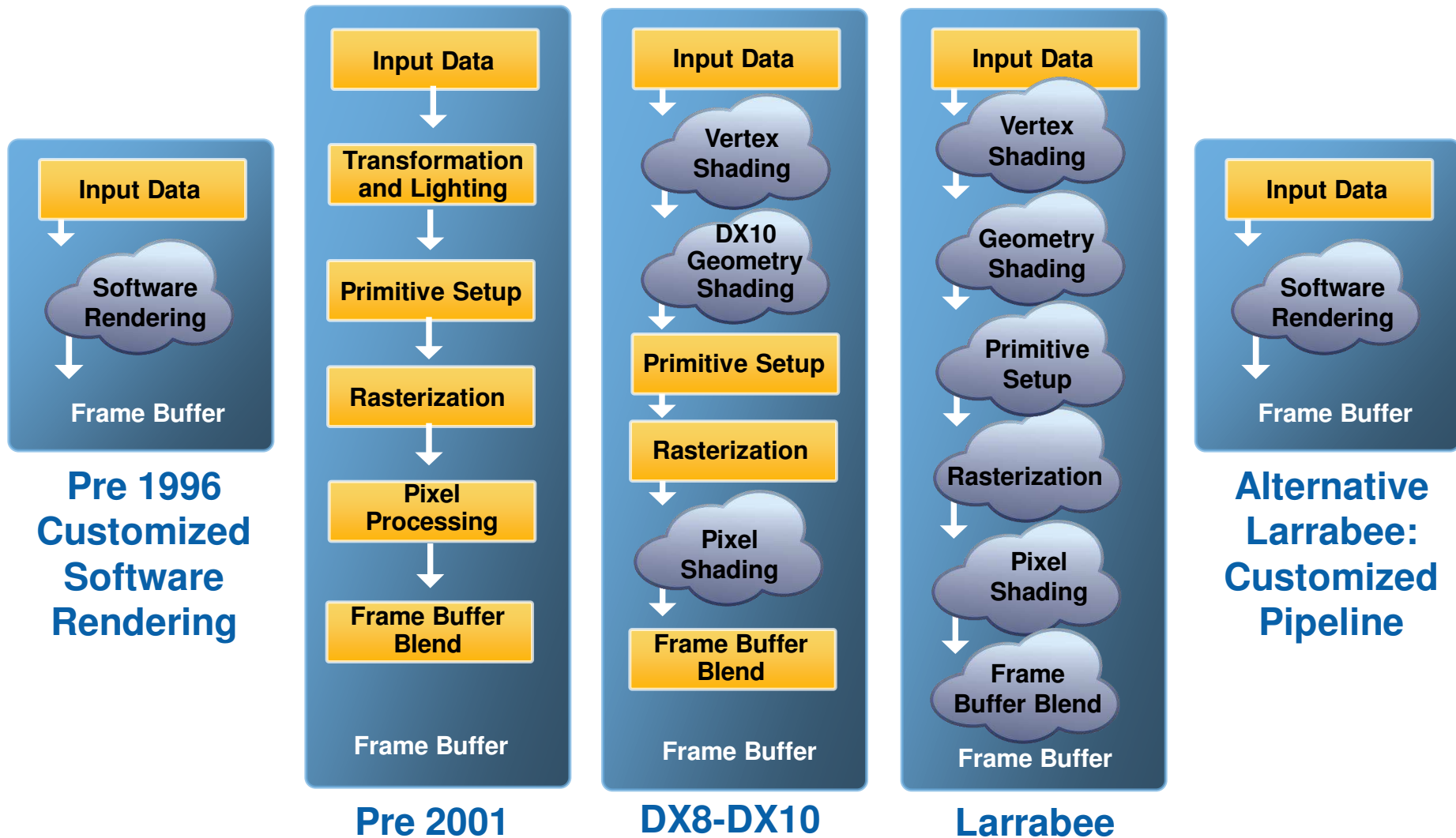
Architecture Convergence



Larrabee: CPU programmability with GPU throughput



Graphics Rendering Pipelines



Larrabee \Lar*a*bee"\, n. [from Intel]

1: a general, programmer-friendly, architecture combining data level and thread level parallelism optimized for high performance throughput applications

2: a high performance visual computing device

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Cores for Throughput Tasks

CPU design experiment:
*specify a throughput-
optimized processor with
same area and power of a
standard dual core CPU.*

Design experiment: not a real 10-core chip!

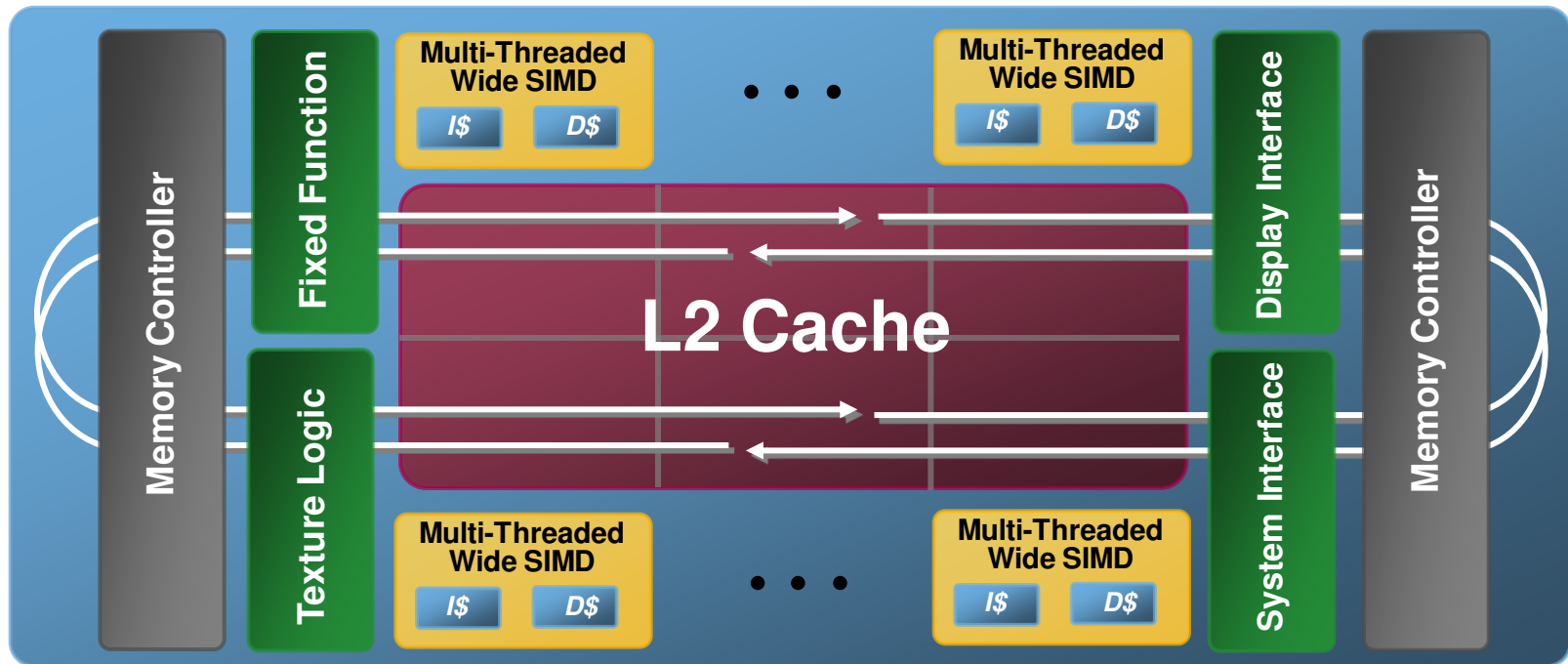
# CPU cores	2 out of order	10 in-order
Instructions per issue	8 per clock	2 per clock
VPU lanes per core	4-wide SSE	16-wide
L2 cache size	4 MB	4 MB
Single-stream	4 per clock	2 per clock
Vector throughput	16 per clock	160 per clock

10 times the peak throughput per clock

**Peak vector throughput for given power and area.
Ideal for graphics & other throughput applications.**

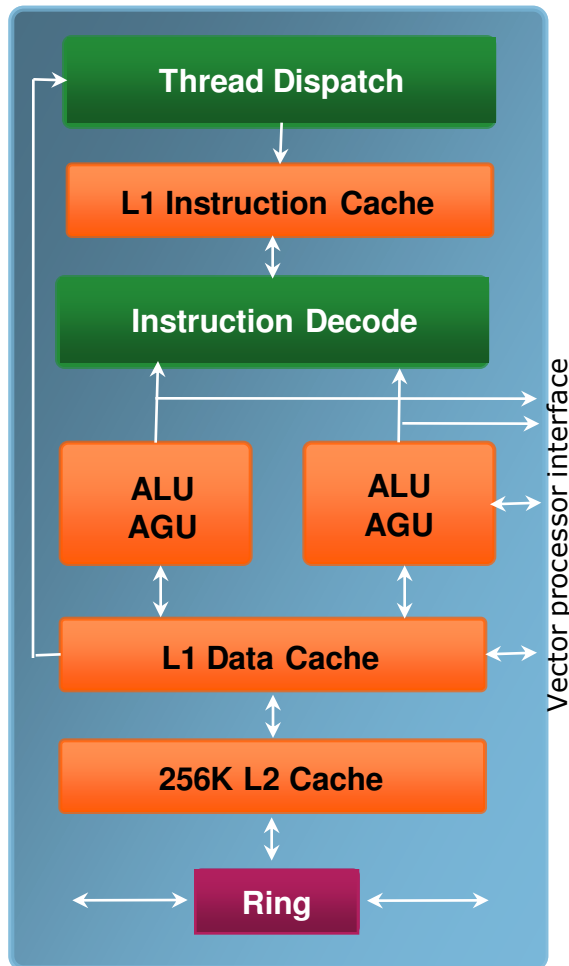


Larrabee Block Diagram



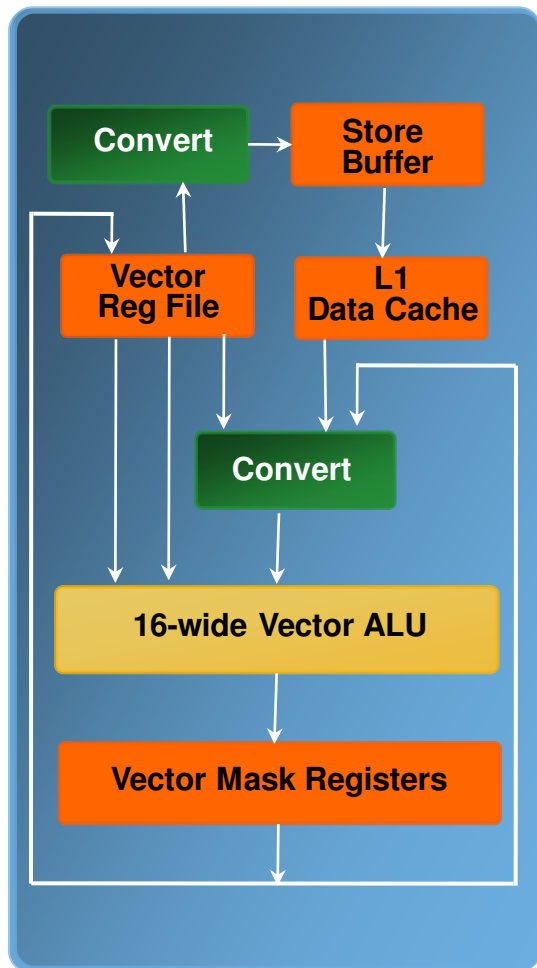
- IA Cores communicate on a wide ring bus
 - Fast access to memory and fixed function blocks
 - Fast access for cache coherency
- L2 cache is partitioned among the cores
 - Provides high aggregate bandwidth
 - Allows data replication & sharing

Larrabee IA Core



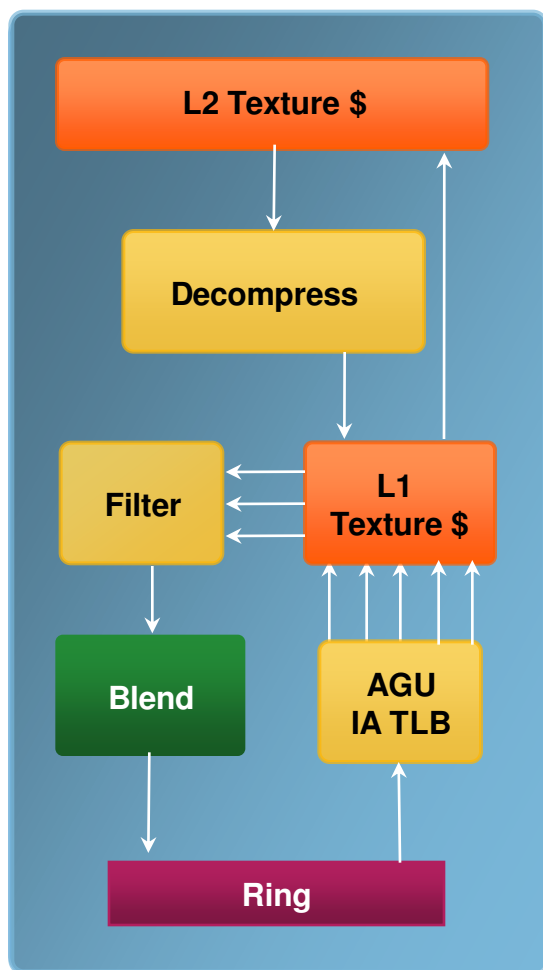
- Separate scalar and vector units with separate registers
- In-order IA scalar core
- Vector unit: 16 32-bit ops/clock
- Short execution pipelines
- Fast access from L1 cache
- Direct connection to subset of the L2 cache
- Prefetch instructions load L1 and L2 caches

Vector Processing Unit



- Vector complete instruction set
 - Scatter/gather for vector load/store
 - Mask registers select lanes to write, which allows data-parallel flow control
 - Can map a separate execution kernel to each vector lane
- Vector instructions support
 - Fast, wide read from L1 cache
 - Numeric type conversion and data replication while reading from memory
 - Rearrange the lanes on register read
 - Fused multiply add (three arguments)
 - Int32, Float32 and Float64 data

Texture Sampler



- Fixed function texture sampler
 - Typical texture operations, including decompression, anisotropic filtering
 - Core communication via the L2 cache
 - Supports virtual address translation using IA page formats
- Fixed function vs. software
 - Texture filtering needs specialized data access to unaligned 2x2 blocks of pixels
 - Filtering is optimized for 8-bit color
 - Code would take 12x longer for filtering or 40x longer if texture decompression is required

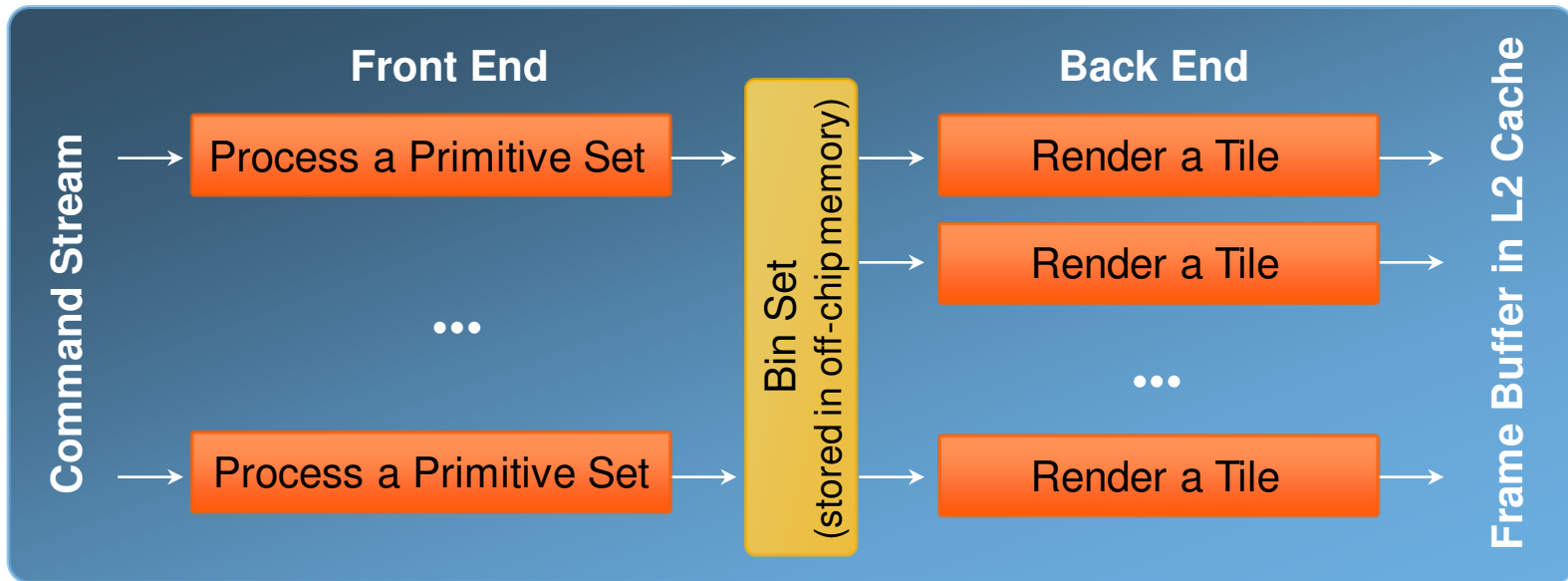
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Architecture Convergence

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Graphics Pipeline

Larrabee's Binning Renderer



- Goals of a Binning Renderer:

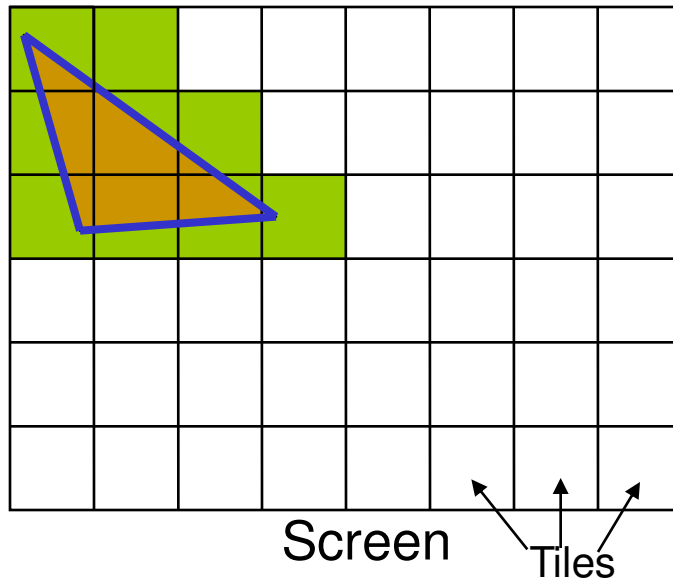
1. Parallelism

- a) Provide independent work queues for cores/threads
- b) Significantly reduce synchronization points

2. Bandwidth Efficiency

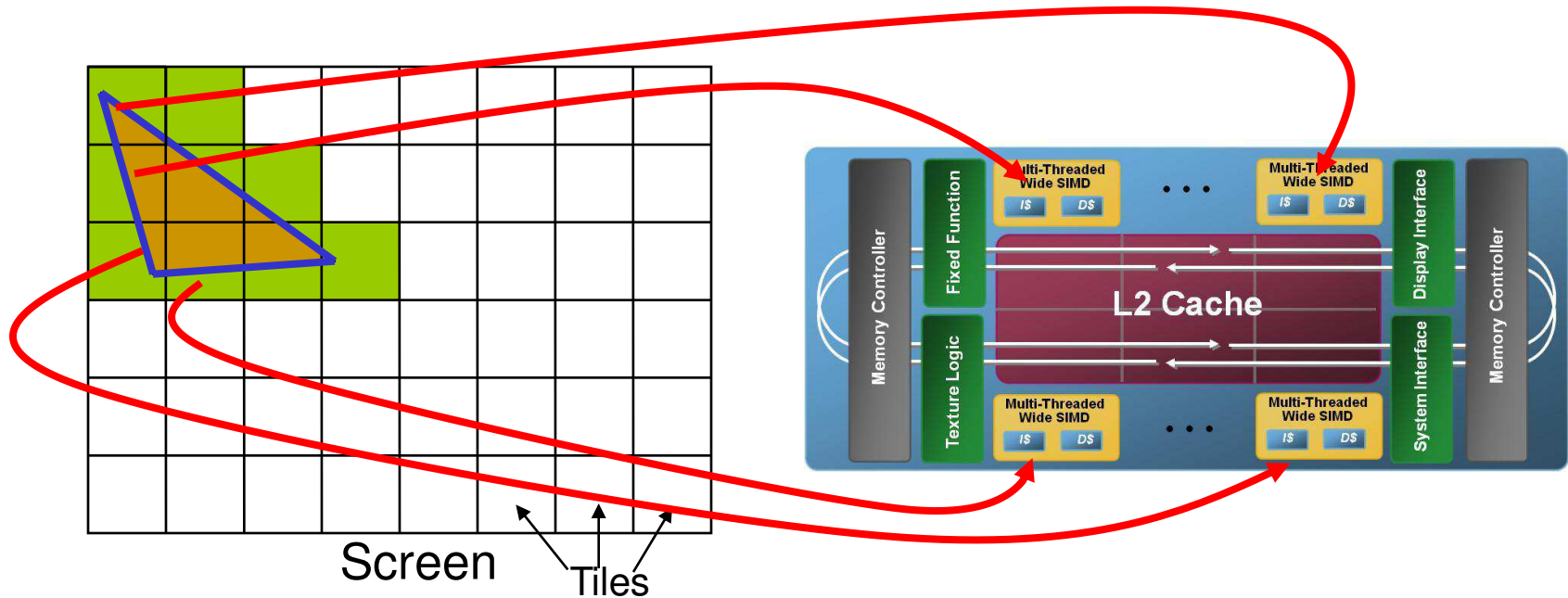
- a) Utilize on-die caches
- b) Reduce off-die bandwidth pressure

Larrabee's Binning Renderer



Screen is tiled and tiles processed concurrently
Software buffers (pixel, depth) also tiled
Tremendous bandwidth to tiled buffers

Larrabee's Binning Renderer



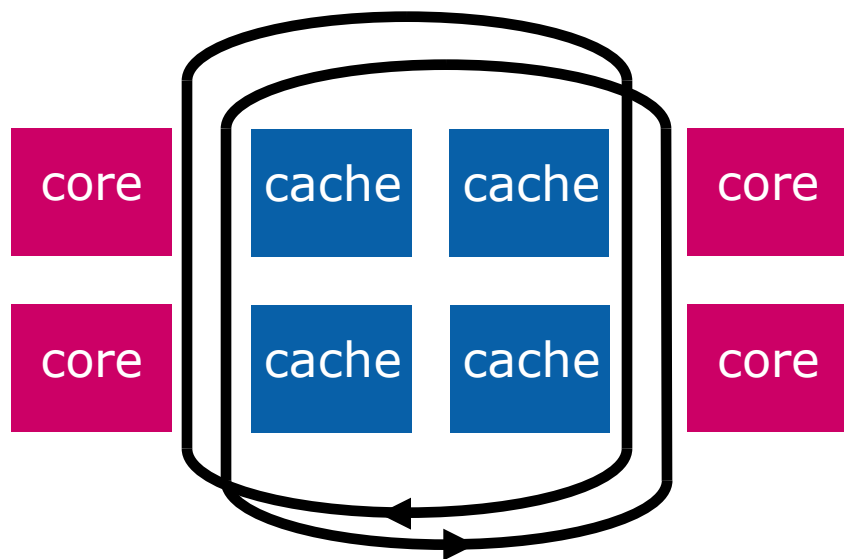
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Bandwidth Implications

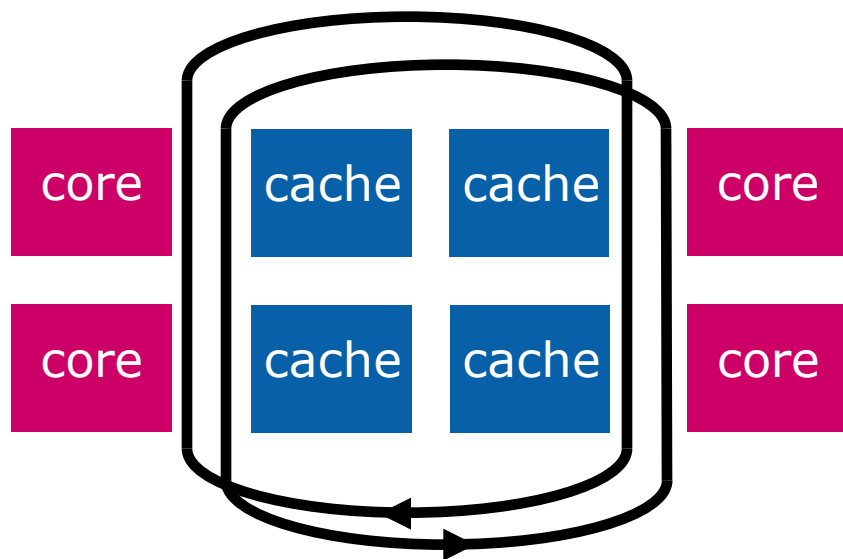


Server Style Interconnect



Bi-direction ring: physically sits over cache
Banked, logically unified ring cache
Straightforward, elegant architecture
Tremendous aggregate ring bandwidth

Server Style Interconnect: 3D Graphics



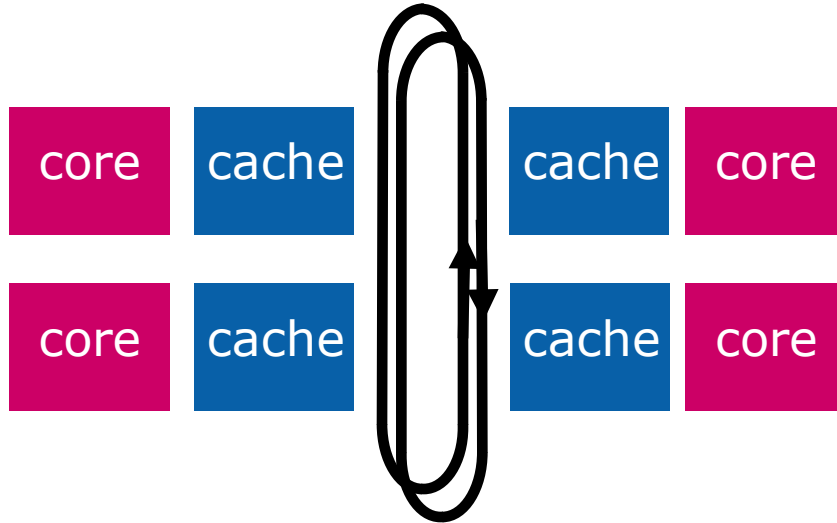
3D graphic tile buffers reside in ring cache

Tiles don't fit in cores L1\$

Tremendous BW to tiled buffers

Tile buffer BW requirement => heavy ring traffic

Larrabee Ring



Access ring on private L2\$ miss

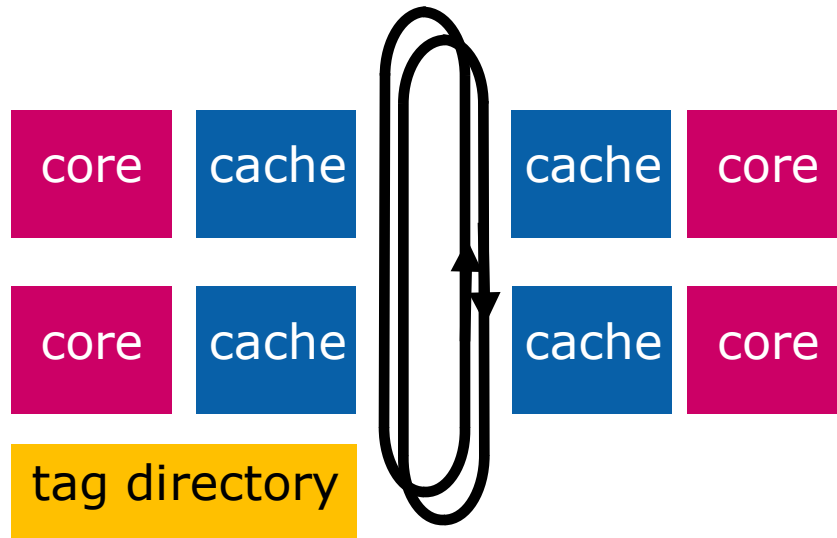
Tile buffer accesses do not travel on ring

However, memory coherence implies

L2\$ miss requires snooping of all other L2\$

RFO transaction needs to traverse ring

Larrabee Ring with Central Tag Directory



Central tag directory (td) reduces coherence traffic

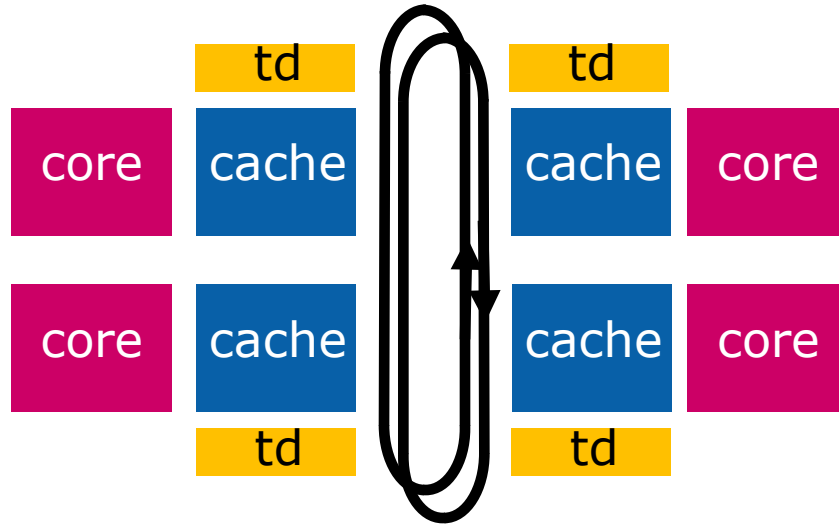
- Copy of all L2\$ tags

- Tracks MESI state

However, hot spot at the tag directory

- Tag directory BW doesn't scale with cores

Larrabee Ring: Distributed Tag Directory



Distributed tag directory (td)

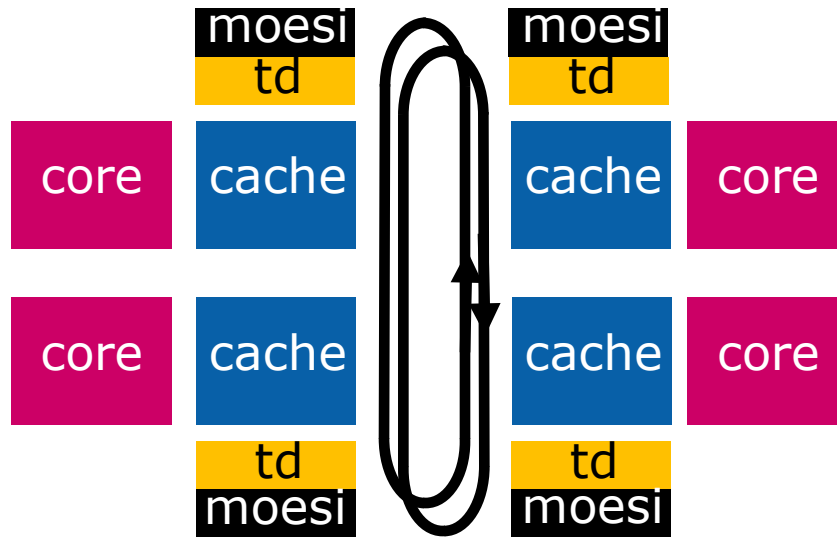
Address hash to determine specific tag directory

Solves hot spot

However, cache-cache transfer require global ordering

Introduces serialization

Larrabee Ring: Enhanced Coherency

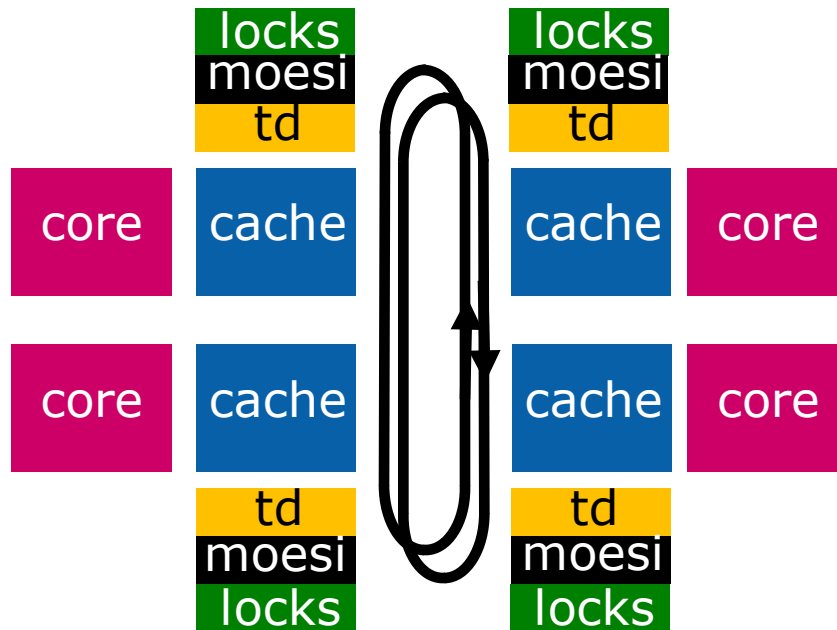


Change from MESI to MOESI

Cache-cache ownership transfer on die

However, contended locks still hop around ring

Larrabee Ring: Future Enhancement



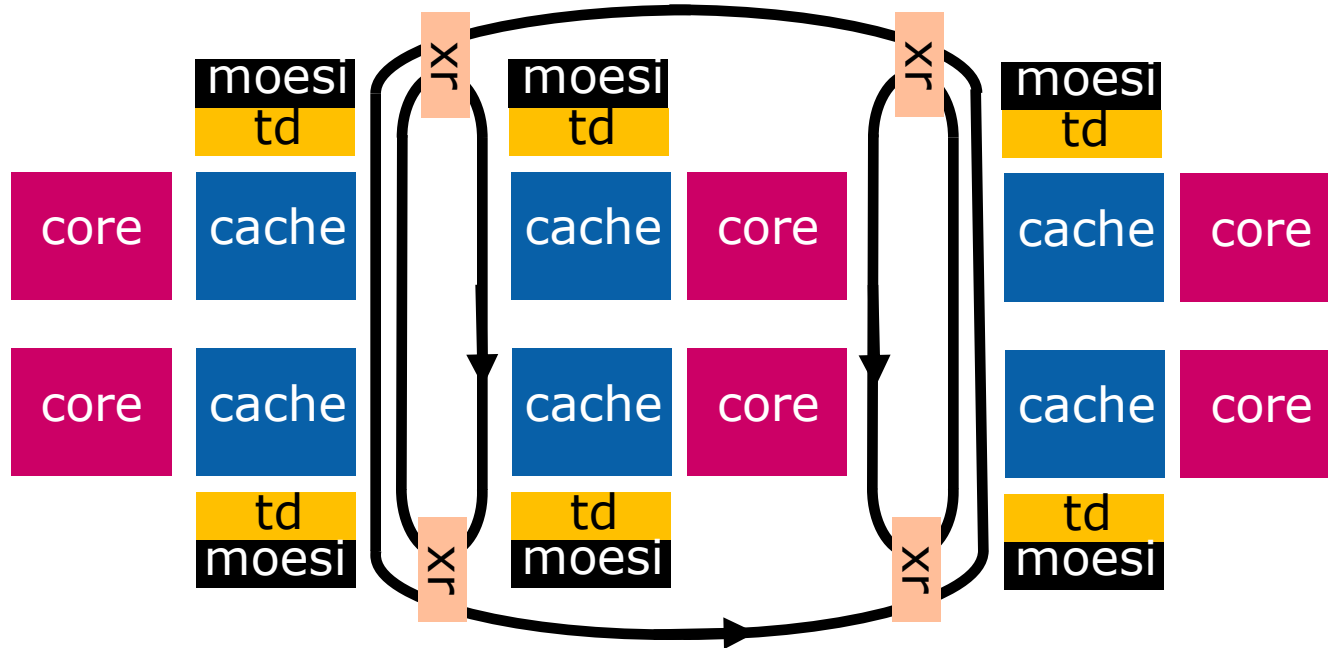
Lock cache holds lines containing contended locks

Locked inc/dec/cmp use ALU in lock cache

Big speedup (>10x) on contended locks

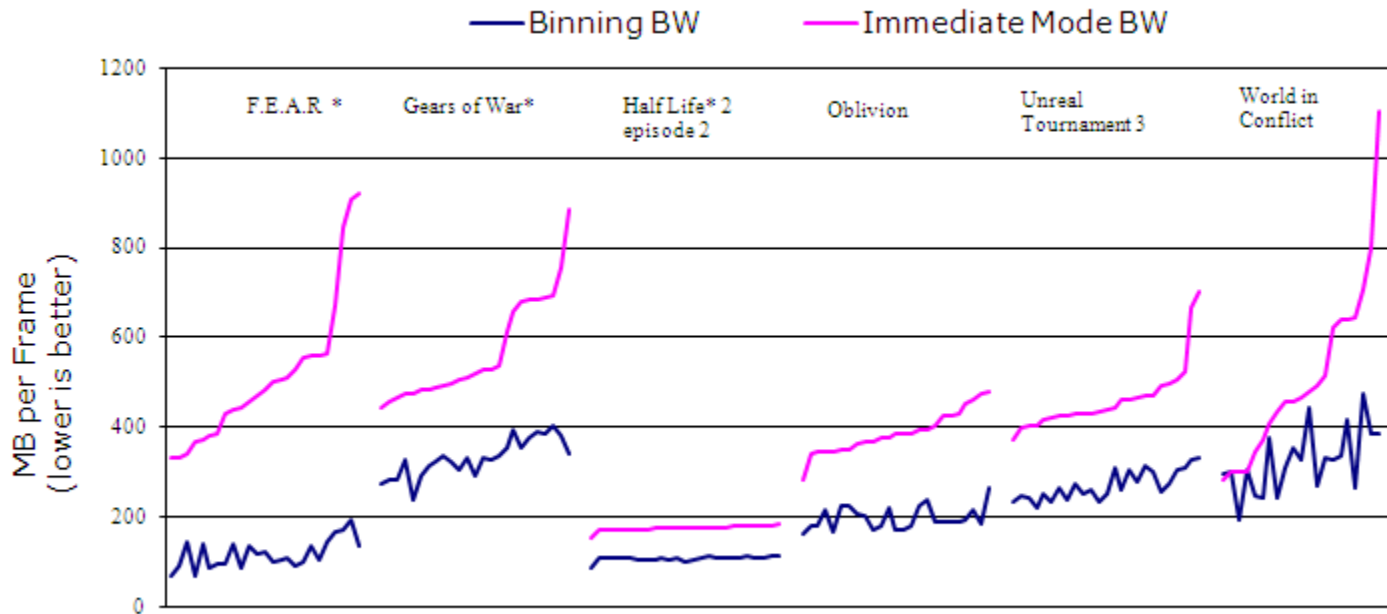
Contended lock throughput @ 1 per clock

Larrabee Ring: Scalability



- Large core count configurations need higher bandwidth
- Required flexibility for physical topology
- Xring: 3 separate rings with efficient ring crossing

Bandwidth Results



- Binning mode

- Includes bin reads & writes
- Reads/writes each pixel once due to tiles in the L2 cache

- Immediate mode

- Assumes perfect HeirZ cull
- Assumes 1MB each for compressed depth, color and stencil buffers

Summary

- Each Larrabee core is a complete IA core
 - Context switching & pre-emptive multi-tasking
 - Virtual memory and page swapping
 - Fully coherent caches at all levels of the hierarchy
- Efficient inter-block communication
 - Ring bus for full inter-processor communication
 - Low latency high bandwidth L1 and L2 caches
 - Fast synchronization between cores and caches
- Elegant use of fixed function logic
 - No backend blender between cores and memory
 - No rasterization logic between vertex and pixel stages
 - Result: flexible load balancing & general functionality

Larrabee: a general throughput computing architecture



Questions?



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