A Low-Cost Chip Set for Broadband Powerline Communications at 200 Mbps

Chano Gómez, DS2

HotChips'20
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What is Powerline Communications?

Powerline Communications is a technology that enables transmission of high-speed data over electrical lines.

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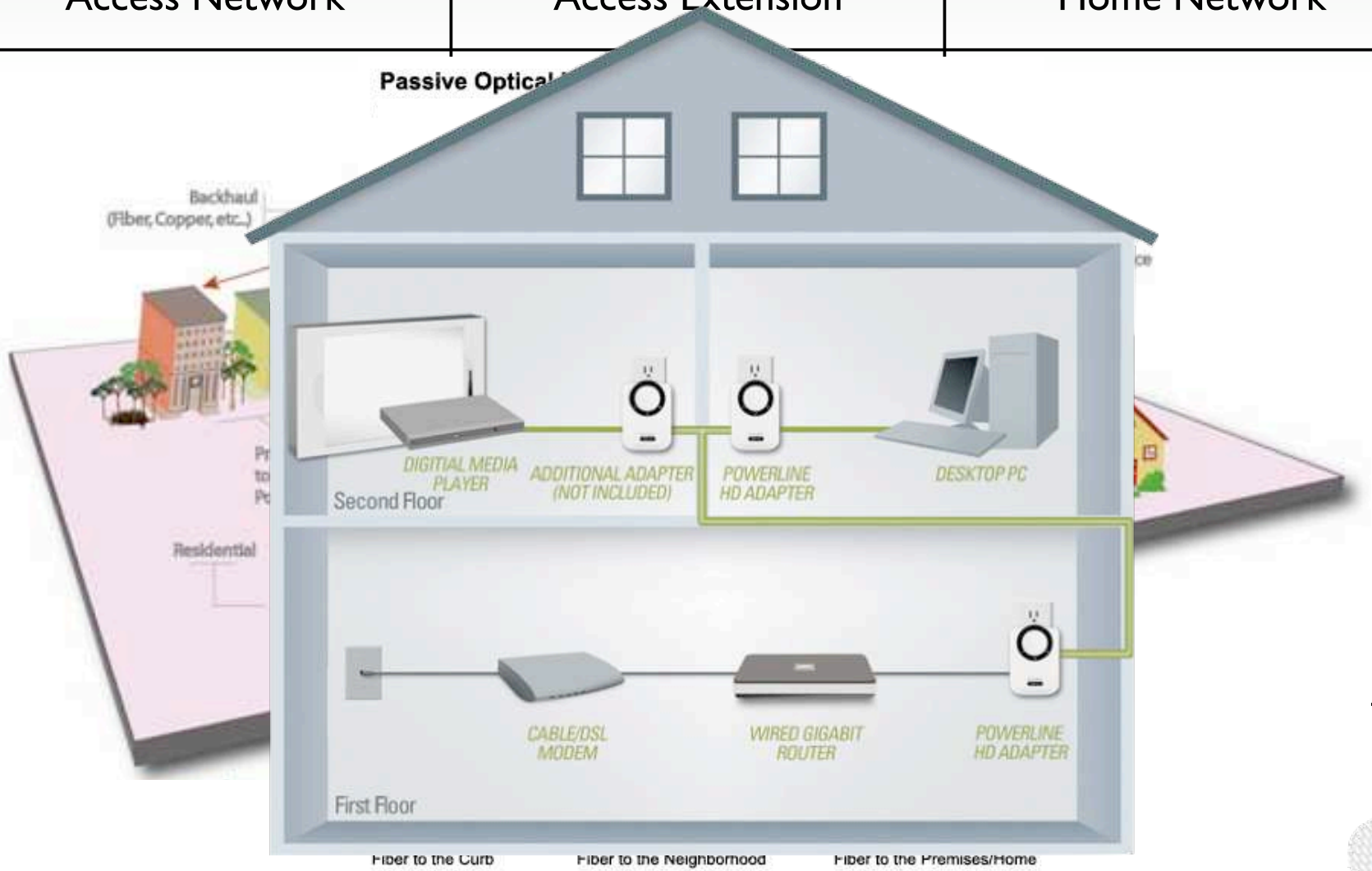
What are the Applications?

Access Network	Access Extension	Home Network



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Wall-plug is most common form factor

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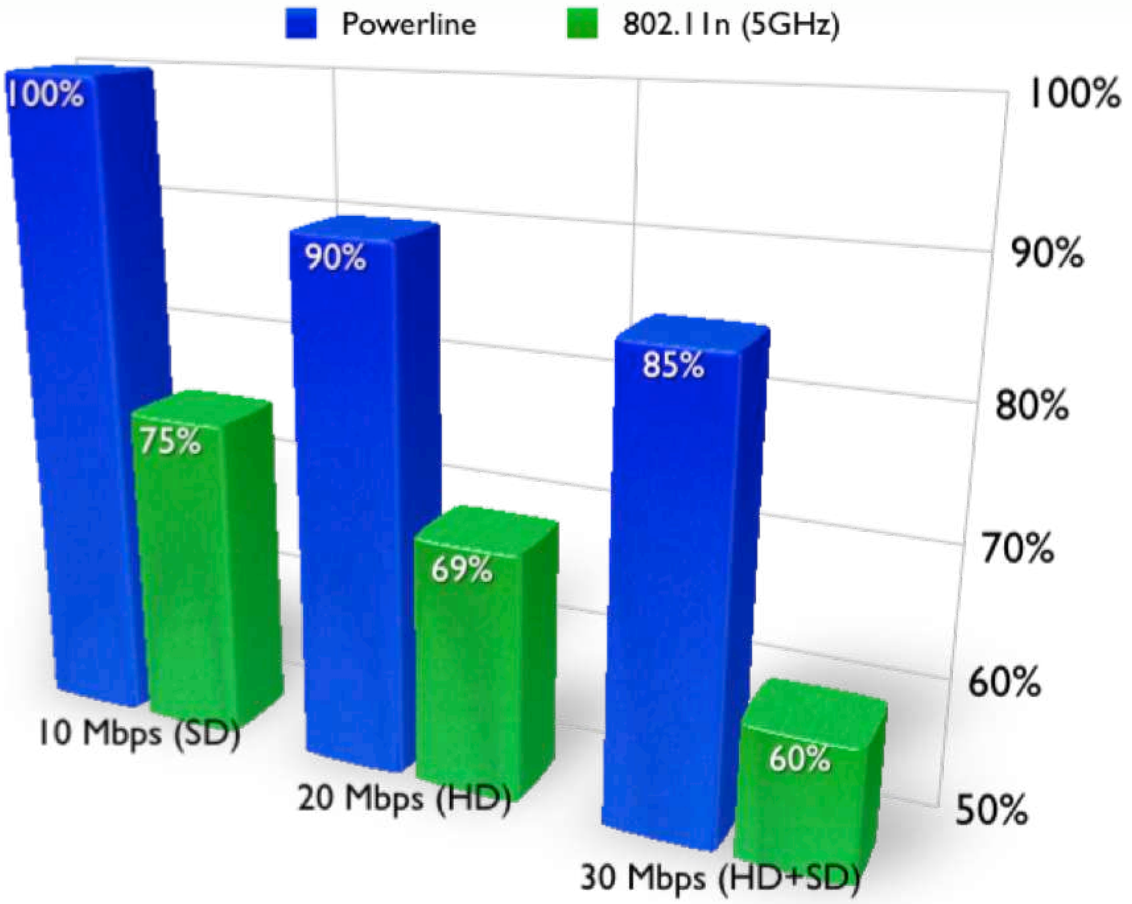
Why not simply Wireless?

Because Powerline provides connectivity where Wireless 802.11n can't



Percentage of locations capable of delivering 10, 20 & 30 Mbps UDP streams with 0% PLR.
Test performed in 9 homes in urban areas in Europe. Source: DS2

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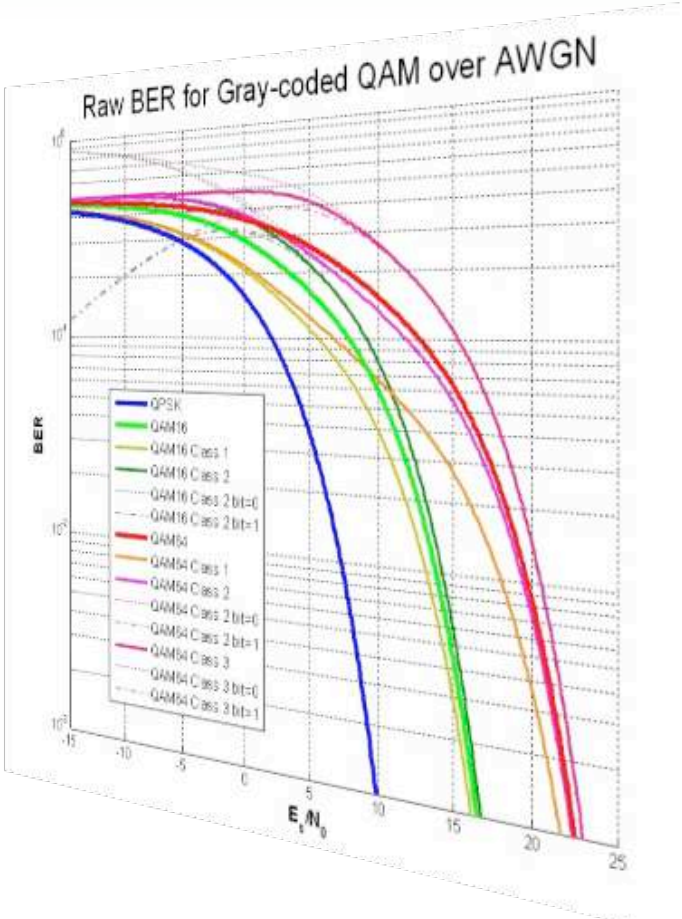
Powerline Networking is a Challenging Technical Problem

- Electrical wires were never designed for high-speed transmission...
  - Uncontrolled and (almost unpredictable) environment
  - Impedance mismatch causes Strong multi-path effect
  - Unknown, non-flat and non-stationary channel frequency response
  - Electrical devices connected to the network generate non-gaussian, non-white, non-stationary noise
  - Risk of EMC problems because of unshielded wires



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Technical Features of Modern Powerline Communication Systems

Feature	Type	Why?
Frequency	2-32 MHz	Lower Frequencies are too noisy. Higher Frequencies have too much attenuation and FCC limits are too strict
Modulation	OFDM	OFDM systems can adapt to non-frequency-flat channels well.
MAC	TDMA	Time-Division Multiple Access provides better QoS than CSMA systems
PHY Data Rate	200 Mbps	Currently limited by available spectrum and available SNR
App Data Rate	120 Mbps	MAC, LLC and FEC overhead
Encryption	AES-256	To avoid eavesdropping by neighbours!

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Dealing with the specific characteristics of the power line channel

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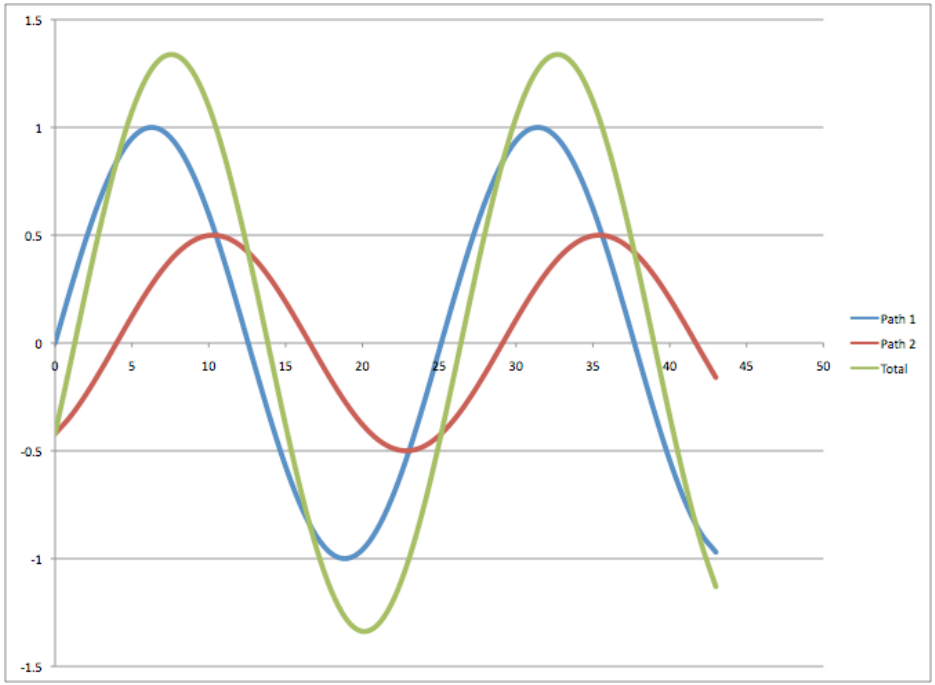
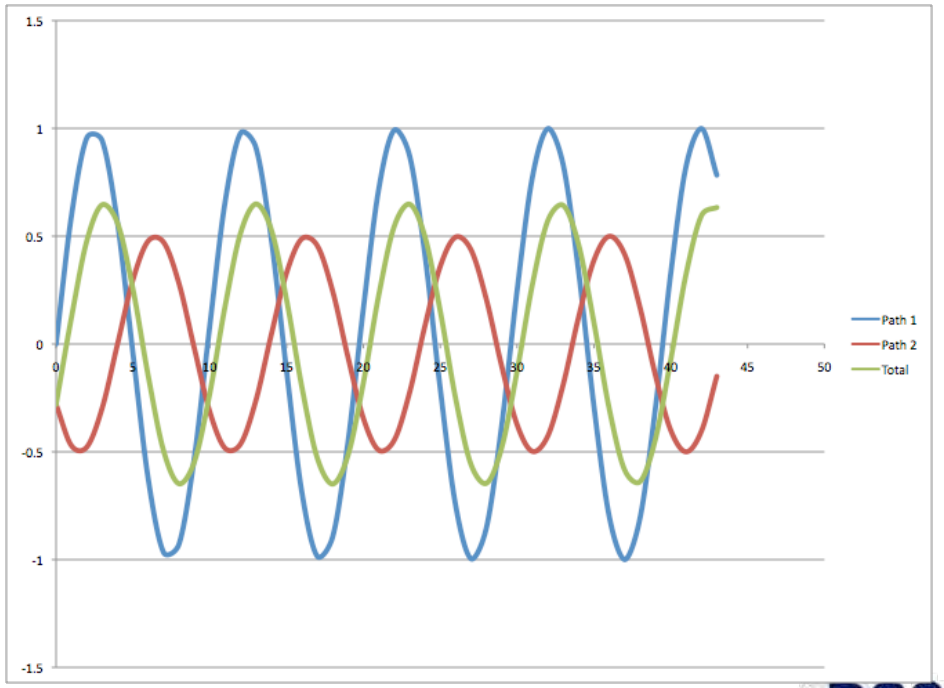
Multipath Effect: Channel Response is Frequency Selective

Combination of original signal + echo produce **stronger** signal at frequency f_x

Combination of original signal + echo produce **weaker** signal at frequency f_y





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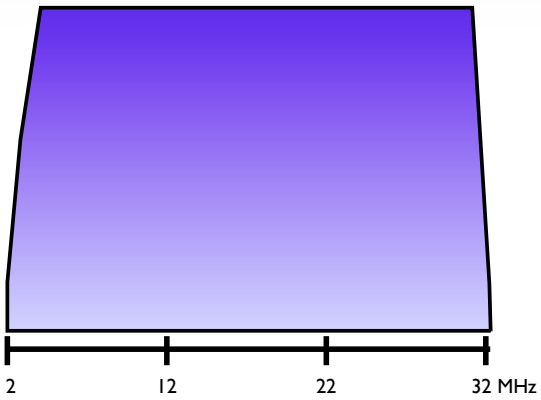
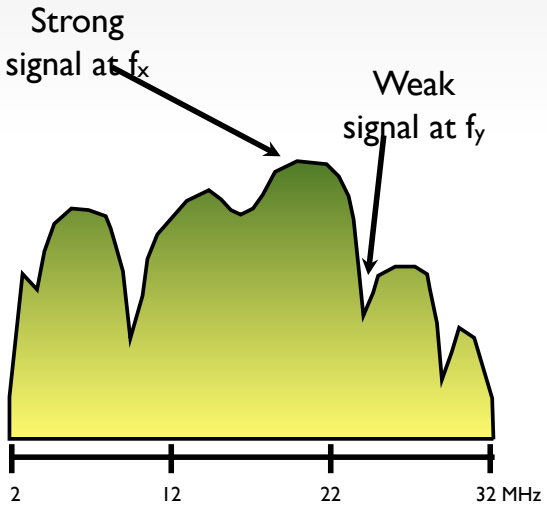
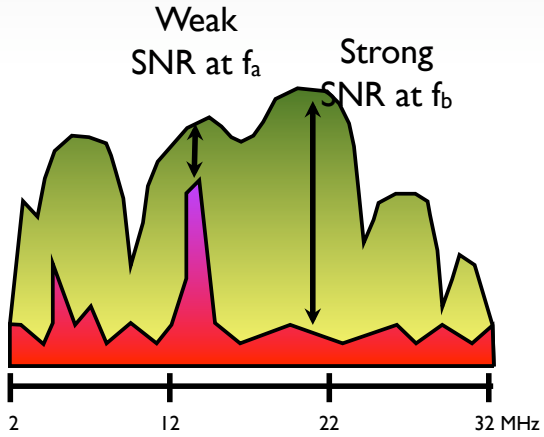
How do received signals look like?



Spectrum of
Transmitted Signal



Spectrum of
Received Signal

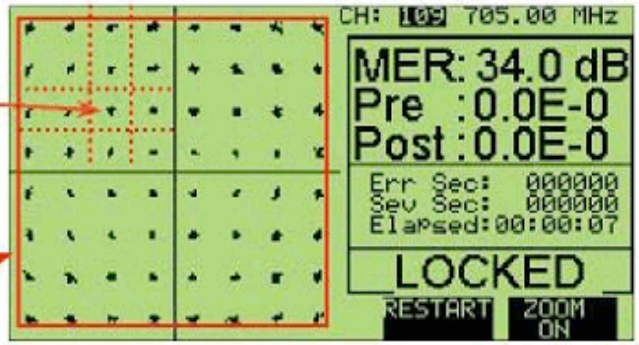


Spectrum of
Received Signal
+ Noise

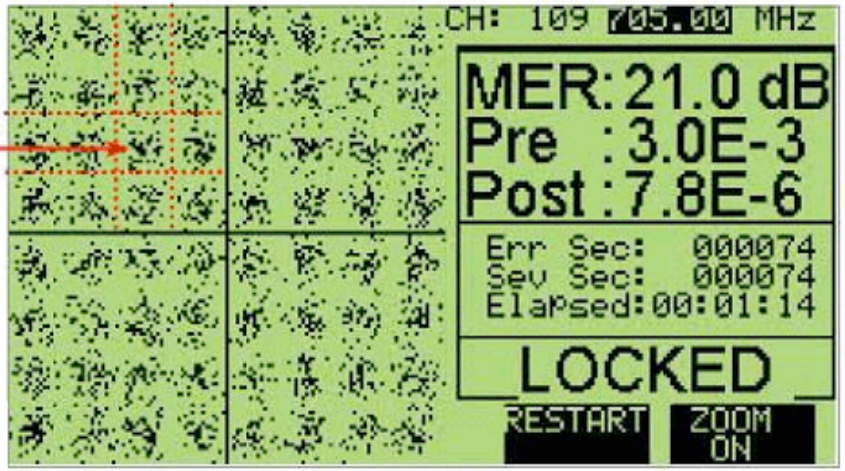
SNR Determines Optimum Modulation Scheme

Well Defined and away from the decision boundaries

Well Positioned Dots in a Square



Dots are spread out causing errors to occur



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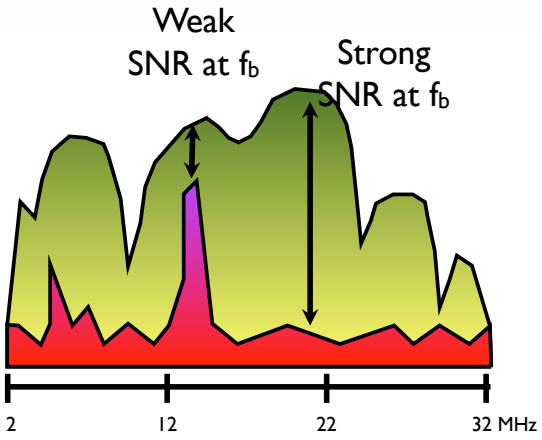
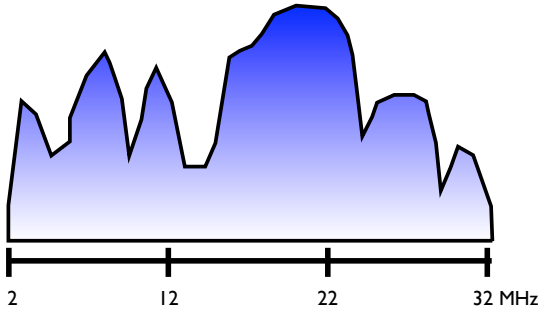
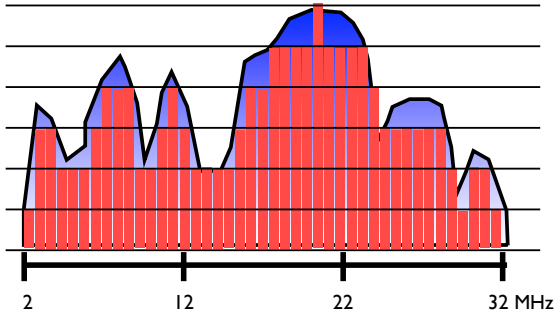
Each sub-carrier is modulated according to the SNR in that frequency



Spectrum of
Received Signal
+ **Noise**

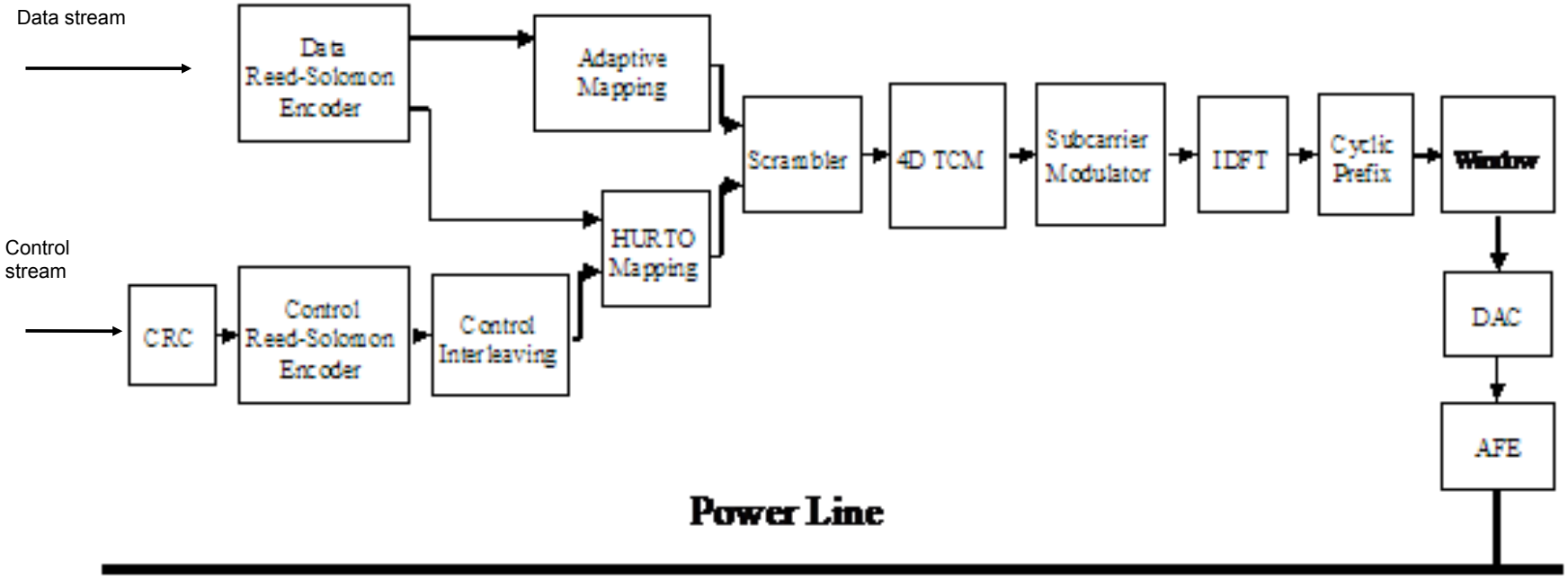


Spectrum of
Signal-to-Noise Ratio
(SNR)



Modulation Level used
in each sub-carrier

Block diagram of a powerline communications transceiver



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Programmable QoS is Key

- Powerline networks are usually deployed in environments where packets may not have QoS tags (802.1p, TOS, DSCP, etc)
- Powerline devices need to figure out how to assign priorities with limited information
- Goal: Allows device manufacturers and service providers to create custom QoS rules that are appropriate for the intended application.
- Example in pseudocode:

```
if ethernet.type == IPv4 then
  if ip.dst_address == 192.168.4.3 then
        powerline.priority = 6
  else
        powerline.priority = 1
else if ethernet.vlan == 5 then
  powerline.priority = 2
```

- Note: in practice this is done configuring registers (see next slide...)

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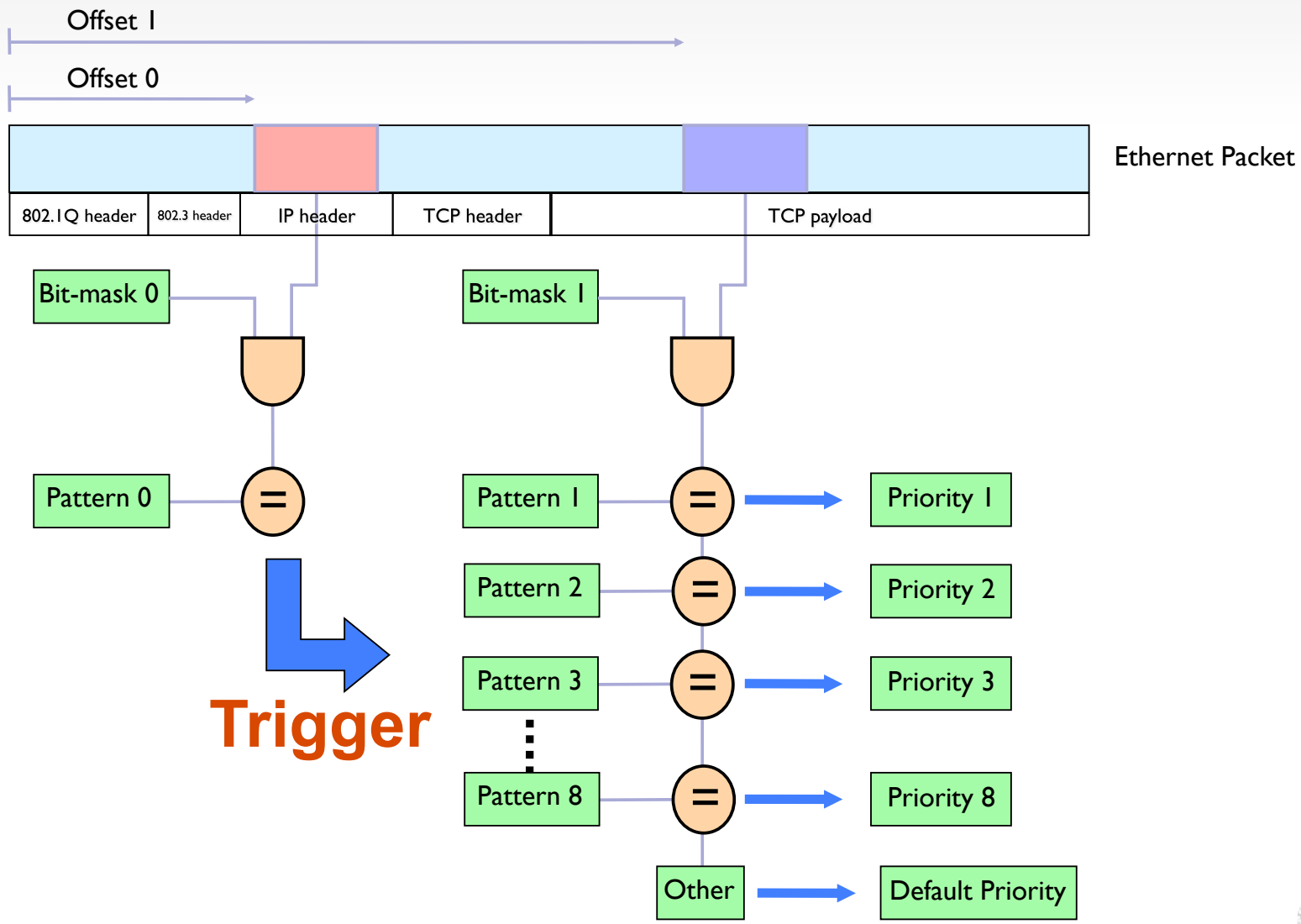
Programming Prioritization Rules



AITANA™ Chipset

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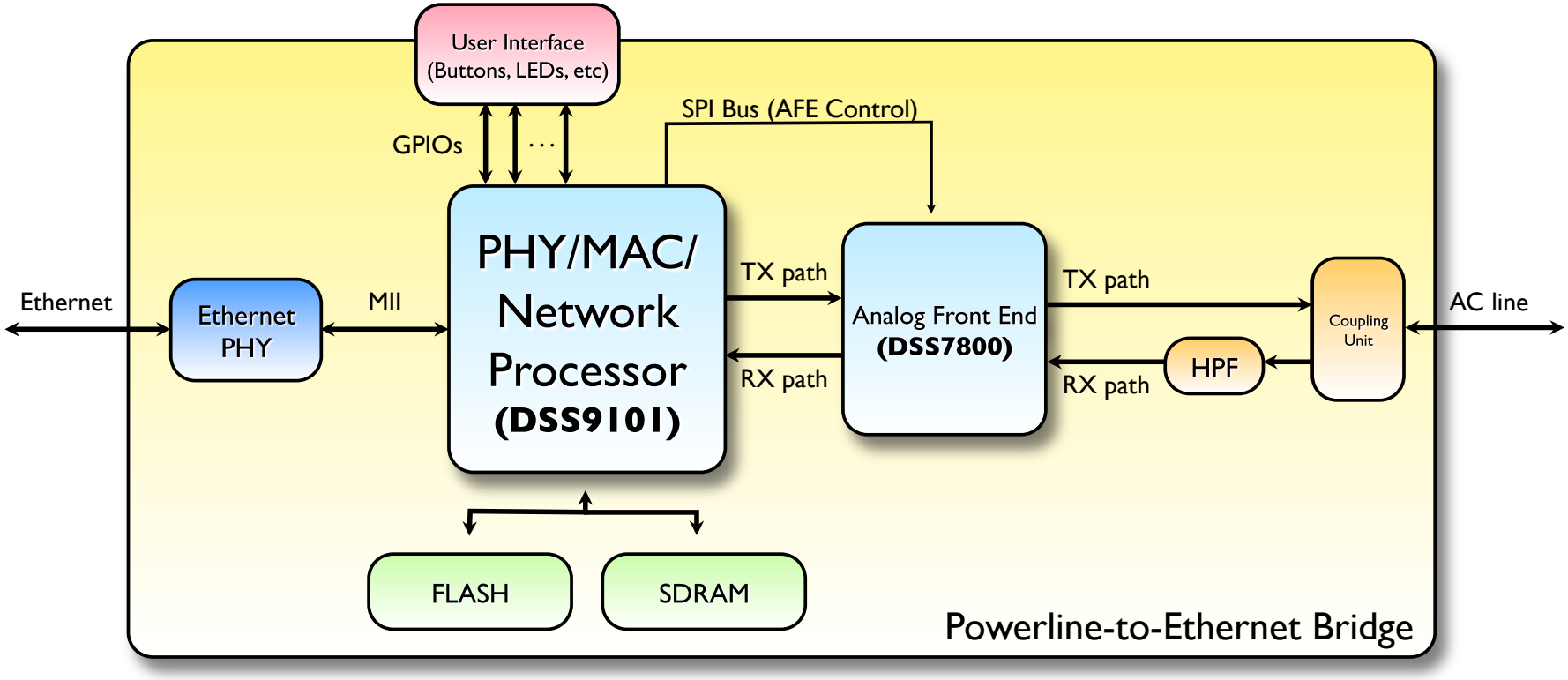
Block Diagram of a Powerline-to-Ethernet Bridge



DSS9101

Area	Description
Application	• PHY, MAC & Network Processor
Standard	• UPA (Universal Powerline Association)
Electrical information	• LQFP176 • Power consumption: 1.2W • I/O Voltage: 3.3V • Core Voltage: 1.5V
PHY	• OFDM Modulation (1536 carriers) • 2-32 MHz • Programmable Carrier Notching • Reed-Solomon + 4D-Trellis FEC • Up to 16 remote devices
Data Rate	• 200 Mbps (PHY layer) • 120 Mbps (Ethernet layer) • 128k packets/sec
Ethernet Switch	• 802.1d compliant, supports STP • 802.1Q compliant • 32 MAC addresses • Packet Snooping (IGMP, etc) • Supports automatic repeating
Security	• AES-256, AES-128, 3DES & DES Encryption • Support for "One-Button Security"
QoS	• 8 priorities • Programmable prioritization rules
Embedded Processor	• Tensilica Xtensa (160 MHz) • SDK available
Interfaces	• MII, 2 x SPI, I2S/TDM, 8 x GPIO, JTAG, UART
Technology	• Toshiba SoC • ADC, DAC, PLL provided by Toshiba

upa

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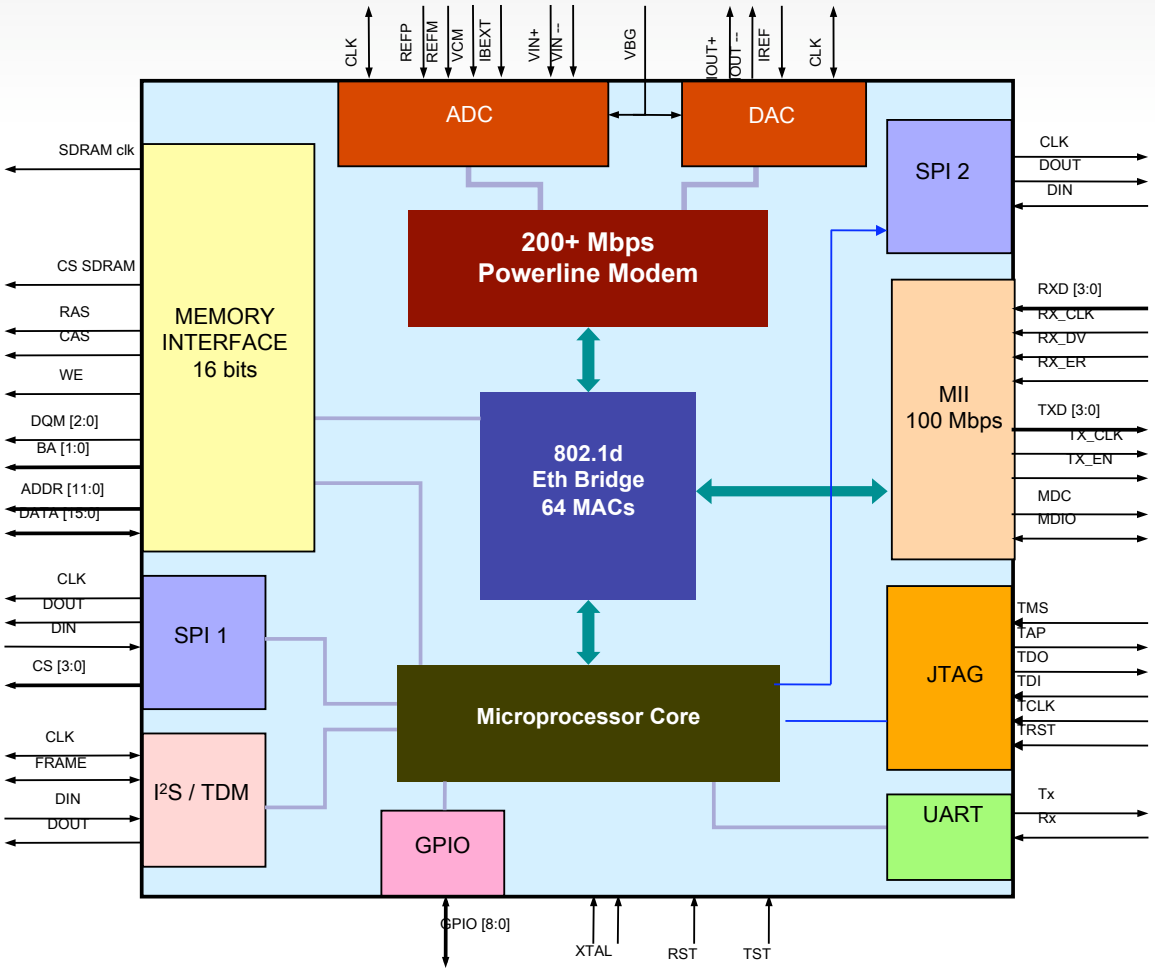
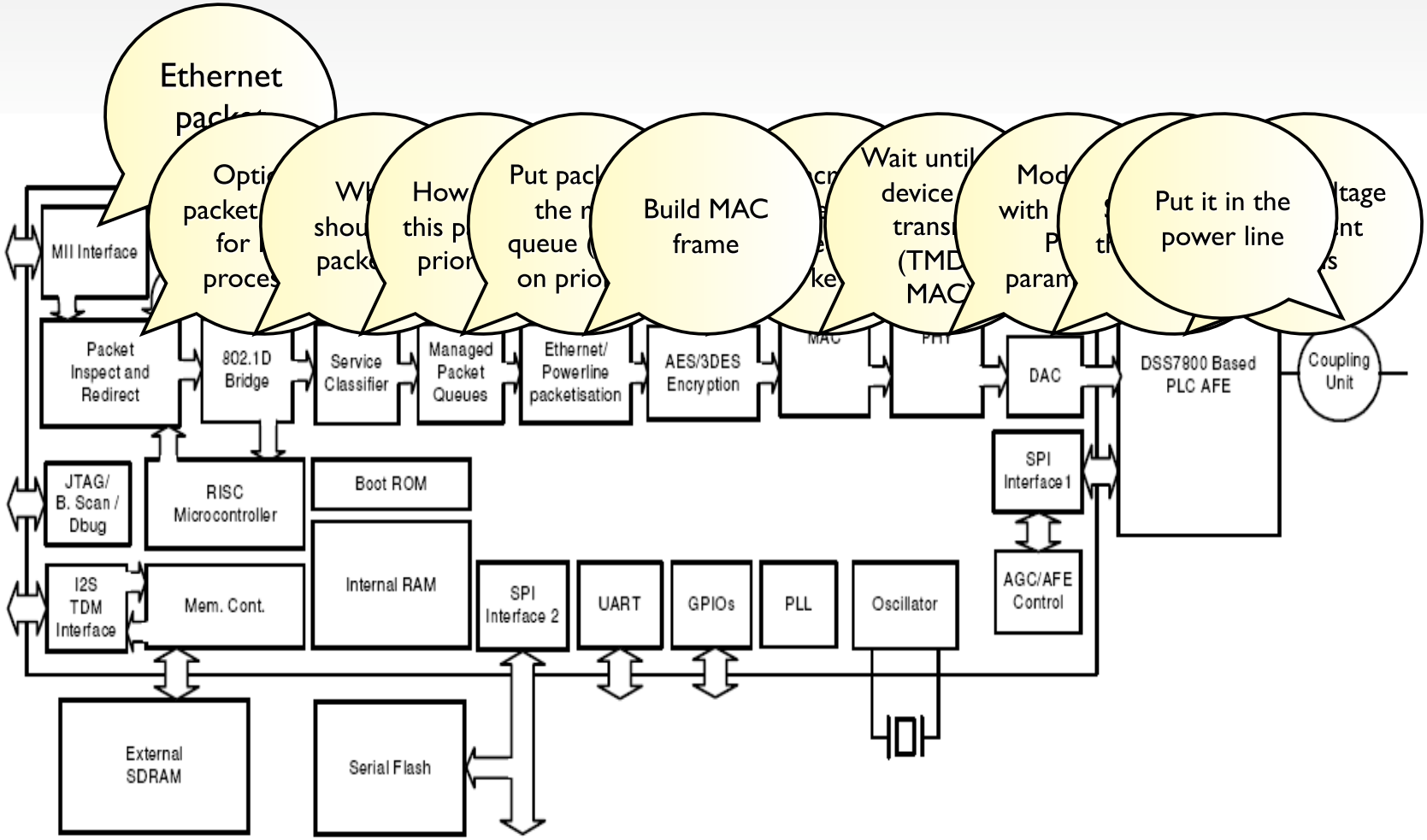
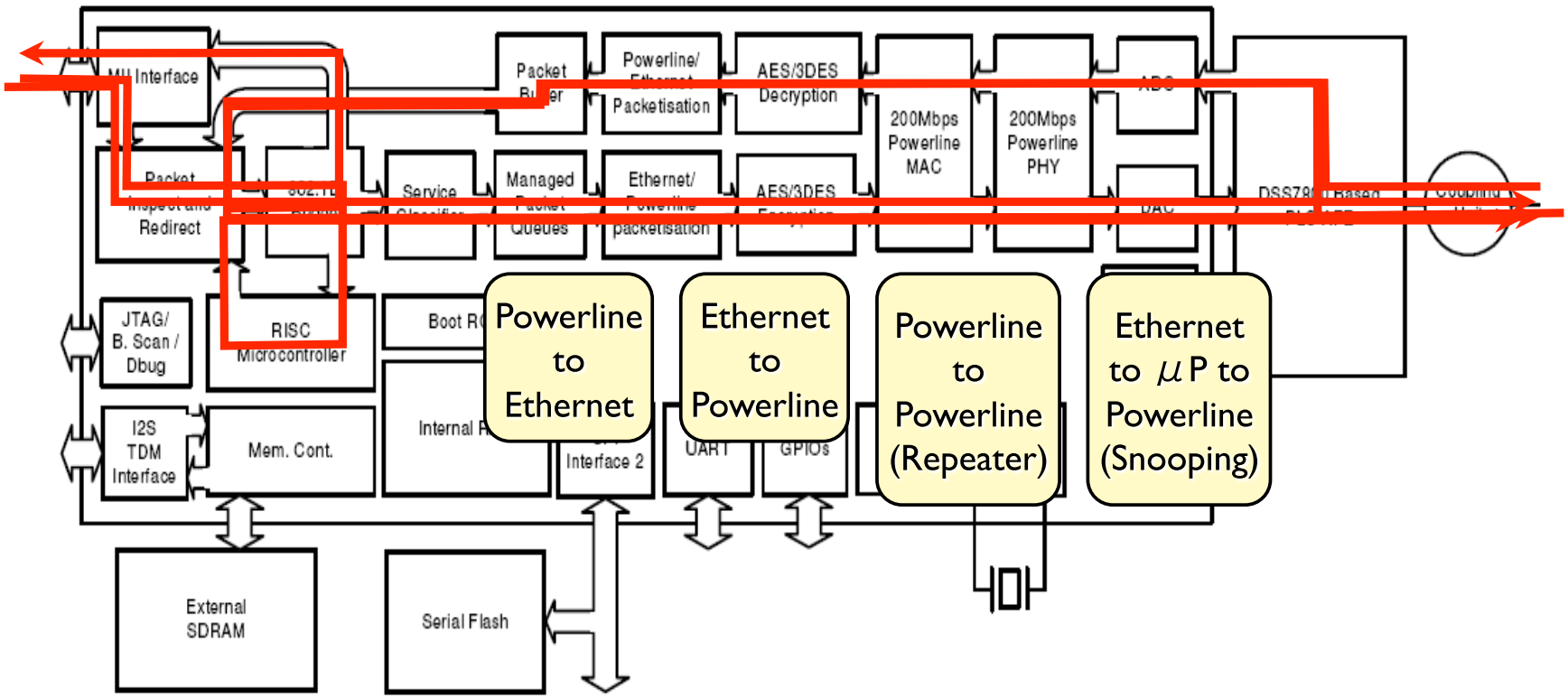
DSS9191 Block Diagram



Packet Flow inside the DSS9101



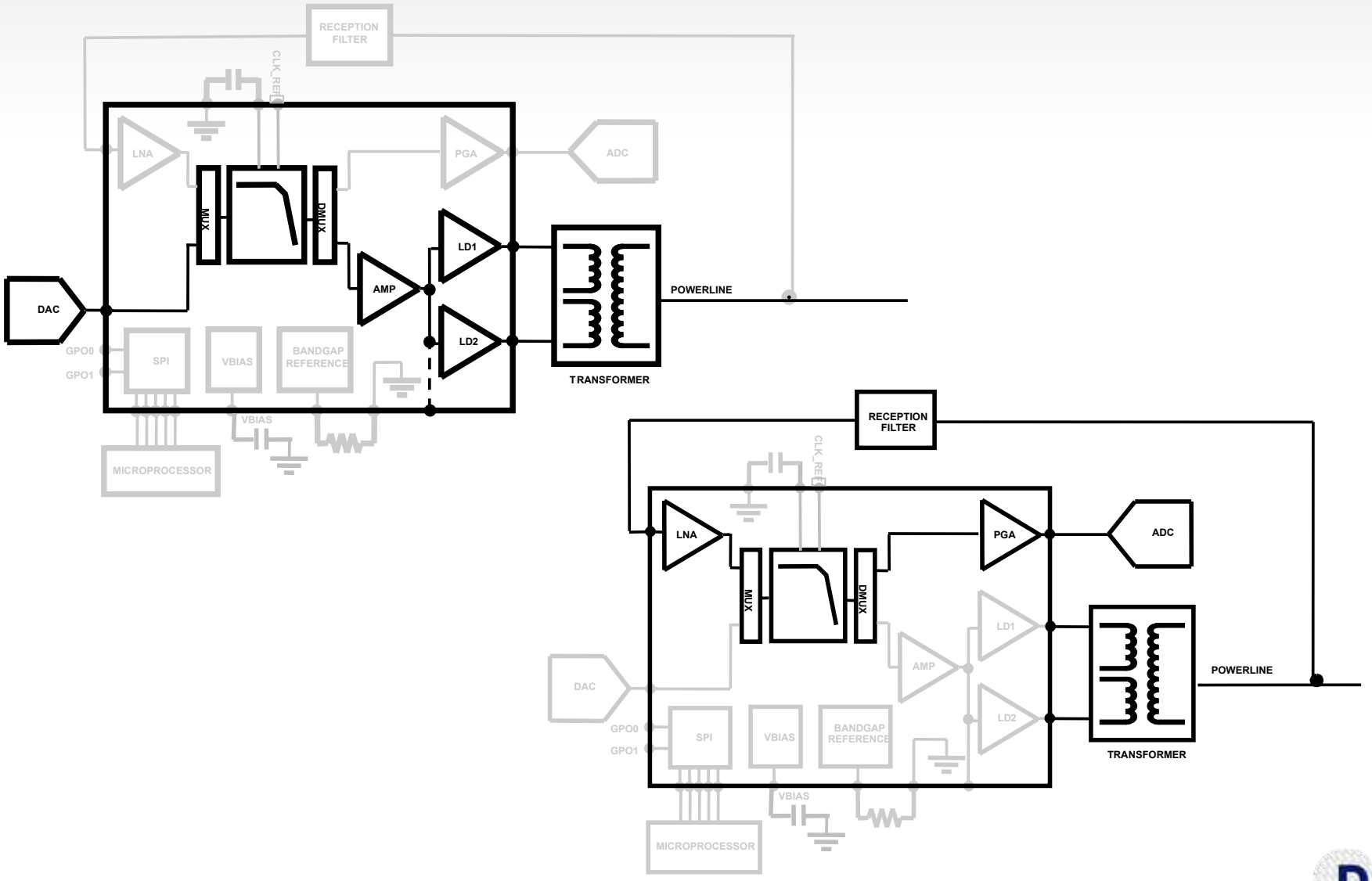
Example of Supported Modes



DSS7800

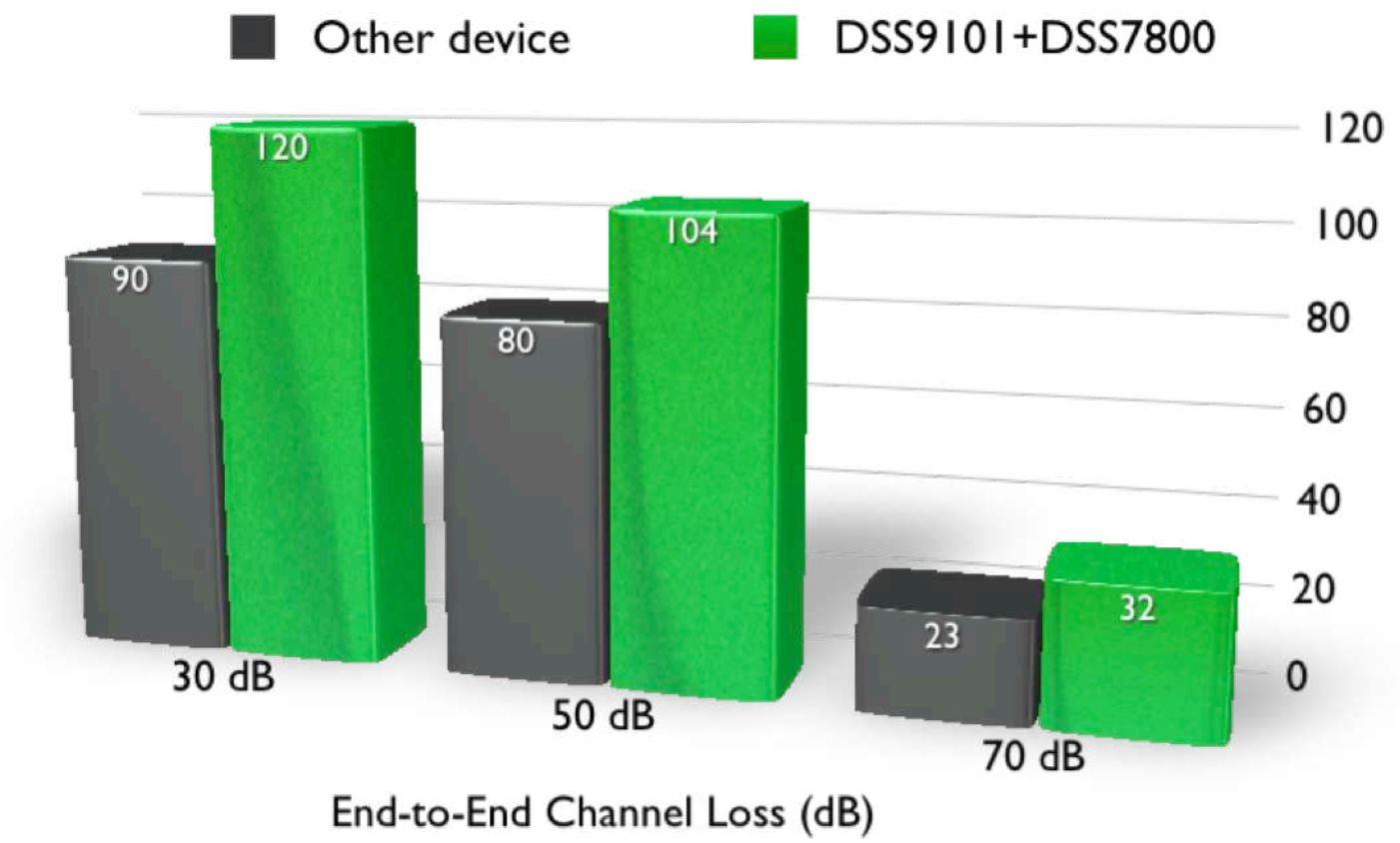
Area	Description
Application	• AFE (Filter + Line Driver)
Electrical information	• QFN48 7x7mm RoHS • 5V Power Supply • Power consumption: • Tx mode: 1700 mW • Rx mode: 685 mW • Idle mode: 15 mW
Features	• Integrated Line Driver • Integrated Low Pass Filter (Anti-aliasing & Smoothing) • Power-down Control for each path • Programmable Low Noise Amplifier • Fully Differential • SPI Interface
Manufacturing	• Austria Micro Systems

Transmission & Reception Mode



Network Performance

Ethernet Throughput in Mbits/sec



Test set-up: Two powerline adapters connected through flat channel attenuators in isolated network. Test software: Chariot (bidirectional data transfer). Equipment: DS2's DW21P reference design (DSS9101 chip) and Devolo AV Easy (INT6300 chip). AC cycle: 60Hz.

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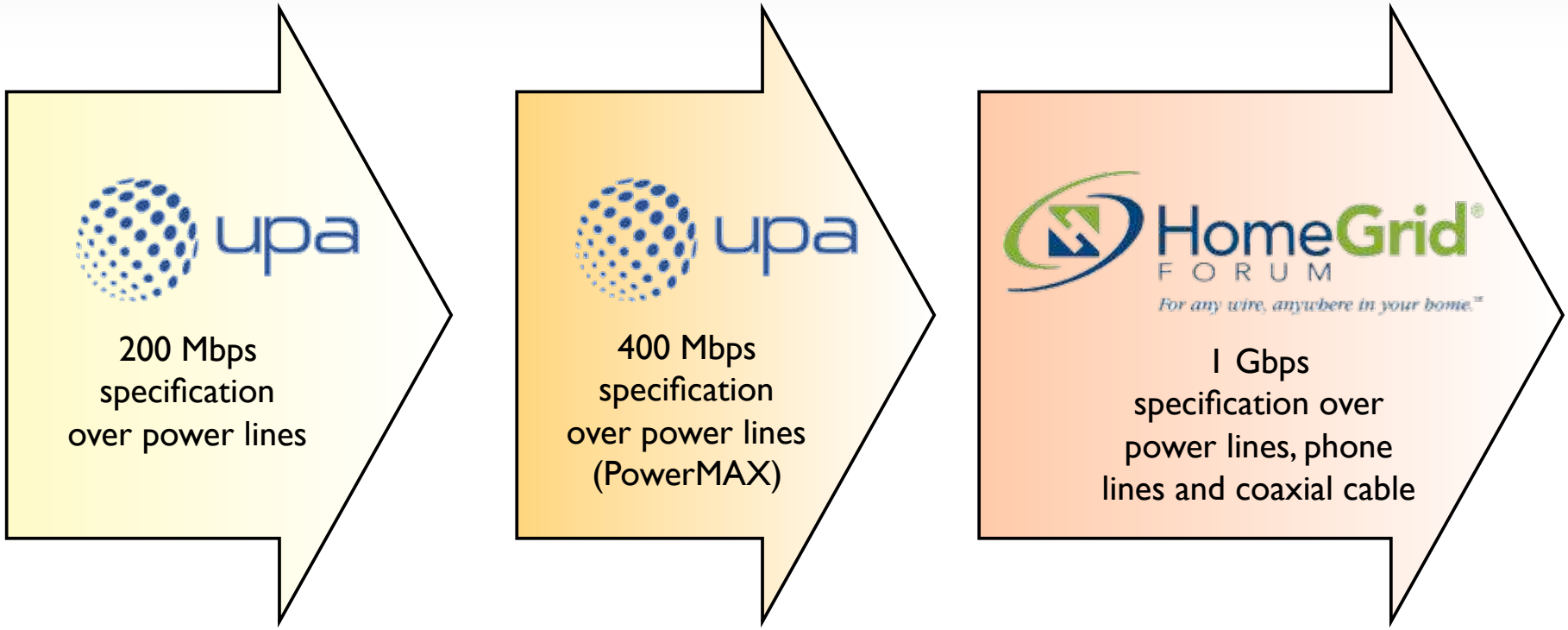
What next?



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