Micro-architecture of Godson-3 Multi-Core Processor

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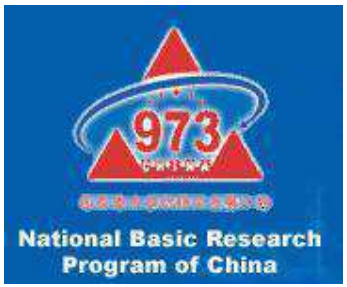
Contents

- **A brief introduction to Godson processors**
- **The architecture of Godson-3 multi-core processor**
- **Physical implementation**
- **PetaFLOPS and TeraFLOPS**

Godson is the academic name of Loongson™

National Project

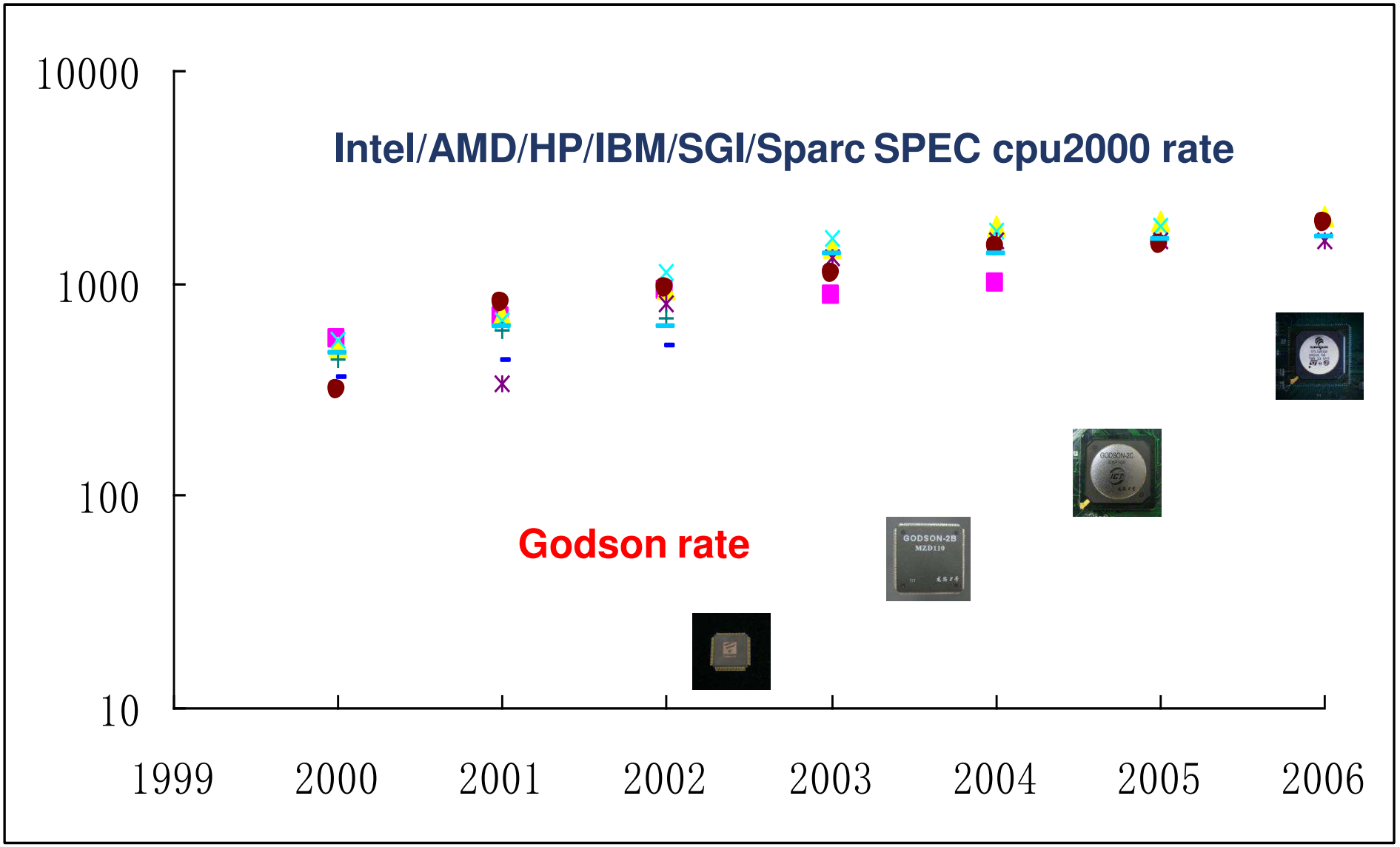
- **High performance CPUs are of national strategic importance**
  - **Chinese ICT industry is growing to a significant scale**
  - **2007 Demand: ICT market = 5.6 trillion RMB**
  - **2007 Supply: only 22% by domestic companies, 3.75% profits**
- **Godson CPU is supported by**
  - **National 863 project**
  - **National 973 project**
  - **National Science Foundation of China**
  - **National key project**
  - **Key project of Chinese Academy of Sciences**



Godson CPU Briefs

- **ICT started Godson CPU design in 2001**
- **The 32-bit Godson-1 CPU in 2002 is the first general purpose CPU in China**
- **The 64-bit Godson-2B in 2003.10**
- **The 64-bit Godson-2C in 2004.12**
- **The 64-bit Godson-2E in 2006.03**
- **Each tripled the performance of its previous one**

Godson Development



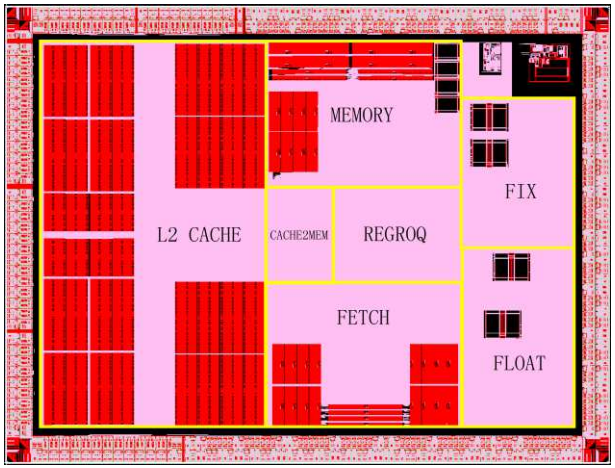
Godson-2E SPEC CPU2000 Rate

Programs	Reftime	Run time	Ratio
164.gzip	1400	403	347
175.vpr	1400	273	512
176.gcc	1100	221	497
181.mcf	1800	307	586
186.crafty	1000	167	598
197.parser	1800	472	382
252.eon	1300	188	690
253.perlbmk	1800	354	508
254.gap	1100	240	458
255.vortex	1900	263	722
256.bzip2	1500	365	411
300.twolf	3000	645	465
SPEC int2000			<503>

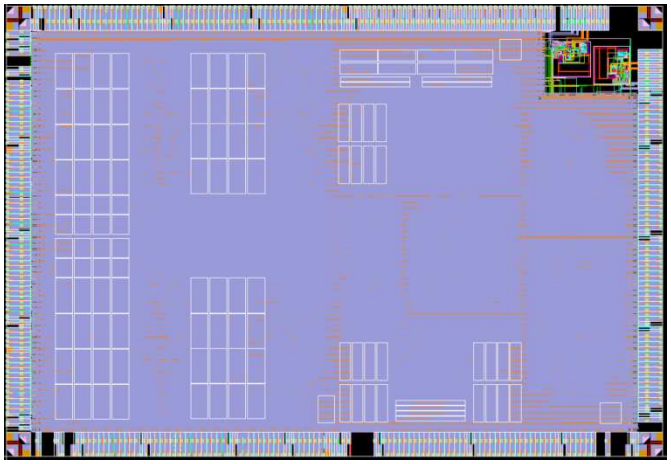
Programs	Ref time	Run time	Ratio
168.wupwise	1600	238	672
171.swim	3100	660	469
172.mgrid	1800	579	311
173.applu	2100	549	382
177.mesa	1400	221	634
178.galgel	2900	412	704
179.art	2600	416	624
183.equake	1300	208	624
187.facerec	1900	300	632
188.ammp	2200	432	509
189.lucas	2000	396	506
191.fma3d	2100	531	395
200.sixtrack	1100	345	319
301.apsi	2600	528	493
SPEC fp2000			<503>

Godson-2E and Godson-2F

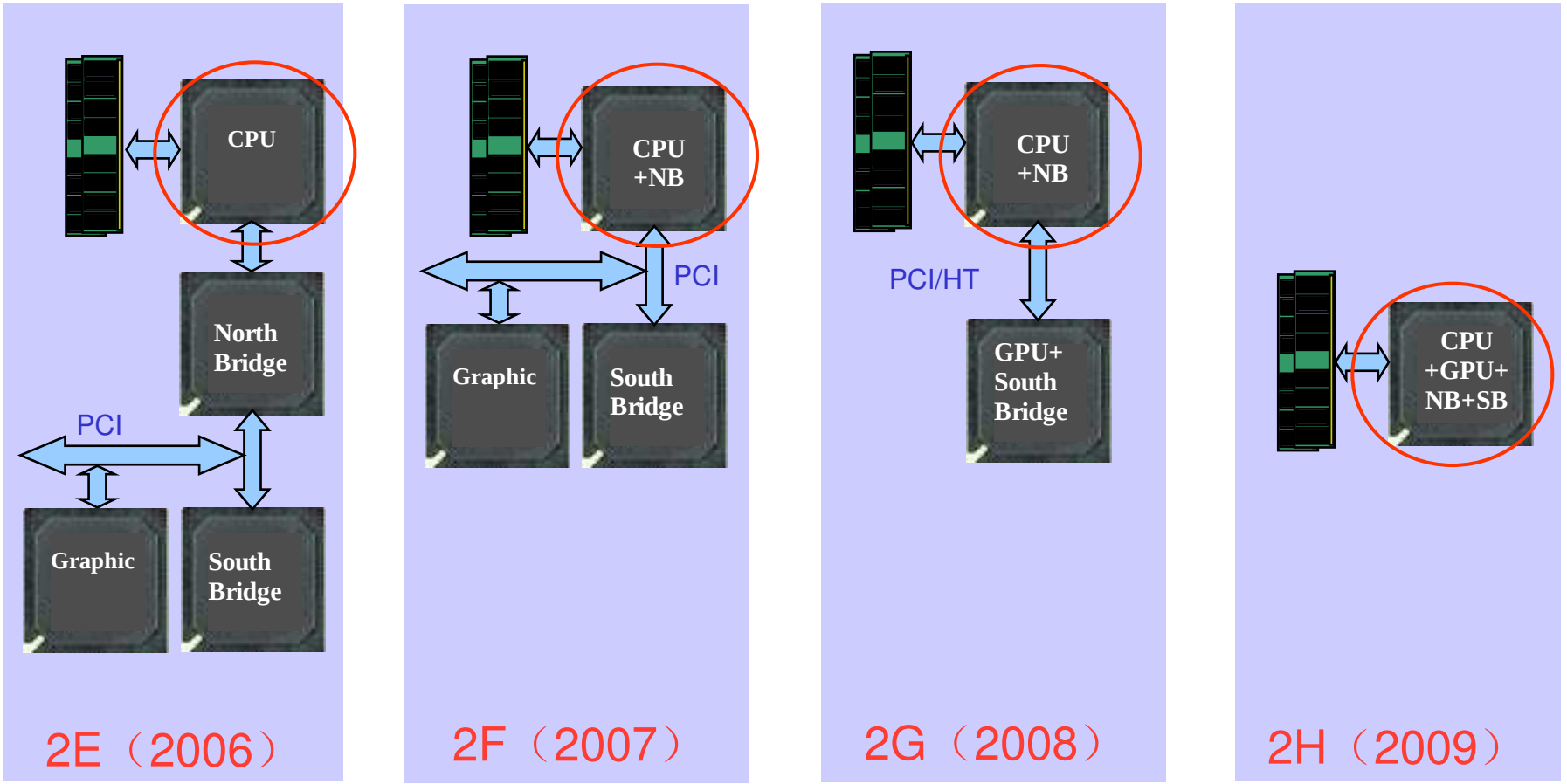
- 1.0GHz@90nm CMOS, 5-7W
- 47M xtors, area 36mm^2
- Godson-2 CPU core
  - 64-bit MIPS III compatible
  - Four-issue, OOO
  - 64KB+64KB L1 (four-way)
  - 512KB L2 (four-way)
- On-chip DDR controller
- SysAD Front-end bus



- 1.0GHz@90nm CMOS, 3-5W
- 51M xtors, area 43mm^2
- Godson-2 CPU core
  - 64-bit MIPS III compatible
  - Four-issue, OOO
  - 64KB+64KB L1 (four-way)
  - 512KB L2 (four-way)
- On-Chip DDR2 controller
- PCI/PCIX, local IO, GPIO, etc.
- Volume production



Low end roadmap: From CPU to SOC



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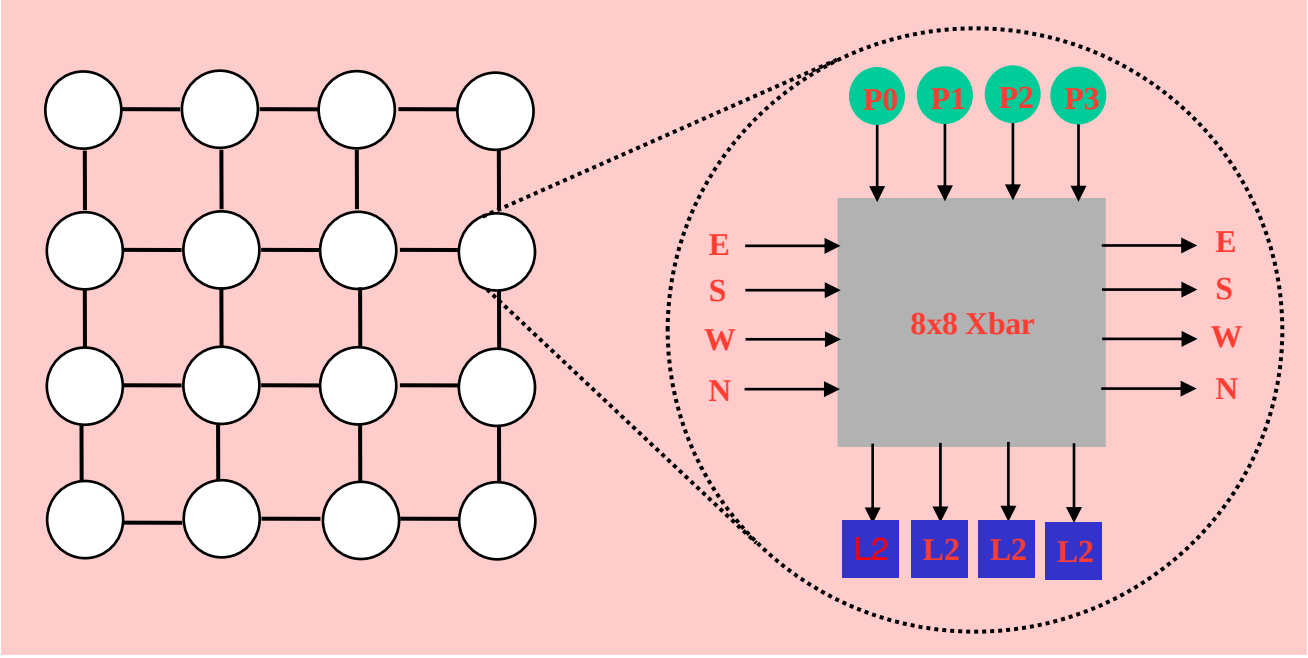
Godson-3 Briefs

- **Scalable architecture**
- **Reconfigurable CPU core and L2**
- **X86 binary translation optimization**
- **Low power consumption**
- **>1.0GHz@65nm**

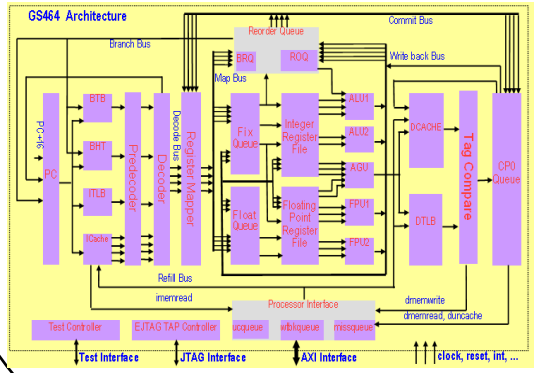
Scalable Architecture Design

- **Scalable interconnection network**
  - **Crossbar + Mesh**
  - **Single crossbar connects cores, L2s, and four directions**
- **Directory-based cache coherence protocol**
  - **Distributed L2 caches are globally addressed**
  - **Each cache block has a directory entry**
  - **Both data cache and instruction cache are recorded in directory**



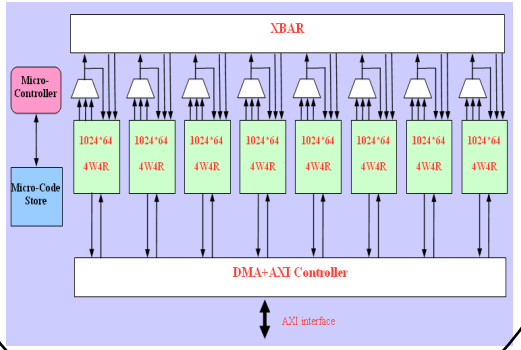
Reconfigurable Architecture

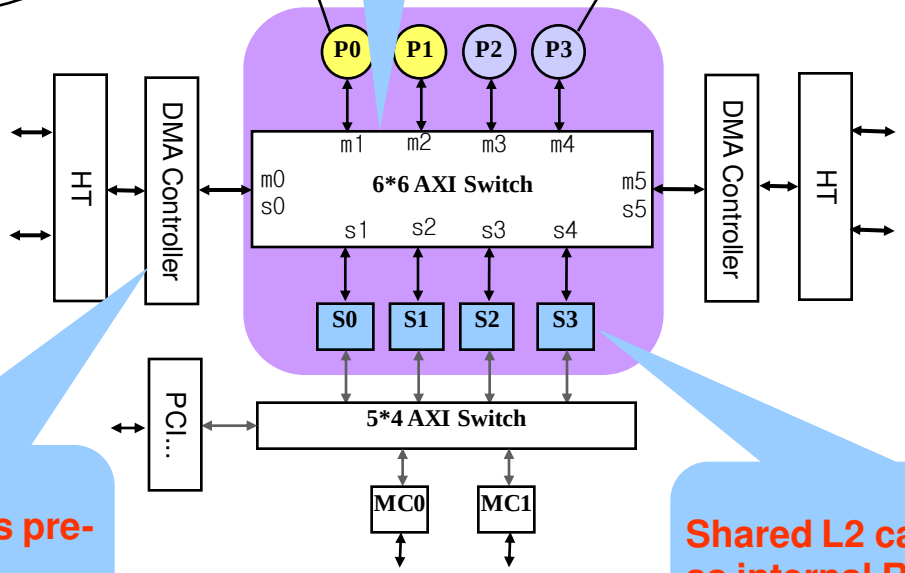
General Purpose Core: 64-bit, 4-issue, OOO, AXI interface



8 configurable address windows of each master port allow pages migration across L2 and memory

Multiple Purpose Core: LINPACK, biology, signal processing, AXI interface





DMA engine supports pre-fetch and matrix transpose

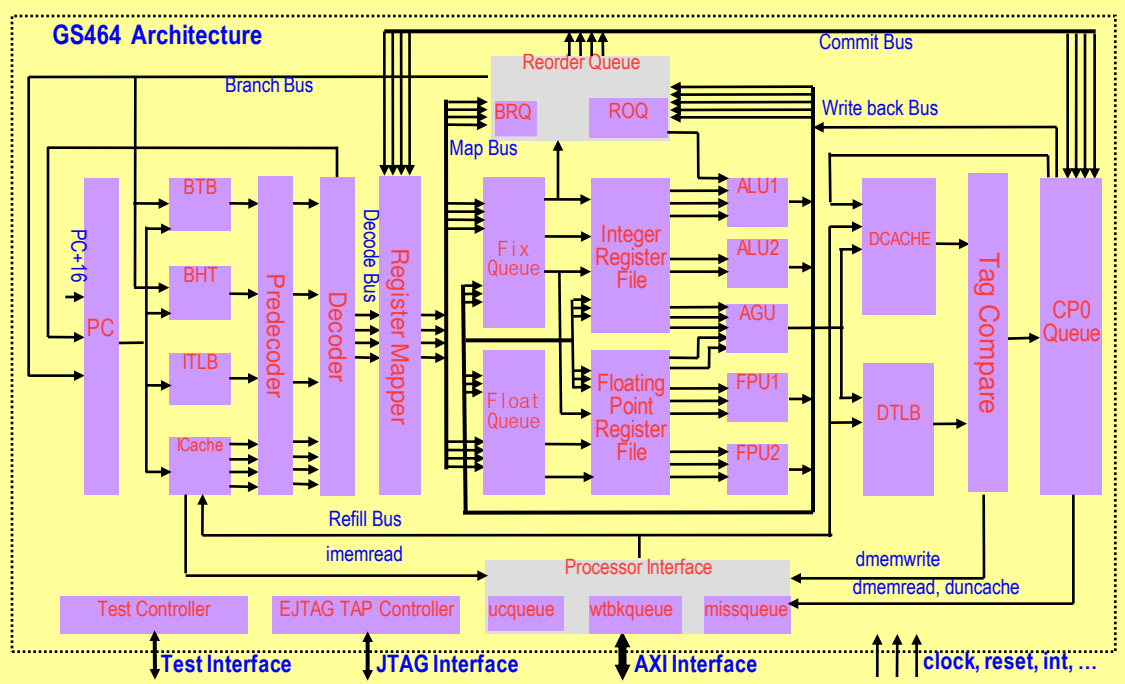
Shared L2 can be configured as internal RAM; DMA to internal RAM directly

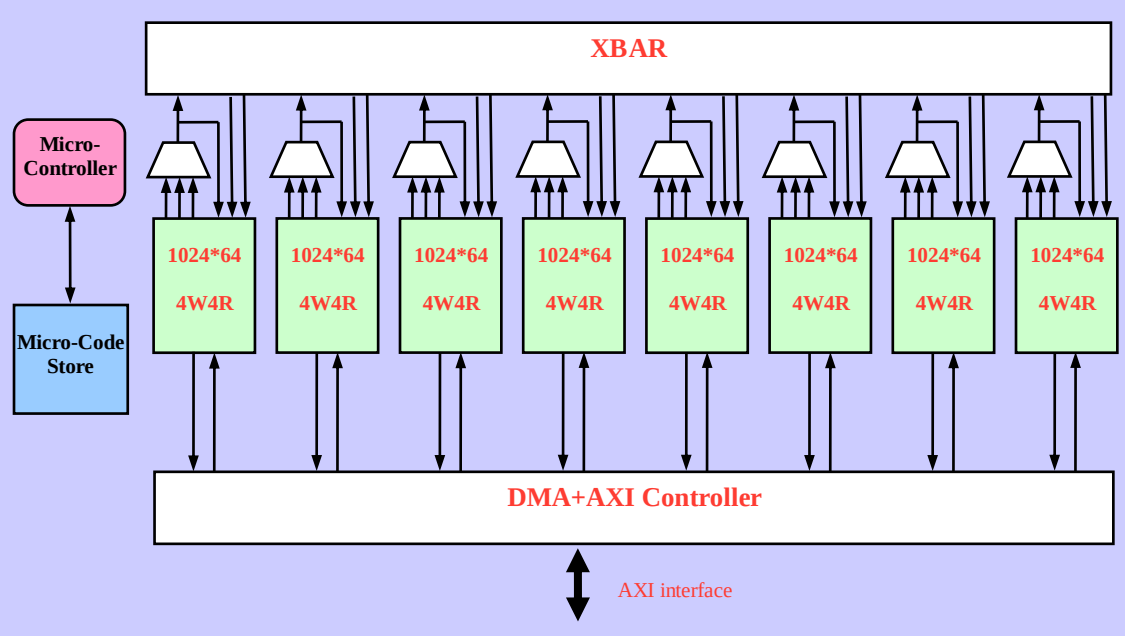
GS464 general purpose core

- MIPS64, 200+ more instructions for X86 binary translation and media acceleration
- Four-issue superscalar OOO pipeline
- Two fix, two FP, one memory units
- Two FP units each supports full pipelined double/paired-single MAC operation
- 48-bit VA and PA, 128-bit memory access
- 64KB icache and 64KB dcache, 4-way
- 64-entry fully associated TLB, 16-entry ITLB, variable page size
- Non-blocking accesses, load speculation
- Directory-based cache-coherence for CMP
- Parity check for icache, ECC for dcache
- EJTAG for debugging
- Standard 128-bit AXI interface

GStera multiple purpose core

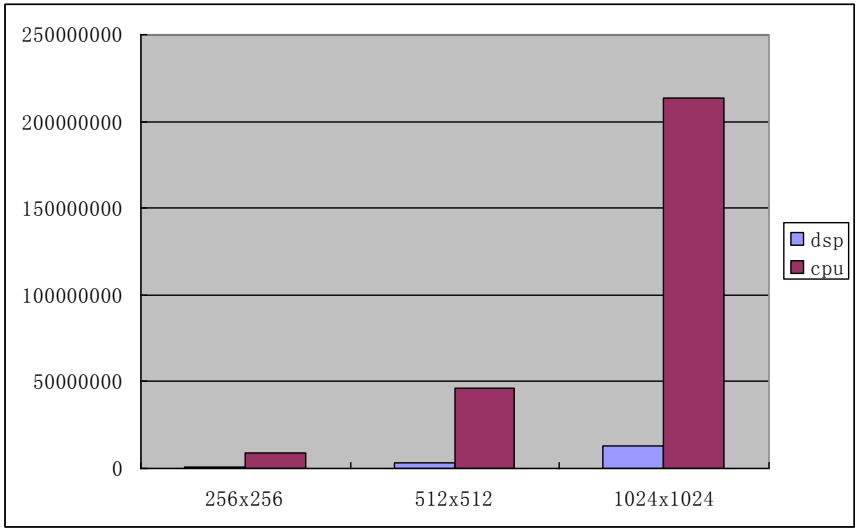
- Target for LINPACK, biology computation, signal processing
- 8-16 MACs per node
- Big multi-port register file
- Reconfigurable based on applications.
- Standard 128-bit AXI interface





Matrix Transposing Performance

- **15+times faster**



Hardware Support for X86 Binary Translation

- **Define new instructions**
  - **X86 ISA function and MIPS ISA format**
  - **Binary translation mechanism supporting**
  - **>200 instructions are defined with 5% additional silicon cost**
- **Speed up X86-to-MIPS binary translation**
  - **10 times compared to software only QEMU**

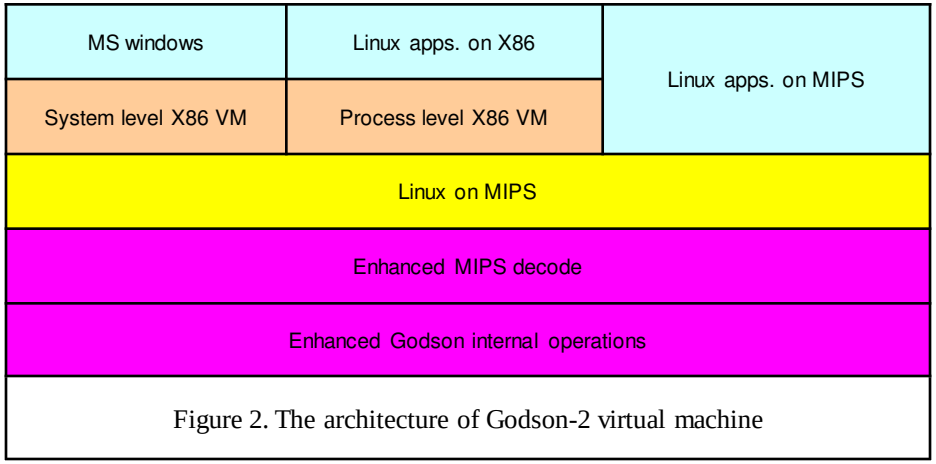
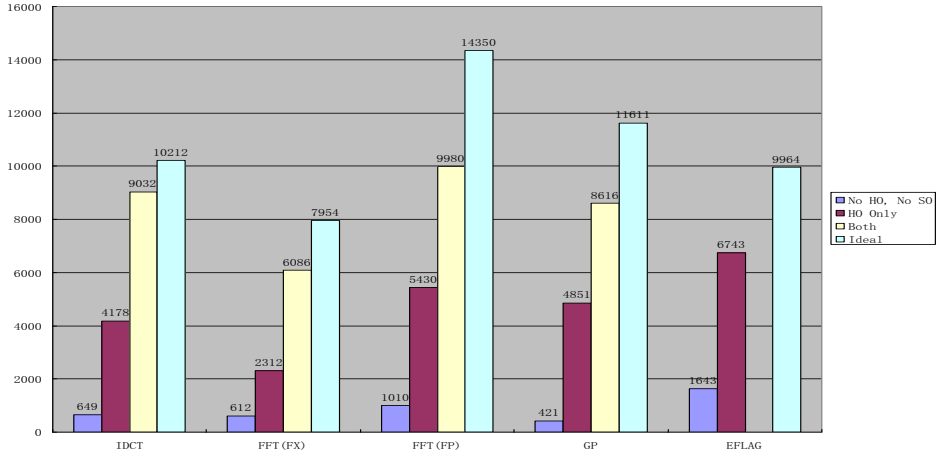


Figure 2. The architecture of Godson-2 virtual machine



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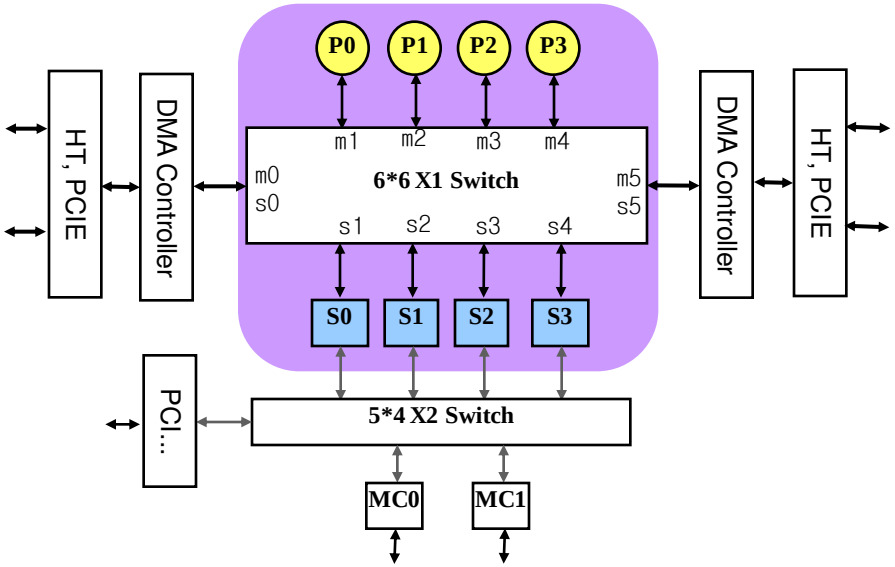
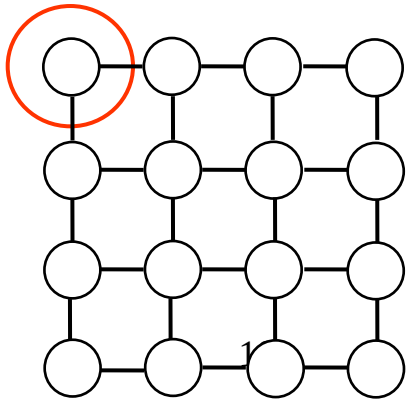
Physical implementation

- **65nm CMOS LP/GP technology**
- **Cell-based design methodology**
  - **DC + ICC**
  - **Manual P&R for critical cells**
- **2008: 4-core (4GP + 0MP) + 4MB L2**
  - **GP: General purpose core**
  - **MP: Multiple purpose core**
  - **10w@1GHz**
- **2009: 8-core (4GP + 4MP) + 4MB L2**
  - **20w@1GHz**

4-core

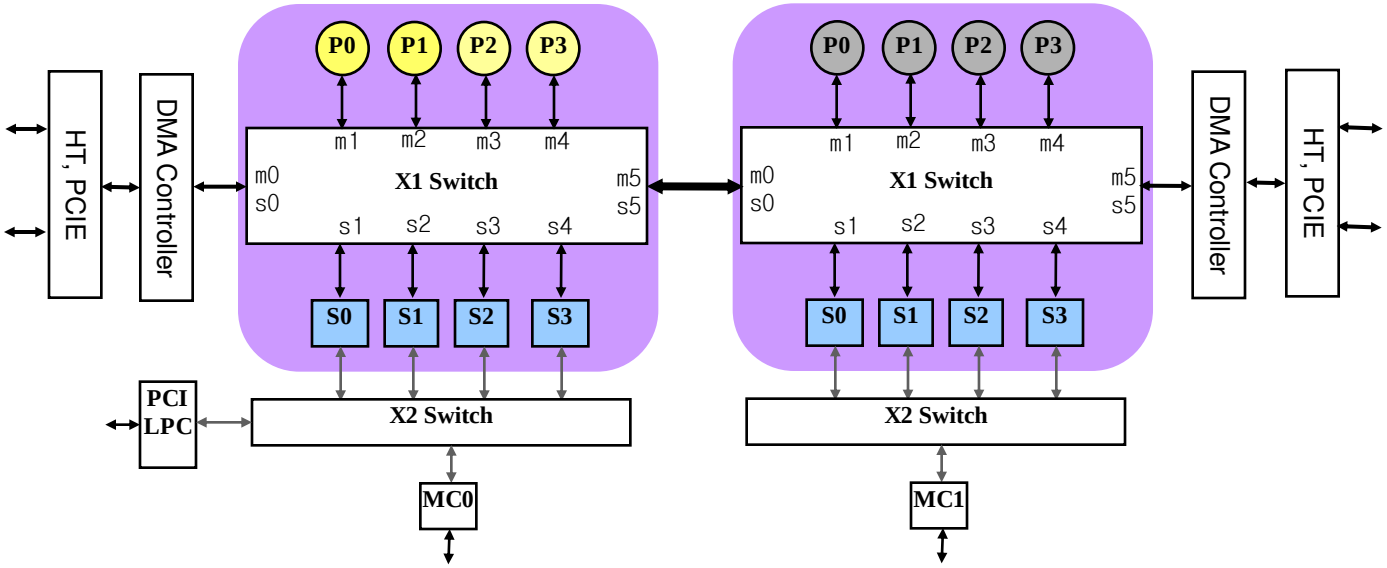
- **2008**
  - **4-core (general purpose core)**
  - **65nm, 1GHz, 10w**

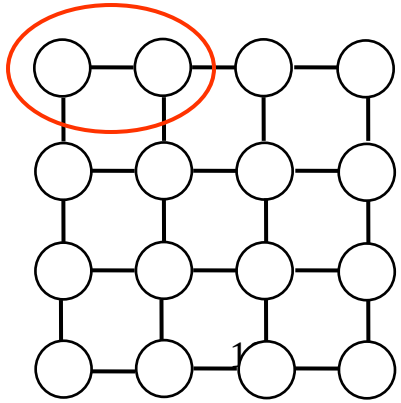




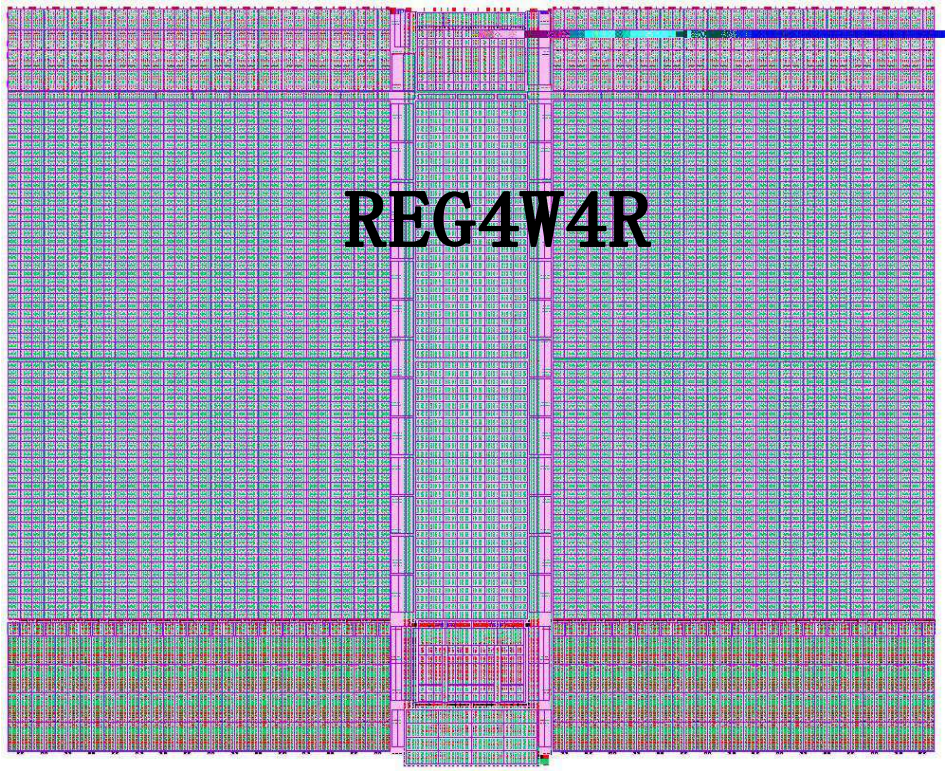
8-core

- **2009**
  - **8-core (4GP + 4MP)**
  - **65nm, 1GHz, 20w**





Full Customer Register file and CAM

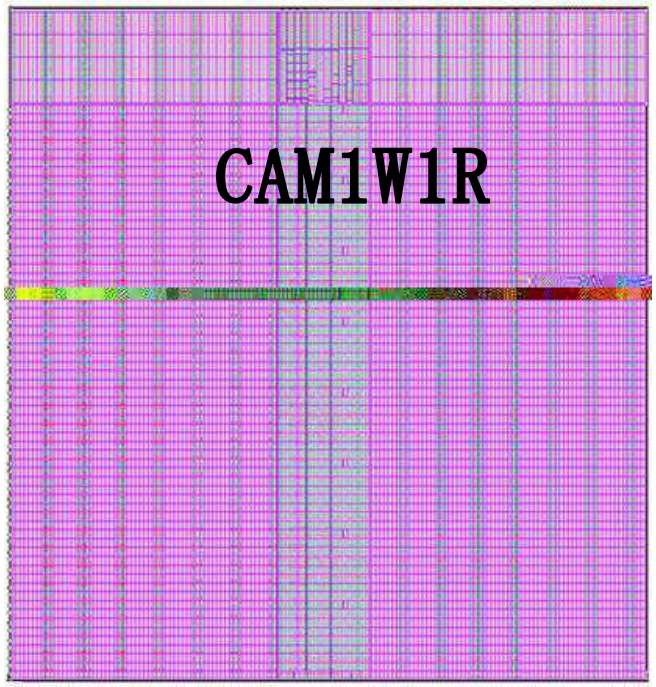


Physical register file

Size: 321um x 262um

Power: 50mW@1GHz

Delay: 470ps



TLB CAM

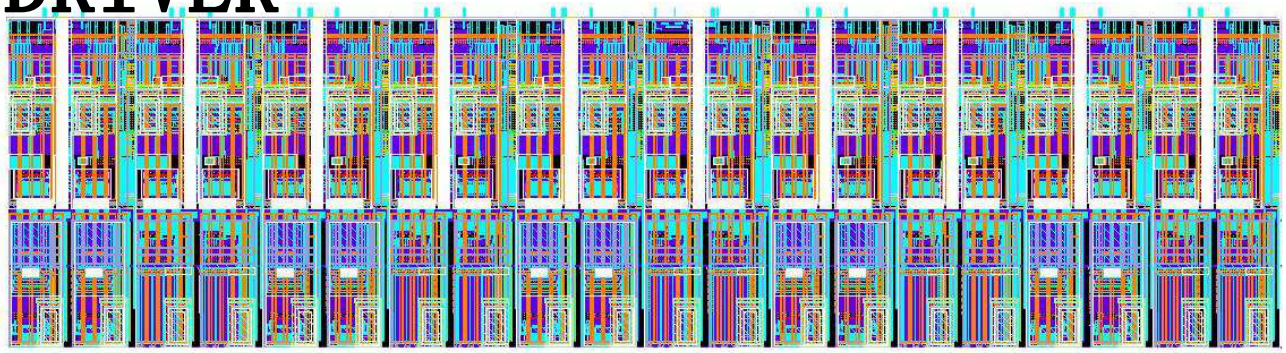
Size: 224 um x 235 um

Power: 55mw @ 1GHz

Delay: 550ps

HyperTransport PHY

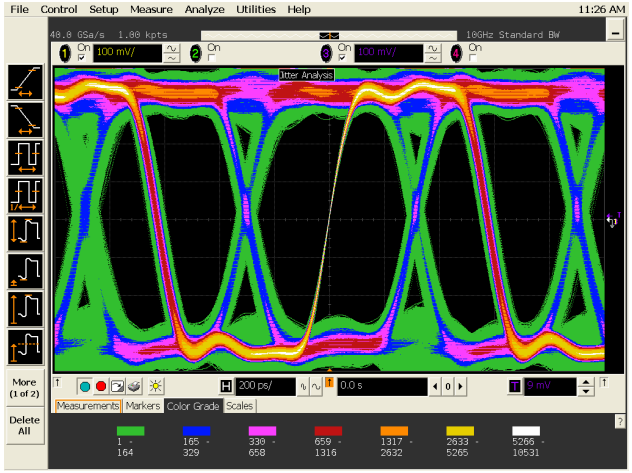
DRIVER



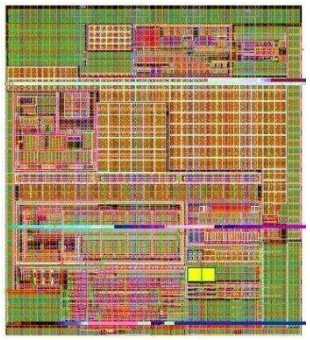
HT1.0 Driver & Receiver

FlipChip Compatible 2Row design

800mw @ 1.6Gbps



PLL



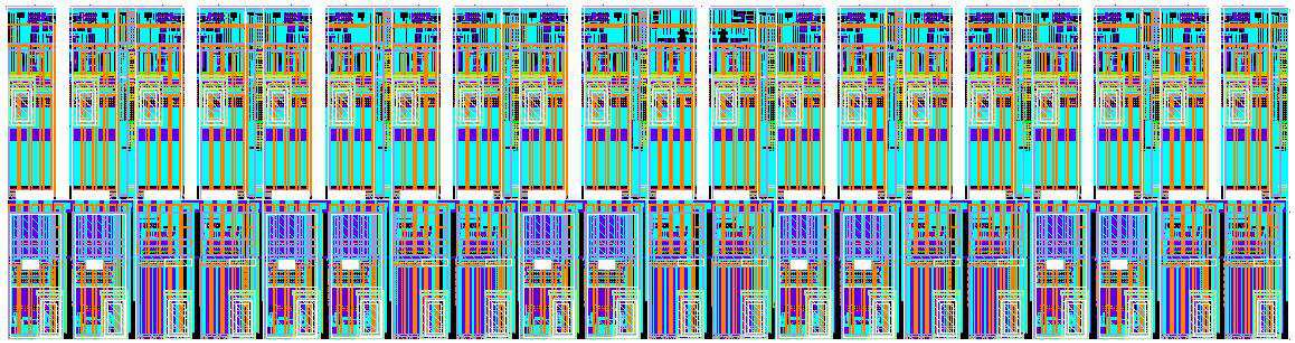
Size: 250um x 300um

Power: < 10mW

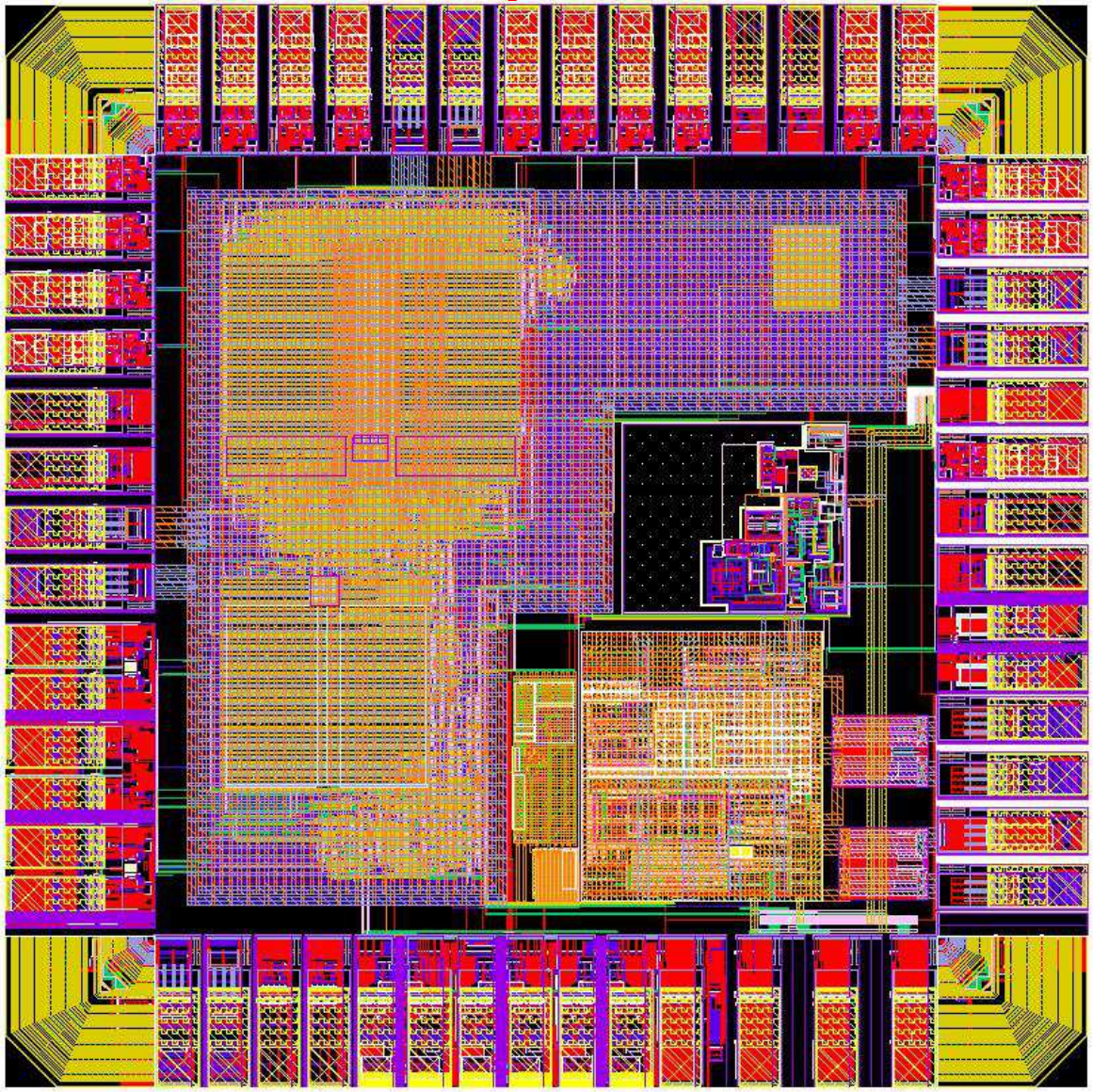
Freq: 1.6GHz

Jitter: 20 ps

RECEIVER



Test Chip for Customer Blocks



TEST CHIP

ST 65nm

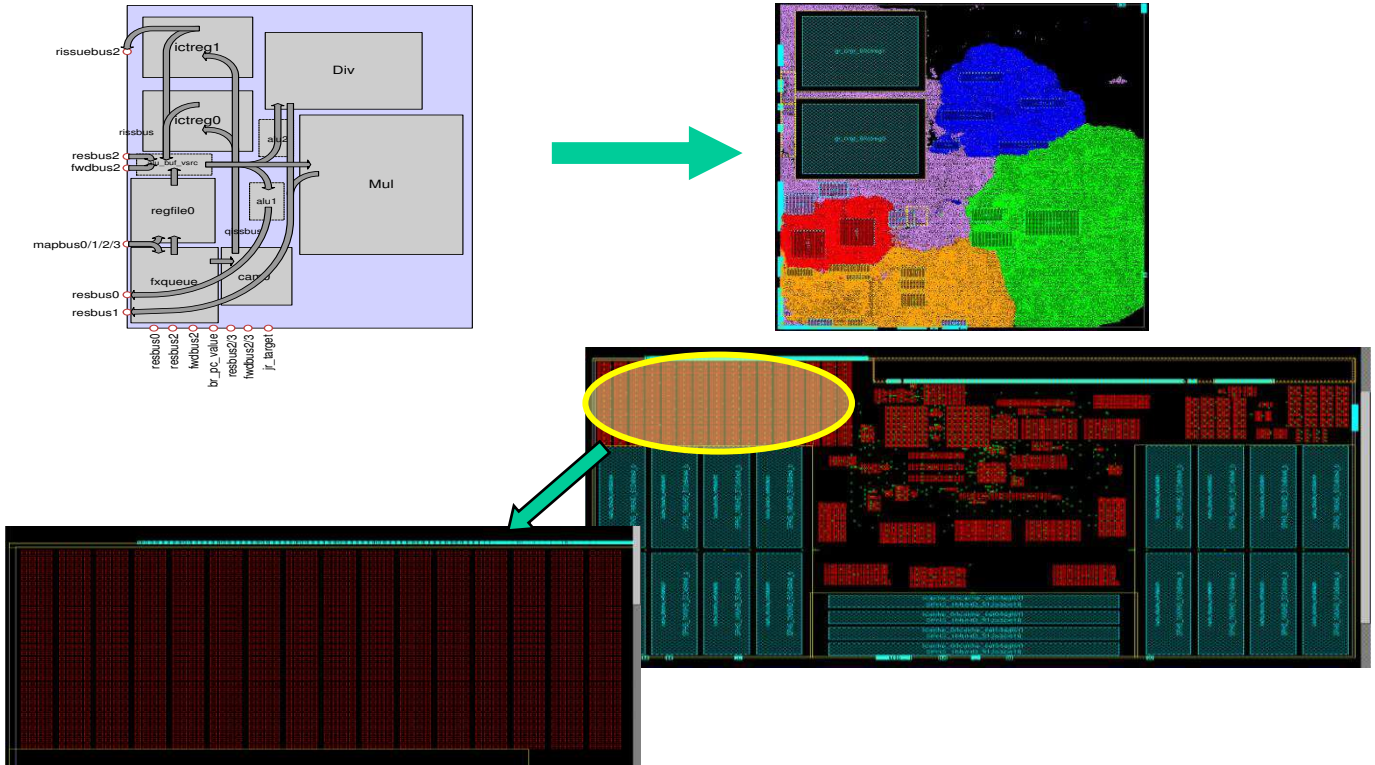
1206um x 1206um

Function:

- **CAM1W1R - BIST**
- **CAM1W1R - Scan**
- **RAM4W4R - BIST**
- **RAM4W4R - Scan**
- **ICT_PLL - Freq. test**
- **HT1.0 - BIST**
- **HT1.0 - Error rate test**

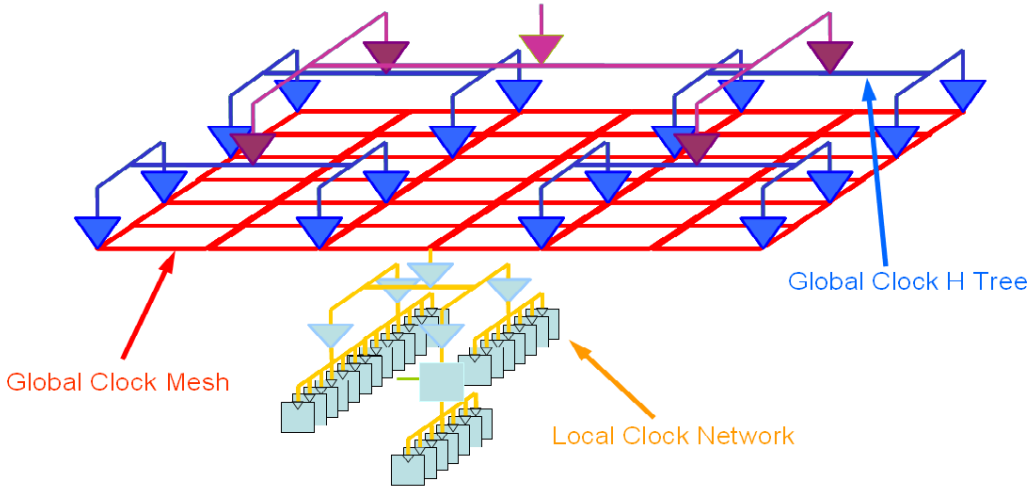
Cell-based High Performance Physical Design

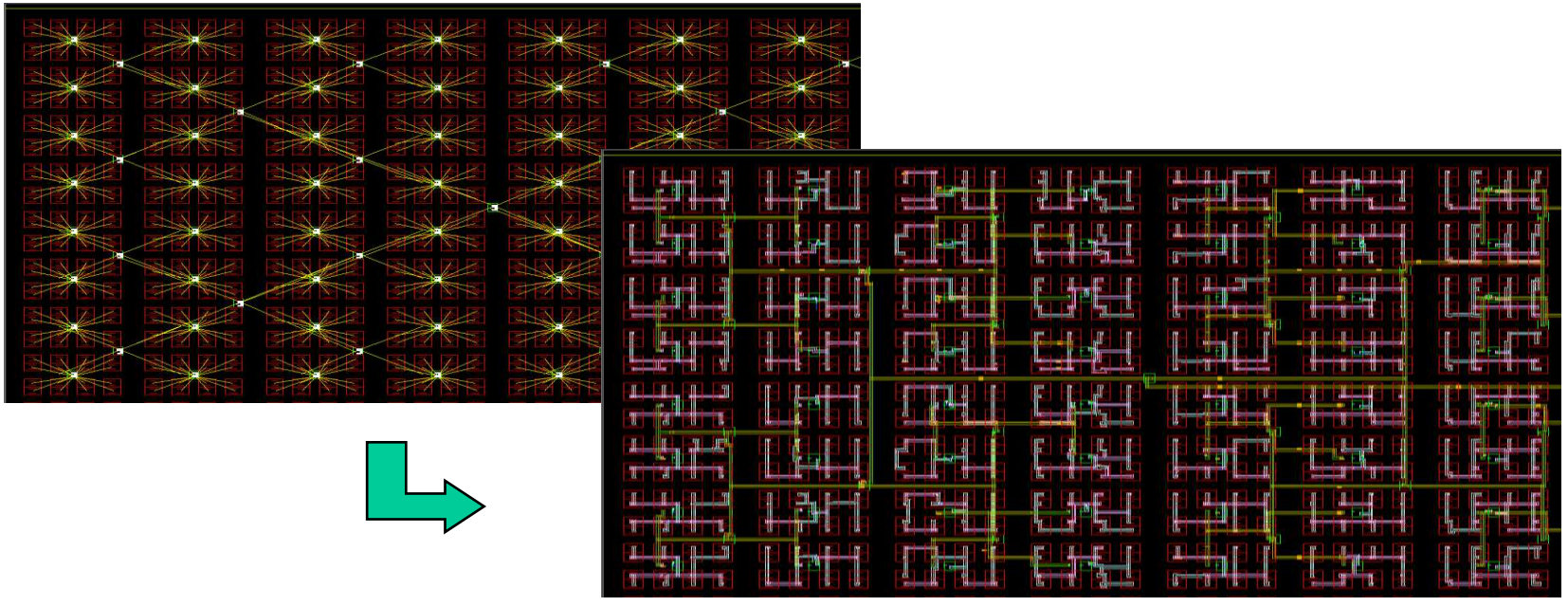
- **The Full Hierarchical Design Methodology**
- **Manual placement & route for critical paths**
- **Manual placement of all FFs and clock buffers, manual clock gating**
- **Architecture optimization with physical feedback**



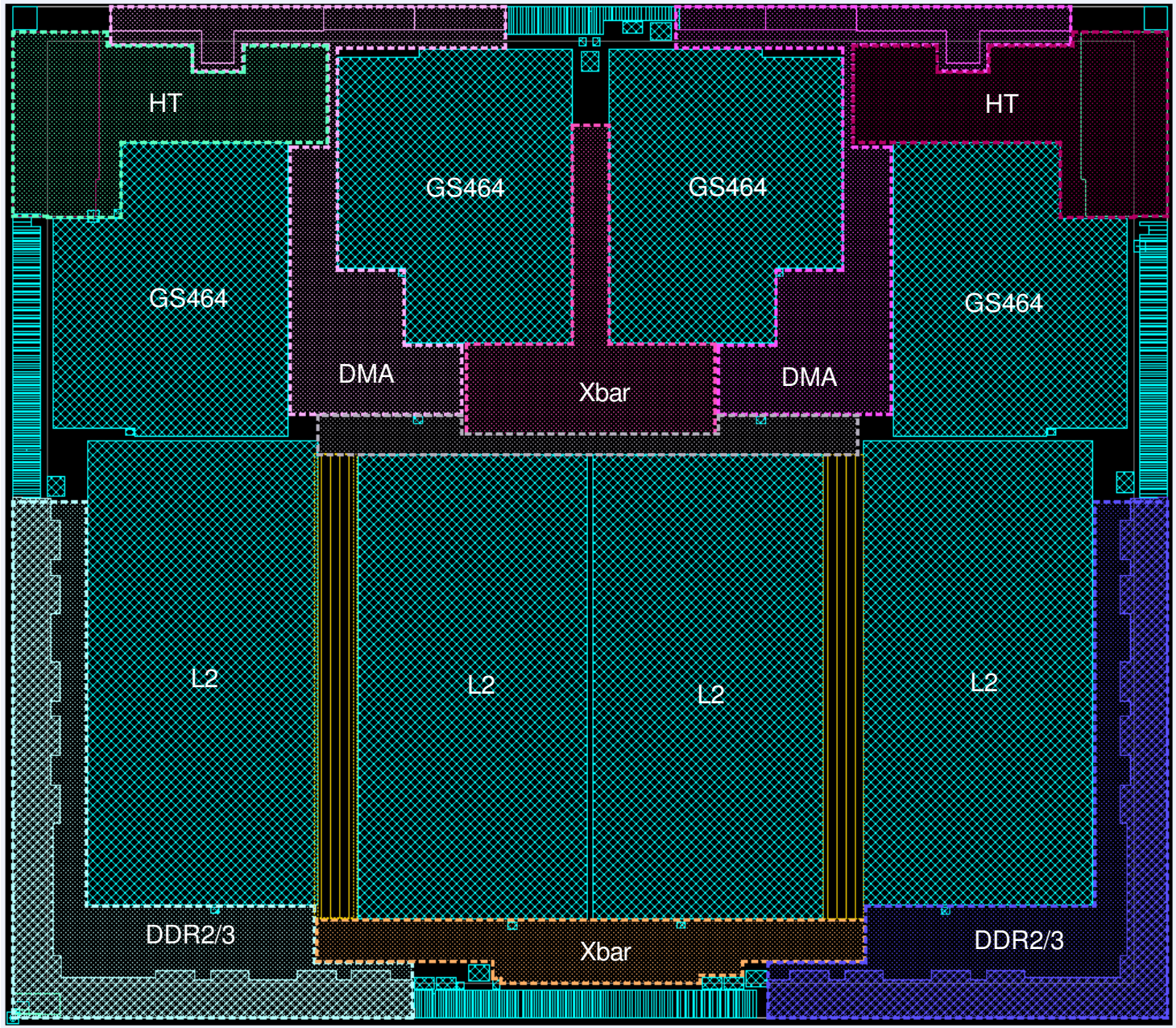
Clock Tree

- **H-Tree + Mesh**
- **Manual placement of FFs**
- **Manual clock gate**





Layout of 4-core Godson-3



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PetaFLOPS and TeraFLOPS

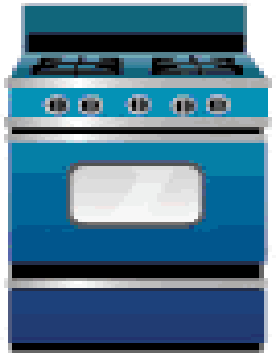
- **PetaFLOPS for Large Scale Applications**
  - **To build PetaFLOPS HPC with Godson-3 in 2010**
- **TeraFLOPS for Personal HPC**
  - **Putting desktop to pockets**
  - **Putting TeraFLOPS to desktop**
  - **High-performance computing for the masses**

Scaling down TeraFLOPS

TeraFLOPS in 1997

Scaling down

$100K/2007
"refrigerator"



$50K/2008
"washing machine"

$10K/2009
"microwave oven"

References

- **The architecture of Godson-2 superscalar architecture is available at:**
  - **Weiwu Hu, Fuxin Zhang, Zusong Li, "Microarchitecture of the Godson-2 Processor", Journal of Computer Science and Technology, 20(2):243-249, Mar. 2005**
  - **Weiwu Hu, Jiye Zhao, Shiqiang Zhong, Xu Yang, Elio Guidetti, Chris Wu, "Implementing a 1GHz Four-issue Out-of-Order Execution Microprocessor in a Standard Cell ASIC Methodology", Journal of Computer Science and Technology, 22(1):1-14, Jan. 2007**
- **The experiences learning from Godson processor design is available at:**
  - **Weiwu Hu, Jian Wang, "Making Effective Decisions in Computer Architects' Real-World: Lessons and Experiences with Godson-2 Processor Designs", Journal of Computer Science and Technology, 23(4), July 2008**
- **The architecture of Godson-3 multi-core is available at:**
  - **HotChip'08**

Concluding Remarks

- **CPU R&D are of national strategic importance**
- **Godson-3 has a low-power, scalable architecture**
- **Godson-3 will be used to build**
  - **client side systems**
  - **Petaflops machines**
  - **Teraflops systems for the masses**
- **The Godson team at ICT: open cooperation**

Thanks