Stratix IV FPGA and HardCopy IV ASIC @ 40 nm

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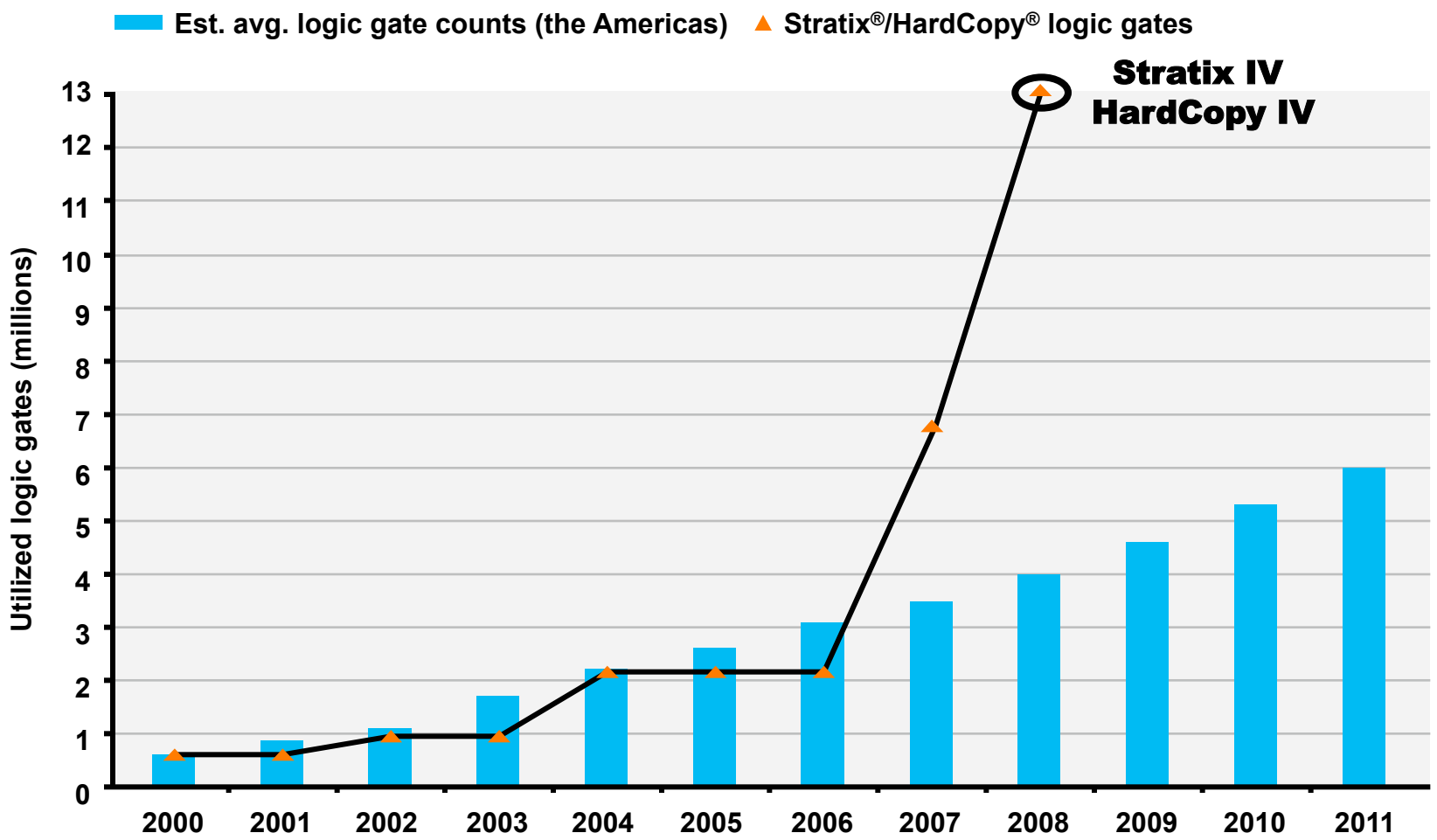
HotChips August 2008

New 40-nm FPGA and ASIC

Stratix IV FPGAs

- 2X logic density
  - Up to 680K logic elements (LEs)
  - Up to 22.4-Mbits internal RAM
  - Up to 1,360 18x18 multipliers
- More performance and 2X bandwidth
  - Up to 48 transceivers operating up to 8.5 Gbps
  - Up to 4 x8 hard intellectual property (IP) blocks for PCI Express Gen1 and Gen2
  - Up to 748 GMACS
- Half the power
  - Programmable Power Technology
  - Quartus® II PowerPlay technology
  - 40-nm process benefits including 0.9V core voltage

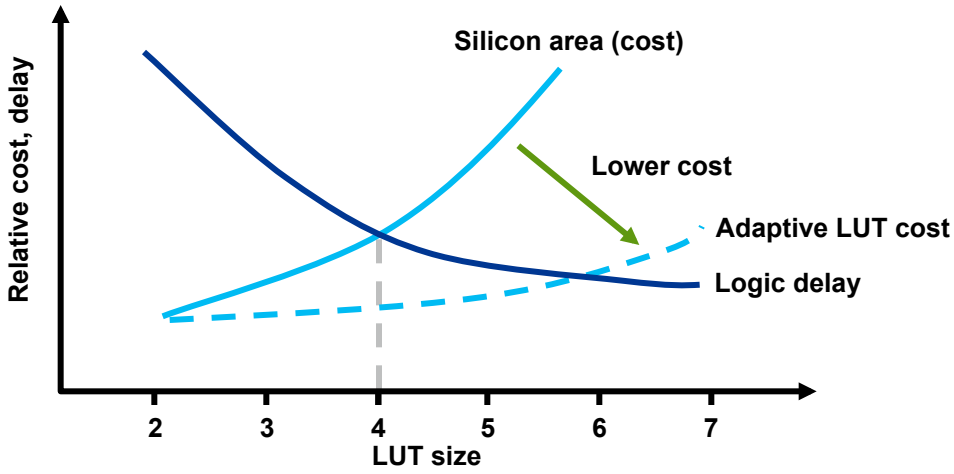
Significant Increase in Capability



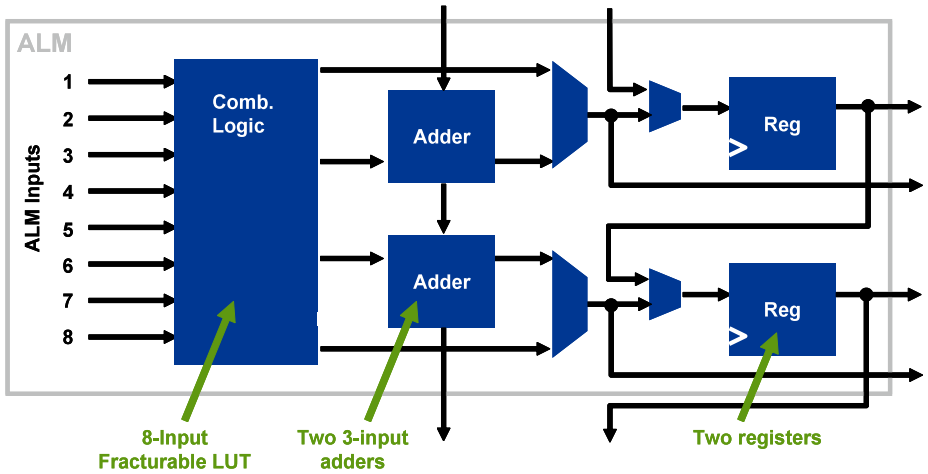
Note: Data based on Gartner Dataquest report 11/21/07

Logic Architecture

Why adaptive logic module (ALM)?

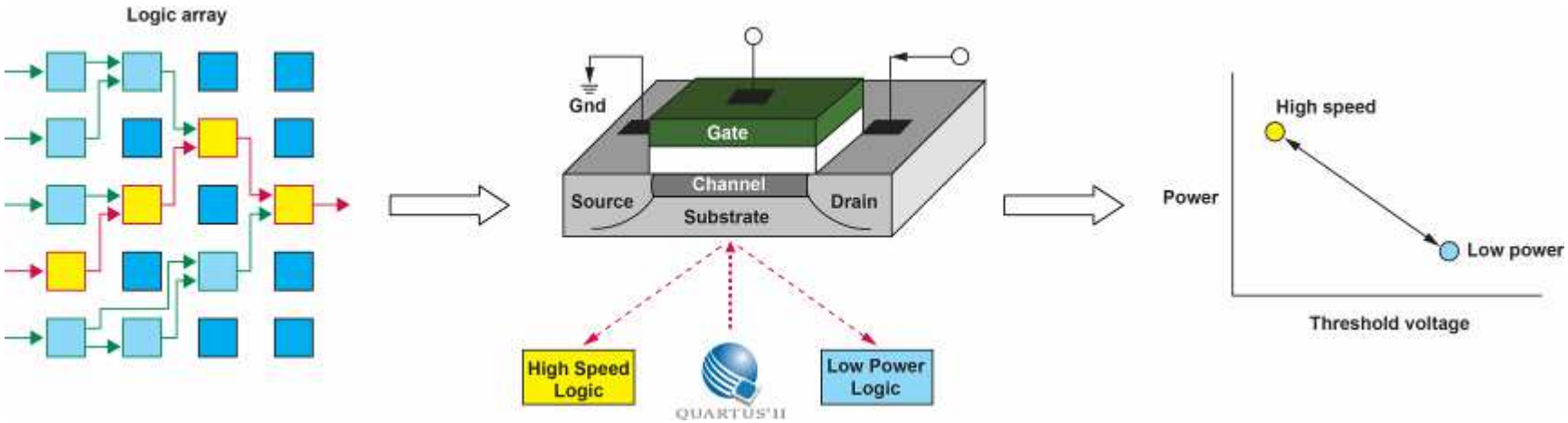


What is ALM?

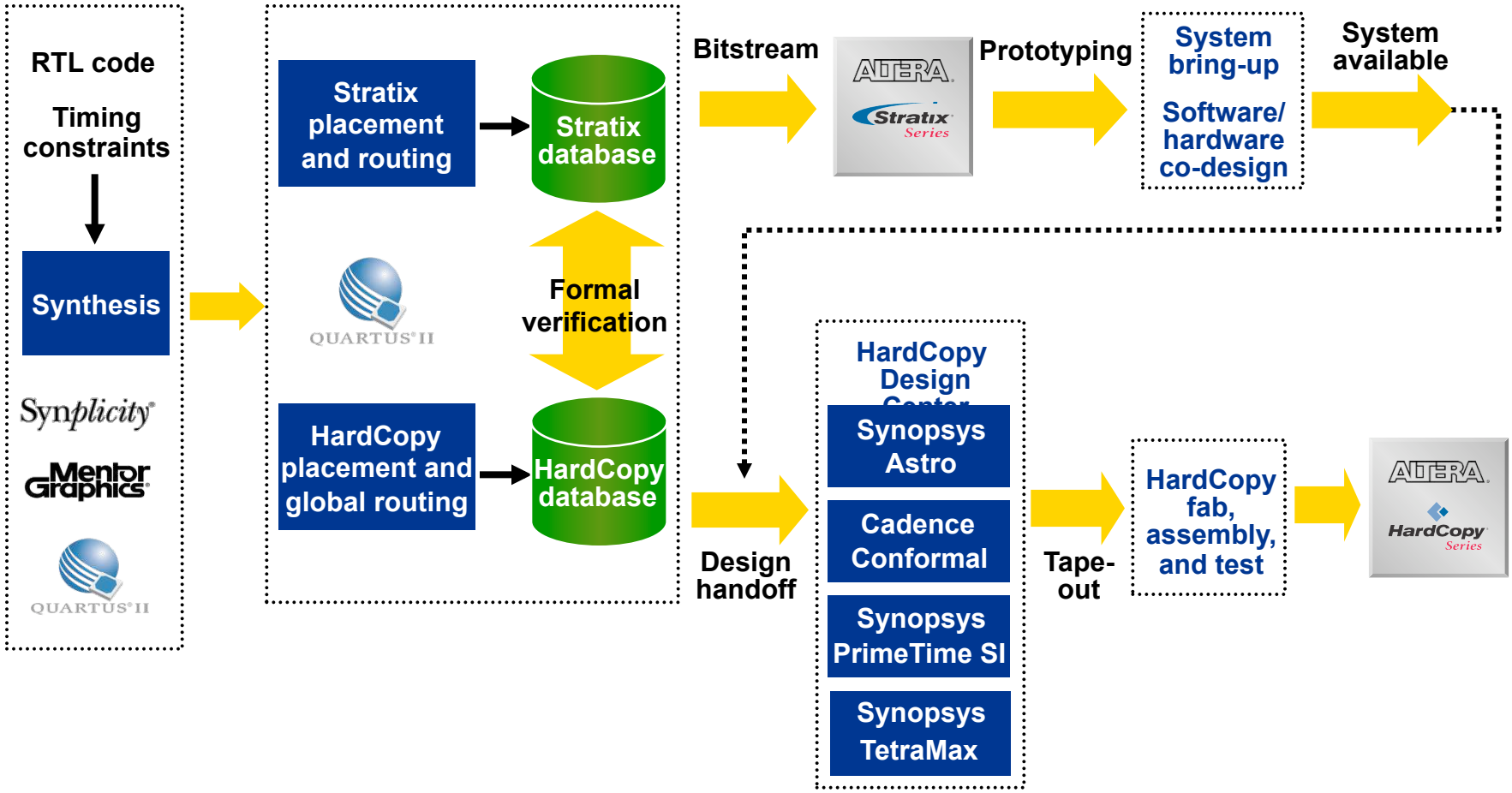


Programmable Power Technology

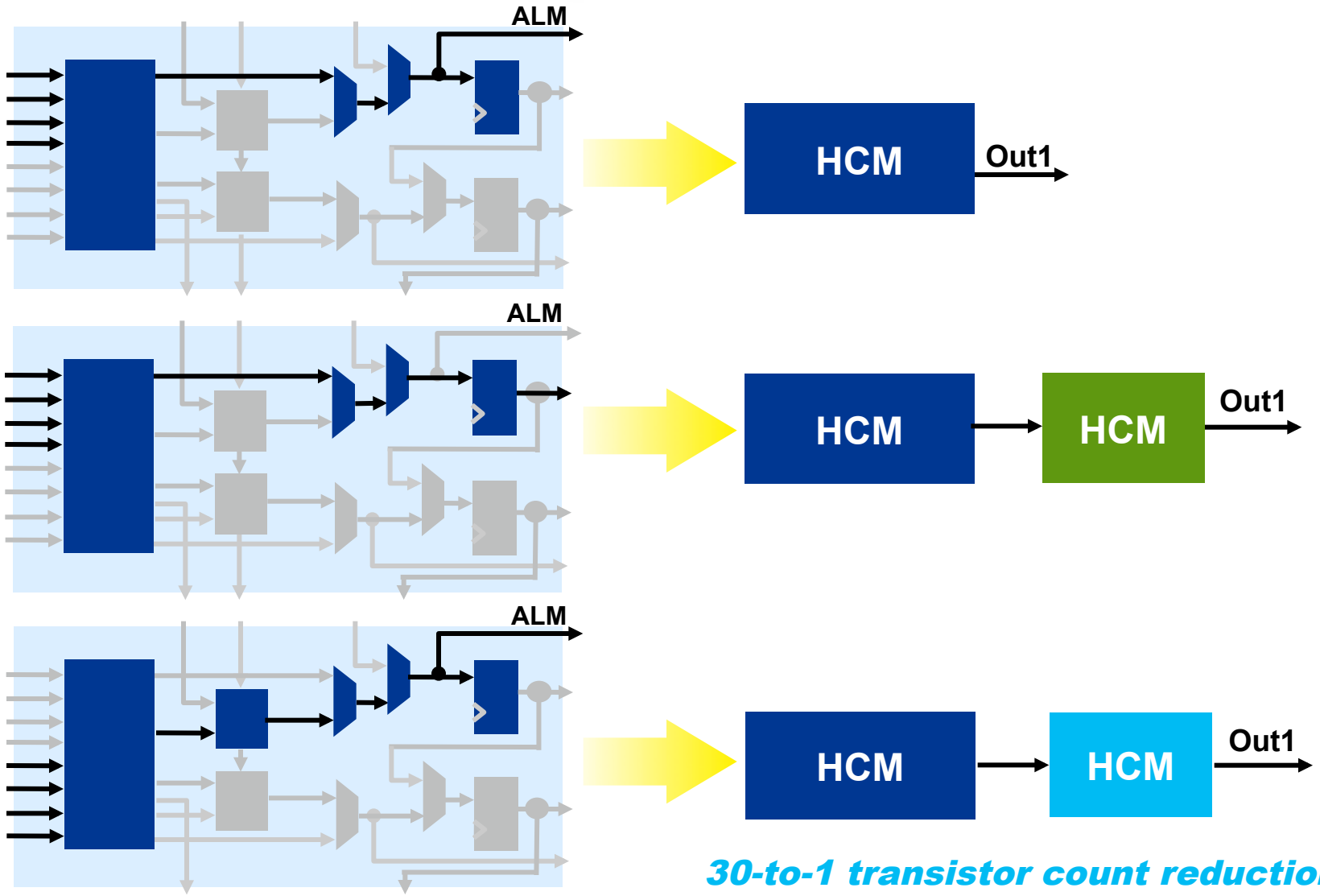
- 40-nm process benefits
  - Triple-oxide, lower, and multiple core voltages…
- FPGA specific: design specific and adaptive



HardCopy/Stratix Design Flow



FPGA to HardCopy ASIC



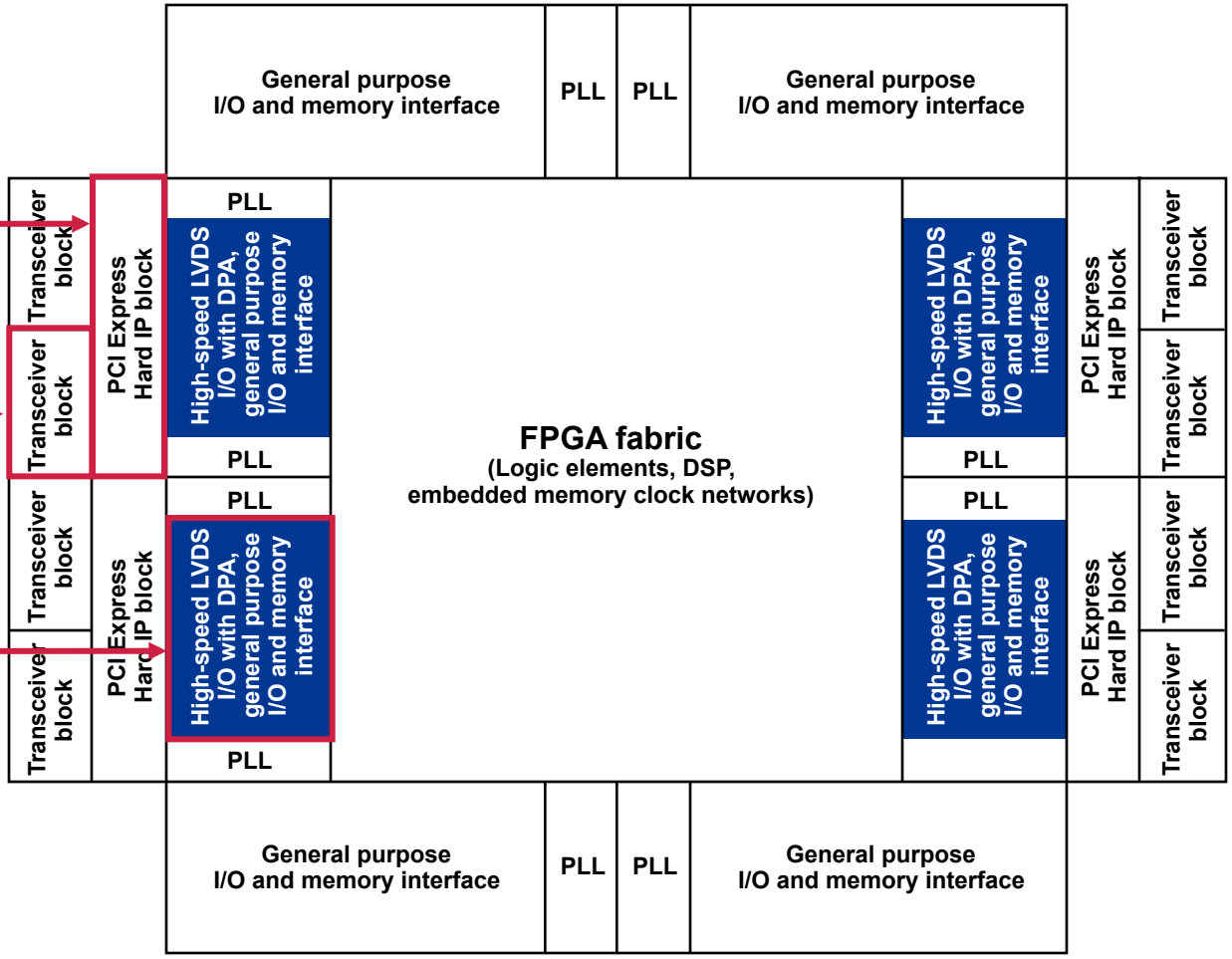
30-to-1 transistor count reduction!

Transceivers and User I/O

PCI Express hard IP blocks

Transceiver block, with four 8.5 Gbps transceivers and two 3.2 Gbps transceivers

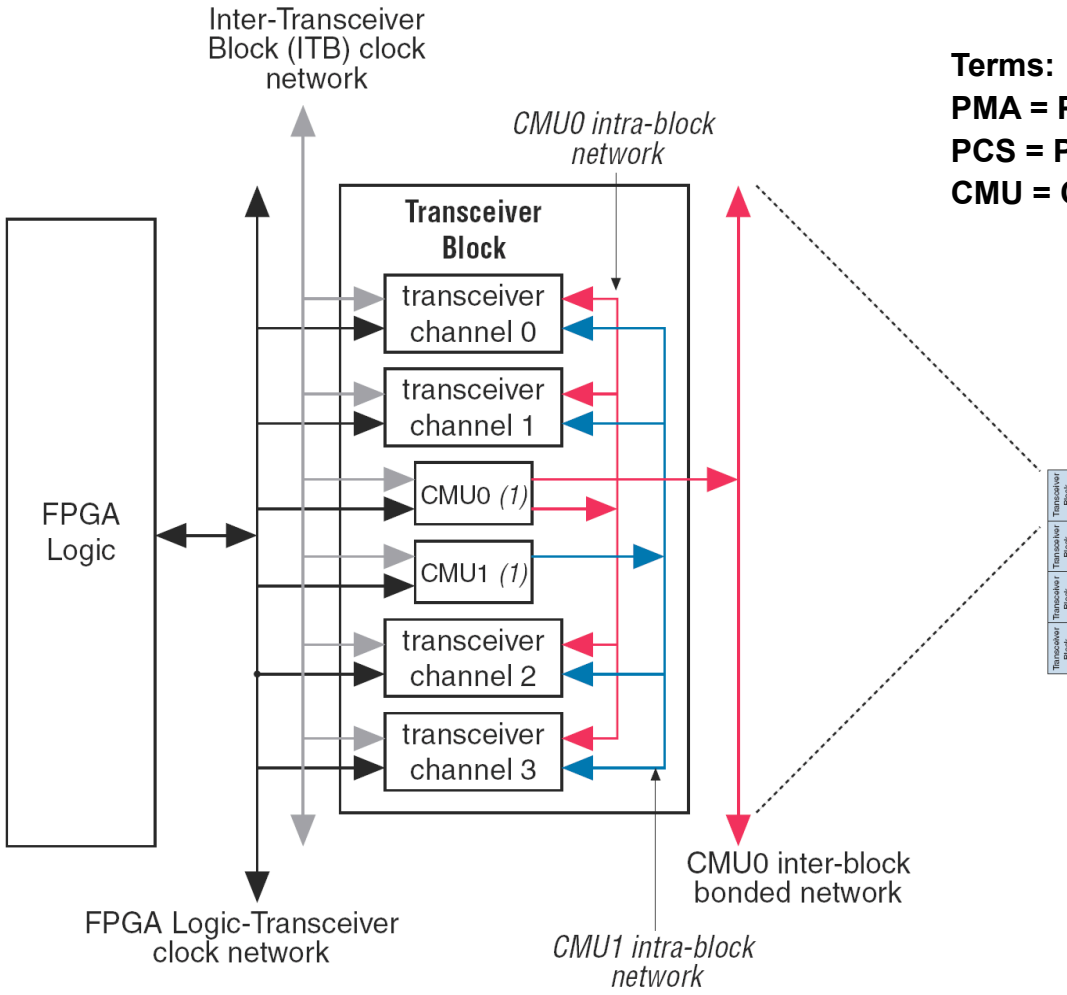
High-speed LVDS I/O banks with DPA capability

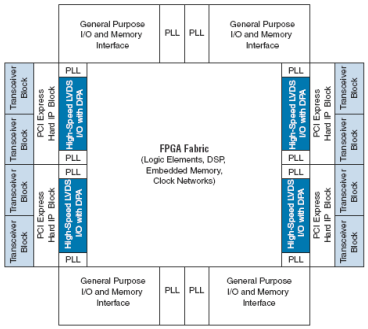


Transceiver Protocols

Protocol	HardCopy IV ASICs	Stratix IV FPGAs
3G Protocols		
PCI Express Gen1 (x1, x2, x4, x8), PCI Express Cable	✓	✓
Serial RapidIO® (1x, 4x)	✓	✓
Gigabit Ethernet, XAUI (IEEE 802.3ae), HiGig+	✓	✓
3G Basic (proprietary), 3G SerialLite II	✓	✓
CPRI v3.0, OBSAI v2.0/RP3-01 v4.0	✓	✓
SONET OC-3/12/48, GPON	✓	✓
SATA, SAS	✓	✓
SD, HD, and 3G SDI, ASI	✓	✓
Serial Data Converter (JESD204)	✓	✓
SFI 5.1	Up to 8 channels	✓
HyperTransport 3.0	Up to 8 channels	✓
6G Protocols		
PCI Express Gen2 (x1, x2, x4, x8)	✓	✓
HiGig2, CEI 6G (SR/LR), Interlaken, DDR-XAUI, SPAUI	✓	✓
6G basic (proprietary), 6G SerialLite II	✓	✓
6G CPRI/OBSAI	✓	✓
Fibre Channel (FC1/FC2/FC4)	✓	✓

Transceiver





Terms:

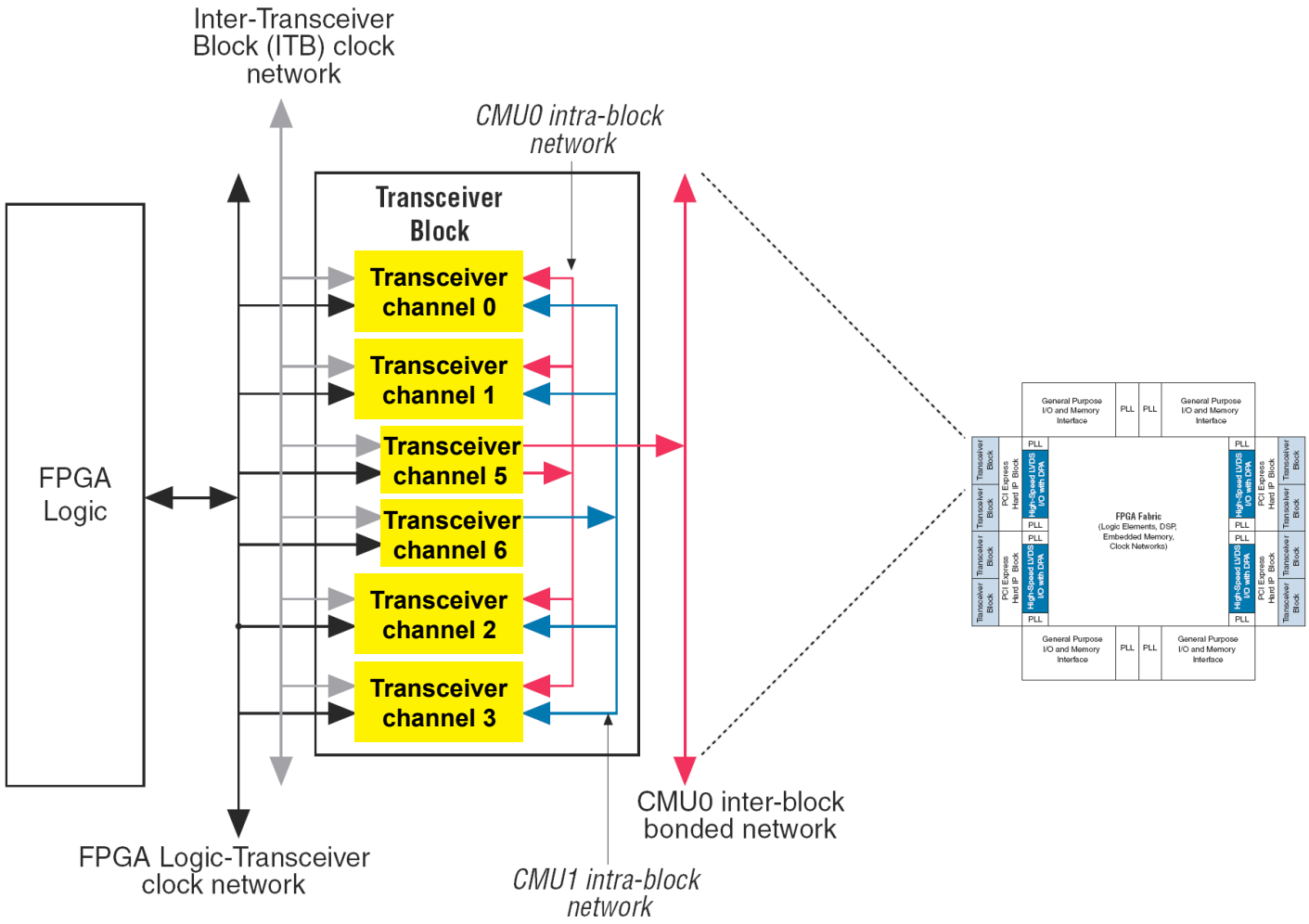
PMA = Physical medium attachment

PCS = Physical coding sublayer

CMU = Clock management unit

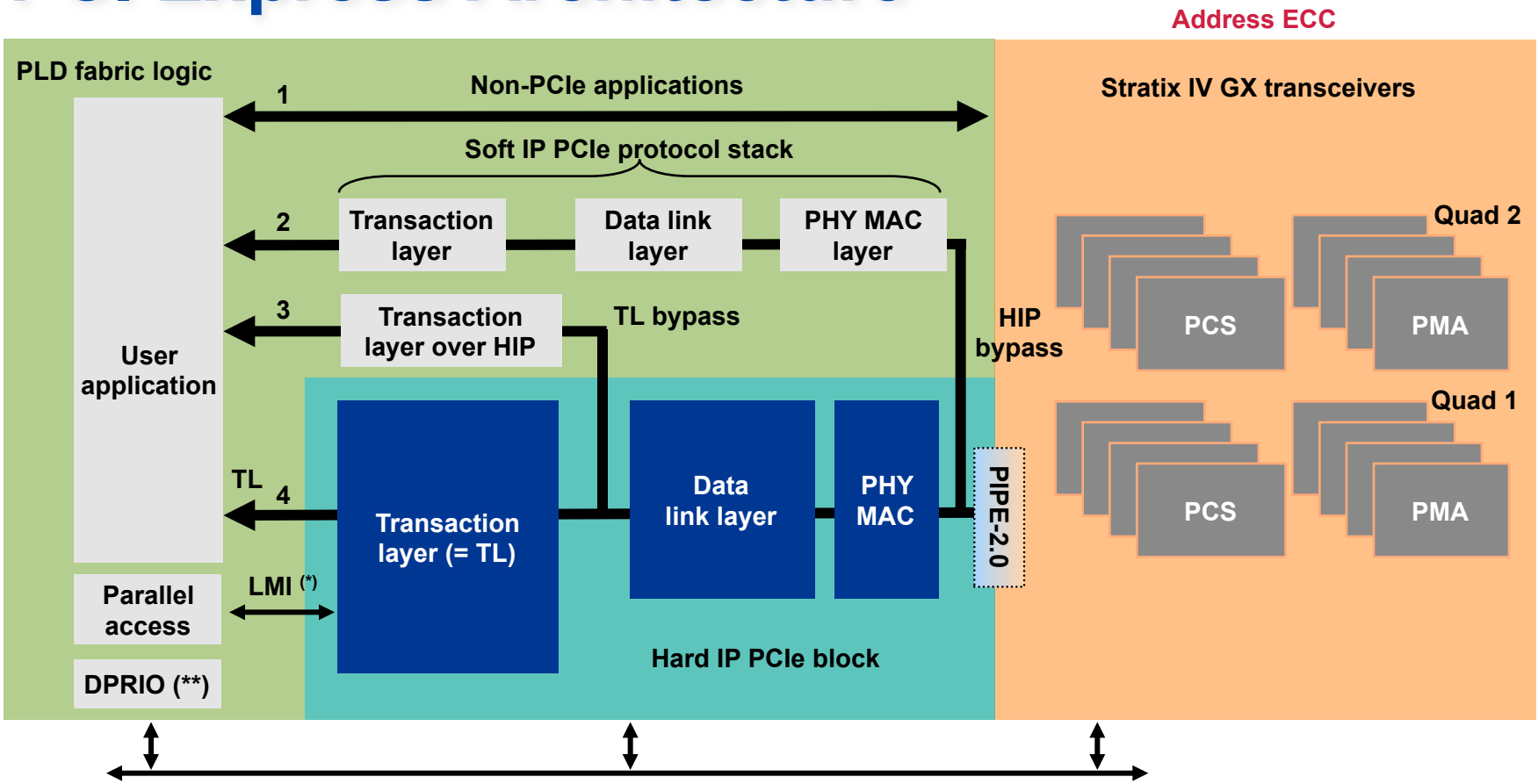
(1) The CMU can be configured as a transceiver channel with PMA only

6-Channels Configuration Example



(1) The CMU can be configured as a transceiver channel with PMA only

PCI Express Architecture



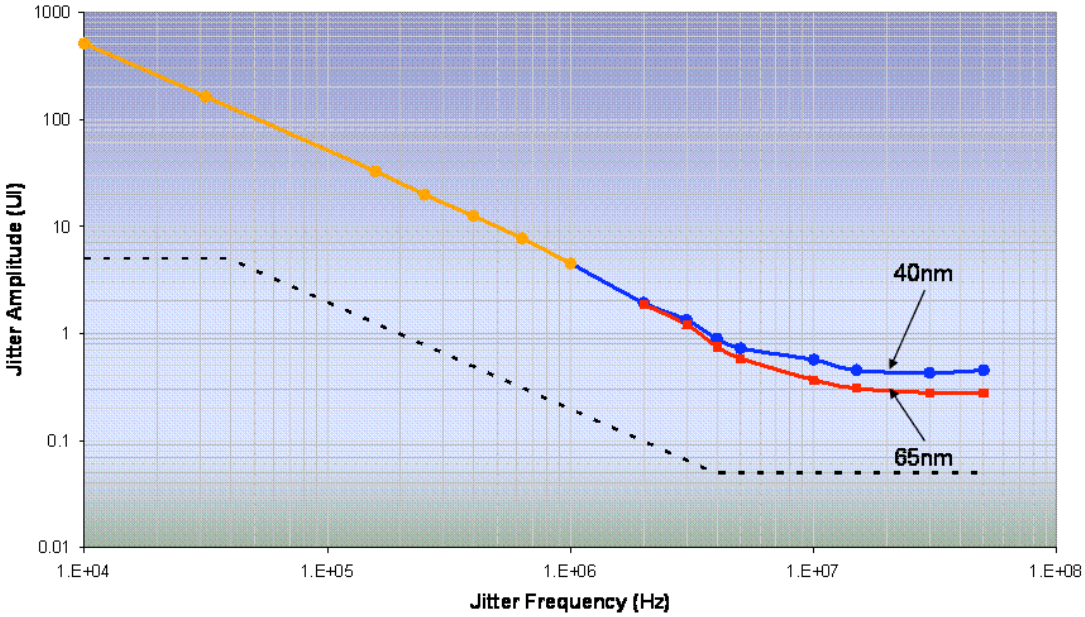
1. Non-PCI Express cores (XAUI, GbE, SRIO, etc…)
2. Soft PCI Express IP protocol stack
3. Soft PCI Express IP transaction layer over hard IP DL and PHY MAC
4. Hard Gen1/Gen2 x8, x4, x1 EP/RP hard IP (HIP) protocol stack

(*) LMI- Local Management Interface
(**) DPRIO- Dynamic Partial Reconfigurable Input/Output

Soft logic
PCIe hard IP
PCS/PMA

Transceiver Results

- Transceiver results
  - Pattern: PRBS 7
  - V_{od}: 600 mV
  - DJ: 10.3 ps
  - RJ (RMS): 1.23 ps
- Jitter compliance for PCI Express, CEI-6, and SONET/ synchronous digital hierarchy (SDH) with margin
- Ability to drive 50" of FR-4 backplane at 6.375 Gbps with built-in pre-emphasis and equalization
- Plug & Play Signal Integrity
  - Monitors and optimizes receive equalization over process, voltage, and temperature (PVT)
  - Supports hot swapping of transceivers
- Watch the demo videos:
  - www.altera.com/b/40-nm-stratix-iv-video.html
  - www.altera.com/plugandplay



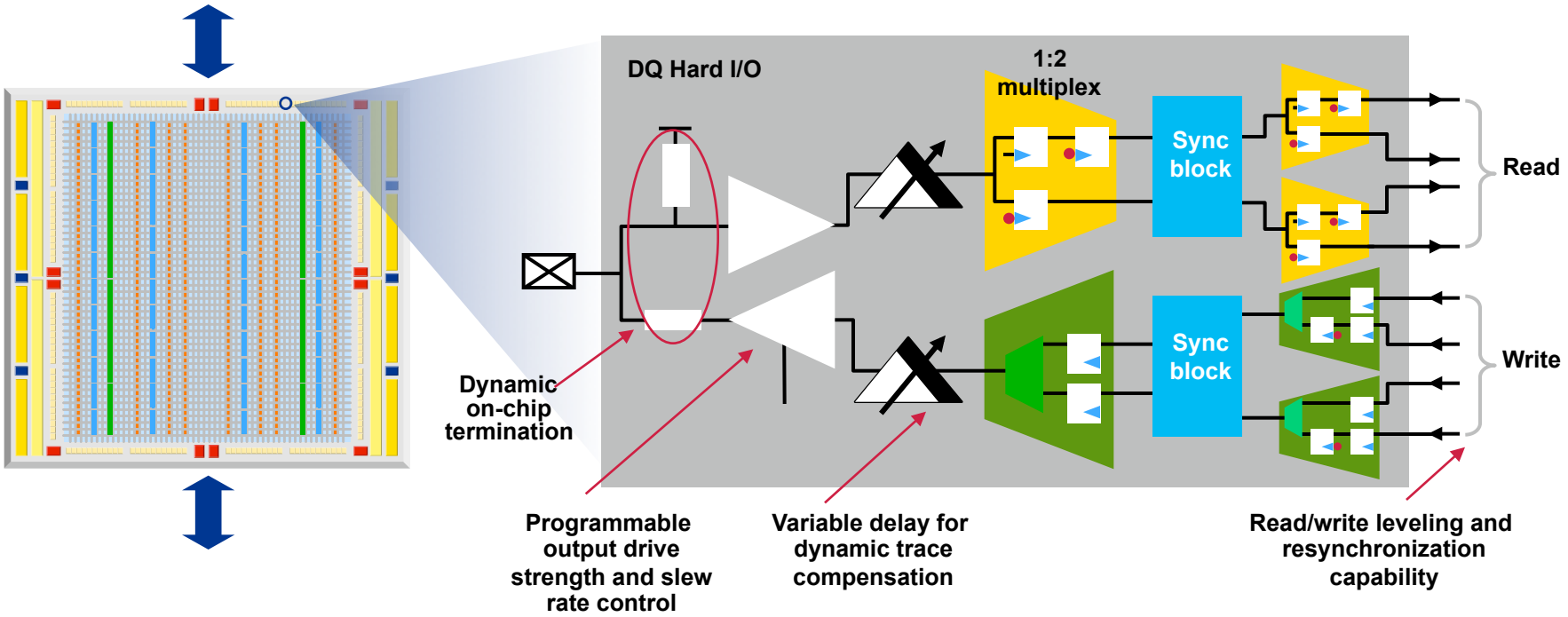
Memory Interconnect

	Stratix III/IV FPGAs
Interconnect	**Performance**
DDR3	533 MHz/ 1,067 Mbps
DDR2	400 MHz/800 Mbps
QDR II	350 MHz
QDR II+	400 MHz
RLDRAM II	400 MHz
LVDS	1.6 Gbps

I/O feature	Stratix III/IV FPGAs	Benefit
Dynamic on-chip termination	✓	Saves power
DDR3 read/write leveling	✓	DIMM support
Variable I/O delay	✓	Allows signal de-skew

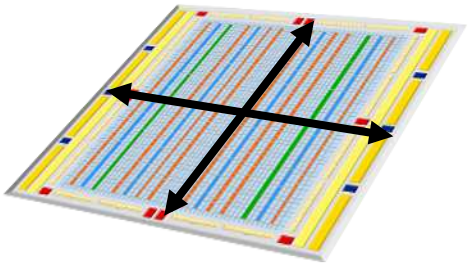
Memory Interconnect Architecture

- Dynamic on-chip termination significantly saves power
  - Example: 1.0W on a 72-bit interface with a 50/50 read/write cycle
- Self compensating for PVT, trace, and resynchronization
- Read/write leveling



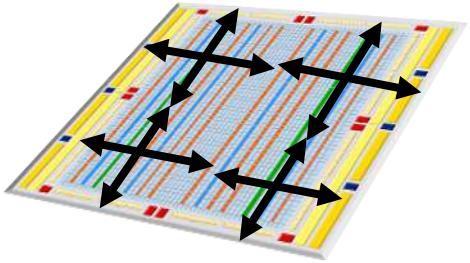
Clocking Resources

Global clock networks



16 networks per device

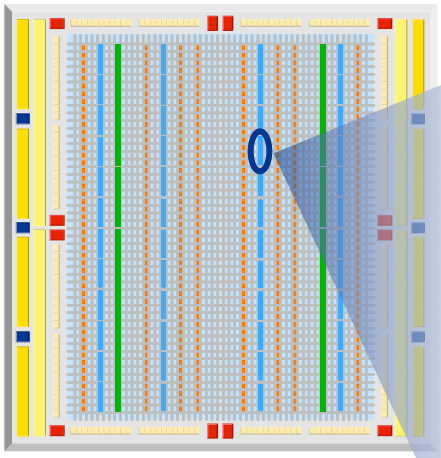
Regional clock networks

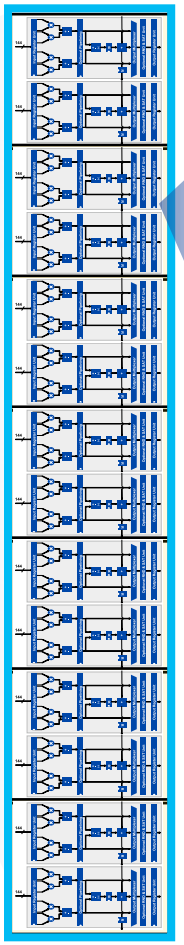


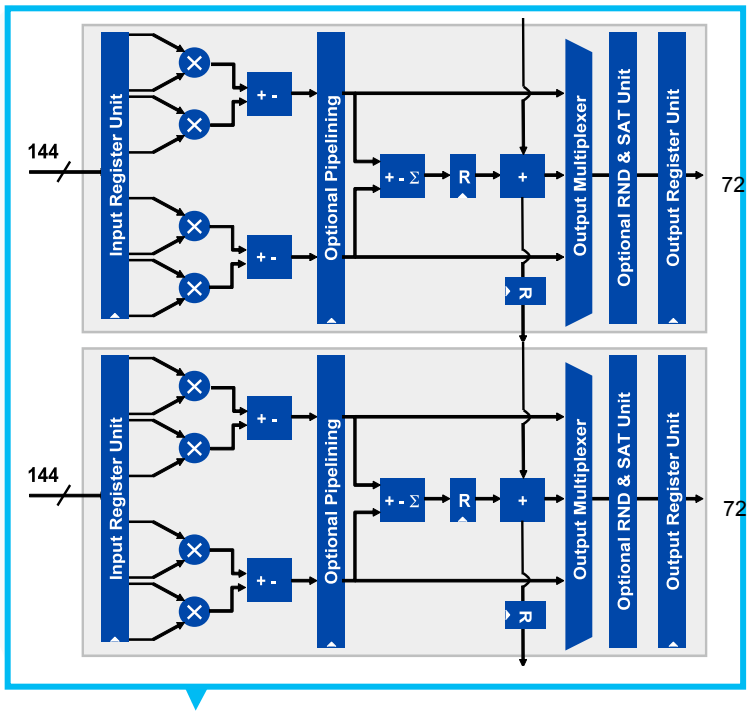
Up to 88 networks per device

- 200+ clock routing resources
  - 16 global clock networks (GCLK),
  - Up to 88 quadrant clock networks (QCLK),
  - Up to 132 periphery clock networks (PCLK)
  - Global clock routing can also be used for global signals
  - Powered down when not in use
- 12 low-jitter PLLs
  - 10 programmable outputs per PLL
  - Both frequency and phase can be dynamically changed
  - Cascadable to allow broader frequency generation

DSP Performance Through Parallelism







- Optimal DSP/memory/ logic ratio
- Resources per 18 x 18 multiplier
  - 400 registers
  - 17 Kbit embedded memory
  - 500 LEs

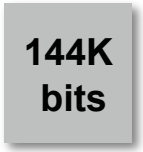
Total 18 x 18 multipliers = 1,360

Maximum clock frequency = 550 MHz

DSP performance = 1,360 * 550 MHz =

748 GMACS

Enhanced TriMatrix Memory

Memory functions	Stratix III devices	Stratix IV/HardCopy IV devices(1)
■ Processor code storage ■ Packet buffers ■ Video frame buffers	M144K 	M144K 
■ General purpose memory	M9K 	M9K 
■ Shift registers ■ Small FIFO buffers ■ Filter delay lines	MLAB  640 bits	MLAB  640 bits

Optimized block size for maximum efficiency

Note: (1) HardCopy ASICs implement memory logic array blocks (MLABs) in HCells

Stratix IV Family

	Device	LEs	Transceivers	Memory (Mbits)	Multipliers (18x18)
Stratix IV GX devices	EP4SGX70	70K	8	6.3	384
	EP4SGX110	110K	16	8.1	512
	EP4SGX230	230K	36	13.9	1288
	EP4SGX290	290K	36	13.3	832
	EP4SGX360	360K	36	17.7	1040
	EP4SGX530	530K	48	20.3	1024
Stratix IV E devices	EP4SE110	110K	-	8.1	512
	EP4SE230	230K	-	13.9	1288
	EP4SE290	290K	-	13.3	832
	EP4SE360	360K	-	17.7	1040
	EP4SE530	530K	-	20.3	1024
	EP4SE680	680K	-	22.4	1360

HardCopy IV Family

	Device	Gates	Transceivers	Memory (Mbits)	Multipliers (18x18)
HardCopy IV GX devices	HC4GX1	2.8M	8	6.3	384
	HC4GX2	3.9M	16	8.1	512
	HC4GX3	9.2M	24	12.2	1288
	HC4GX4	7.6M	24	12.7	832
	HC4GX5	9.5M	24	13.3	1040
	HC4GX6	11.5M	24	13.3	1024
HardCopy IV E devices	HC4E2	3.9M	-	8.1	512
	HC4E3	9.2M	-	10.7	1288
	HC4E4	7.6M	-	13.3	832
	HC4E5	9.5M	-	16.8	1040
	HC4E6	11.5M	-	16.8	1024
	HC4E7	13.3M	-	16.8	1024

Conclusion

- Significant logic and memory density
  - – 680K LEs (10+ Mgates) and 22 Mbits
- Innovations in performance, power, and cost
  - ALM, Programmable Power, HardCopy ASIC
- Bandwidth and flexible I/Os
  - 48 transceivers and 1100 user I/Os at 1 Gbit/pin