Tutorial

High-Bandwidth Memory Technology and Systems Implications

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Chuck Moore
AMD

High-Bandwidth Memory Technology and Systems Implications

Abstract: As Moore's Law enables us to pack more CPUs and other computing devices onto future chips, addressing the "Memory Wall" takes on a whole new level of importance.

The combination of larger working sets, multiple working sets, and bandwidth hungry offload computing devices take a difficult situation and make it worse.

This tutorial will introduce these challenges, and present several potential technology solutions, as well as the associated system-level implications.

Agenda

- Introduction and Motivating Issues

  Don Draper, Rambus, for Chuck Moore, AMD

- Terabyte Bandwidth Initiative - Architectural Considerations for Next-Generation Memory Systems

  Craig Hampel, Rambus

- Tera-scale Computing and Interconnect Challenges: 3D Stacking Considerations

  Jerry Bautista, Intel

- High Bandwidth Memory Technology: System Architecture Implications and Perspective

  Fritz Kruger, AMD