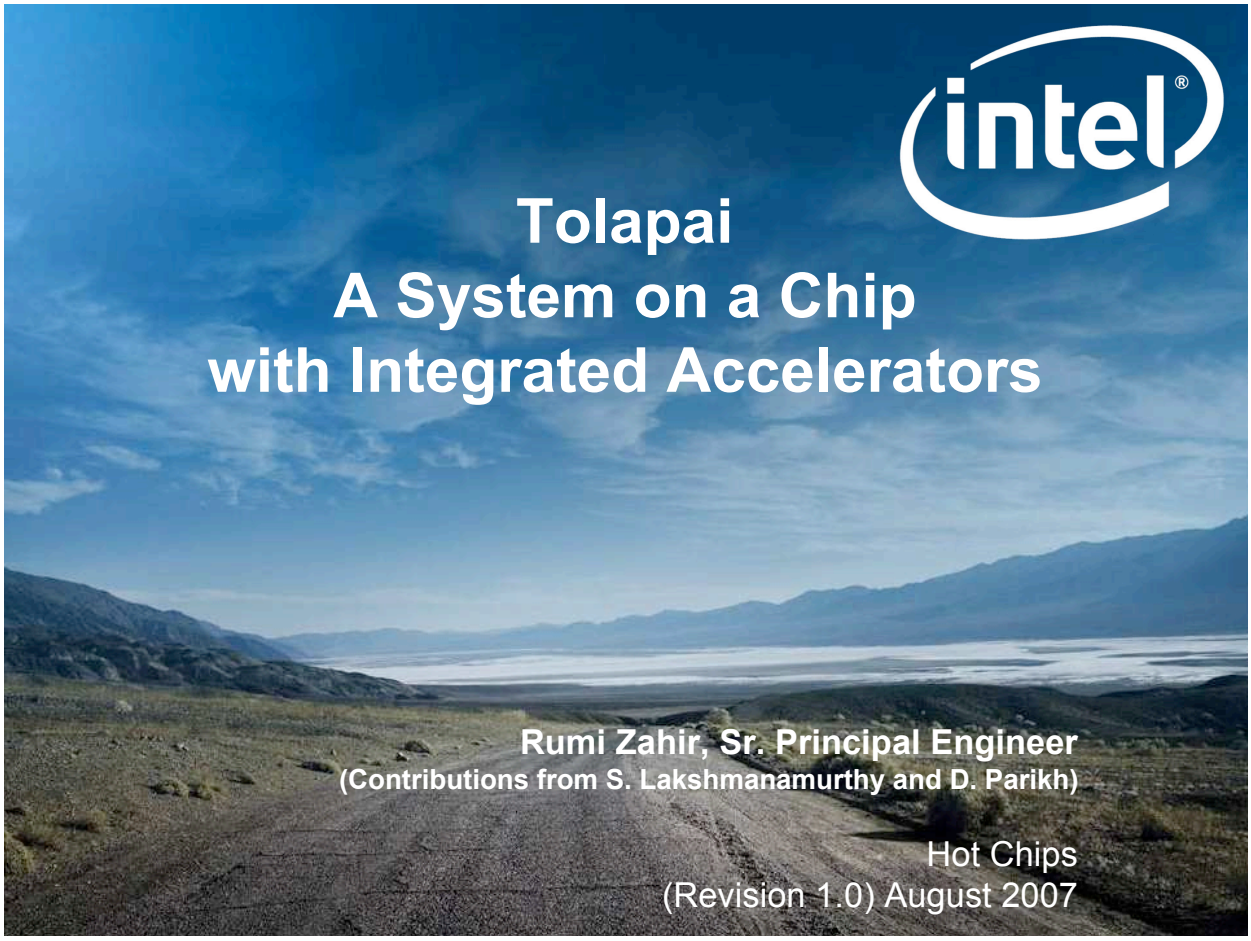
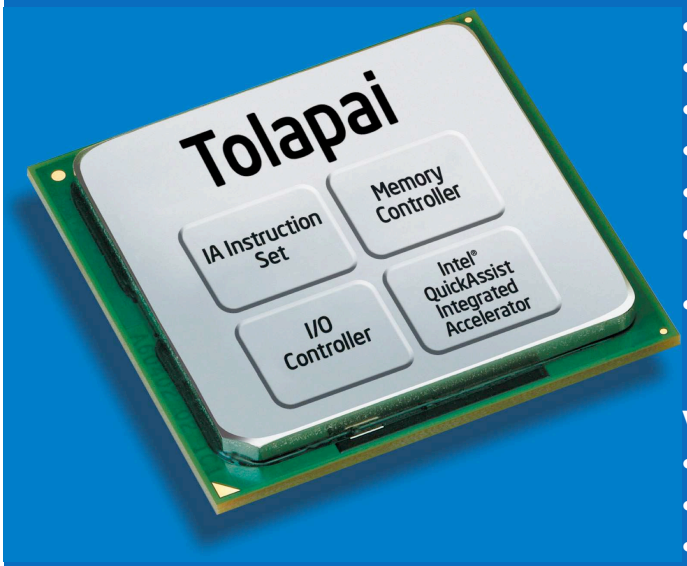


Tolapai
A System on a Chip with Integrated Accelerators

Rumi Zahir, Sr. Principal Engineer
(Contributions from S. Lakshmanamurthy and D. Parikh)

Hot Chips
(Revision 1.0) August 2007

Tolapai SOC – Intel® Architecture (IA) Computing & Secure Packet Processing on 1 Die



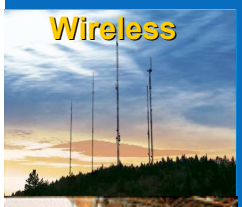
Single Die integrates

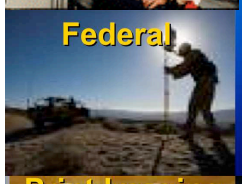
- IA CPU @ 600, 1066 and 1200MHz
- DDR2 memory controller (MCH)
- PCI Express*
- Standard IA PC peripherals (ICH)
- 3x Gigabit Ethernet MACs
- 3x TDM high-speed serial interfaces for 12 T1/E1 or Slic/Codec connections
- Intel® QuickAssist Integrated Accelerator
  - For high-performance security and IP telephony applications

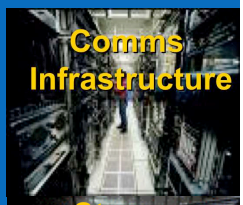
Vital Statistics

- 148 Million transistors
- 1,088-ball FCBGA w/1.092 mm pitch
- 37.5 mm x 37.5 mm package
- Intel's first integrated IA processor, chipset and memory controller since 1994's 80386EX.

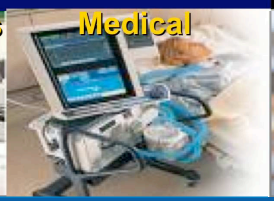
Tolapai Market Segments







Tolapai is expected to play in a diverse set of embedded, storage & comms segments.



Tolapai Agenda

- Objectives
- Block Diagram, Interconnect Topology
- Security/Packet Processing Models
- How IA and Accelerators Share Memory
- Memory Controller Design
- Expected Tolapai Benefits

Tolapai Objectives

1. **IA code base**
   - **Run existing mainstream IA OS, driver and application software**
   - **Standard tool chains & platform mechanisms (e.g., BIOS, ACPI)**
2. **Low power**
   - **13-20+ Watts TDP, based on application**
   - **Reduce operating frequency and voltage**
3. **Integration**
   - **Intel® QuickAssist Acceleration for security and IP telephony applications**
   - **PCI Express, Gigabit Ethernet, TDM (T1/E1) connectivity**
4. **Bill of Materials & Time to Market**
   - **Minimize pin count**
   - **Standard PC/ICH interfaces**
   - **Standard mainstream DDR2 memory technology**
   - **Wide (1.092mm) ball pitch helps reduce PCB layer count**

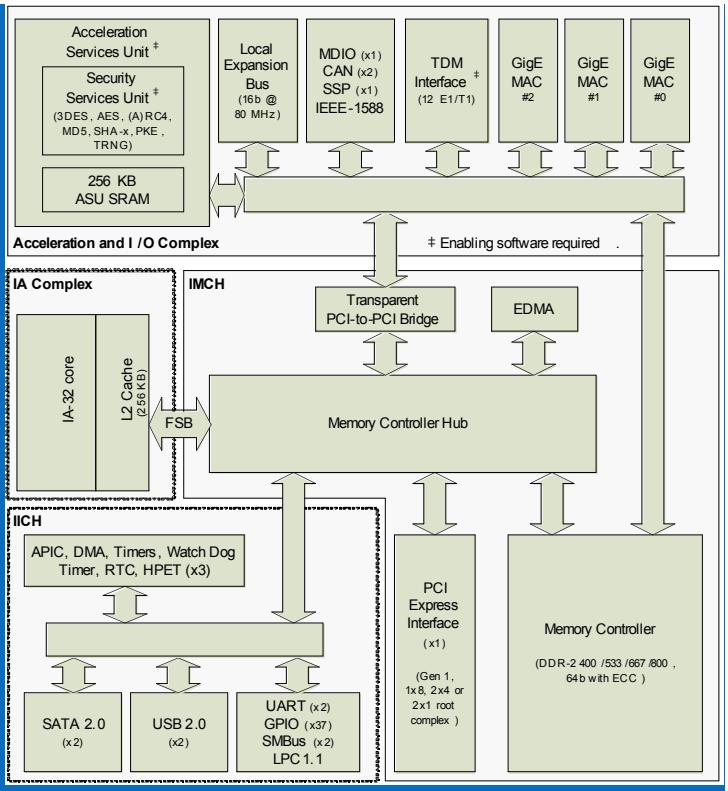
Tolapai

IA CPU Core w/ 256KB L2 cache
- Intel® Pentium® M processor derivative

Integrated Memory Controller
- 1 channel 64-bit DDR2
- 4 channel DMA engine
- PCI Express* (1x8, 2x4, or 2x1)

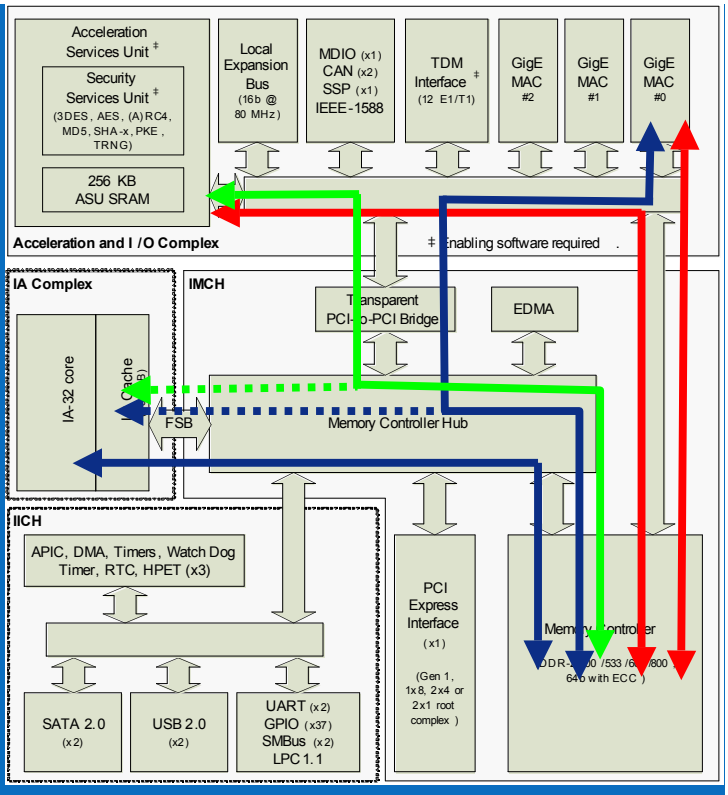
Intel® QuickAssist Acceleration
- Multi-core, Multi-threaded Engines
- 256KB Internal SRAM
- Security Hardware Acceleration for
  - Bulk: AES, 3DES, (A)RC4
  - Hash: MD5, SHA-x
  - Public Key – RSA, DSA, DH
  - Internal True Random Number Generator (TRNG)

Integrated I/O Interfaces
- 3x TDM (12 T1/E1)
- 3x GbE MAC (RGMII or RMII)
- 1x Local Expansion Bus (16b)
- 2x Controller Area Network (CAN)
- 1x Sync Serial Port (SSP)
- 2x UART, 37x GPIO,
- 2x SMBus/I2C, LPC
- 2x USB, 2x SATA
- WDT, RTC

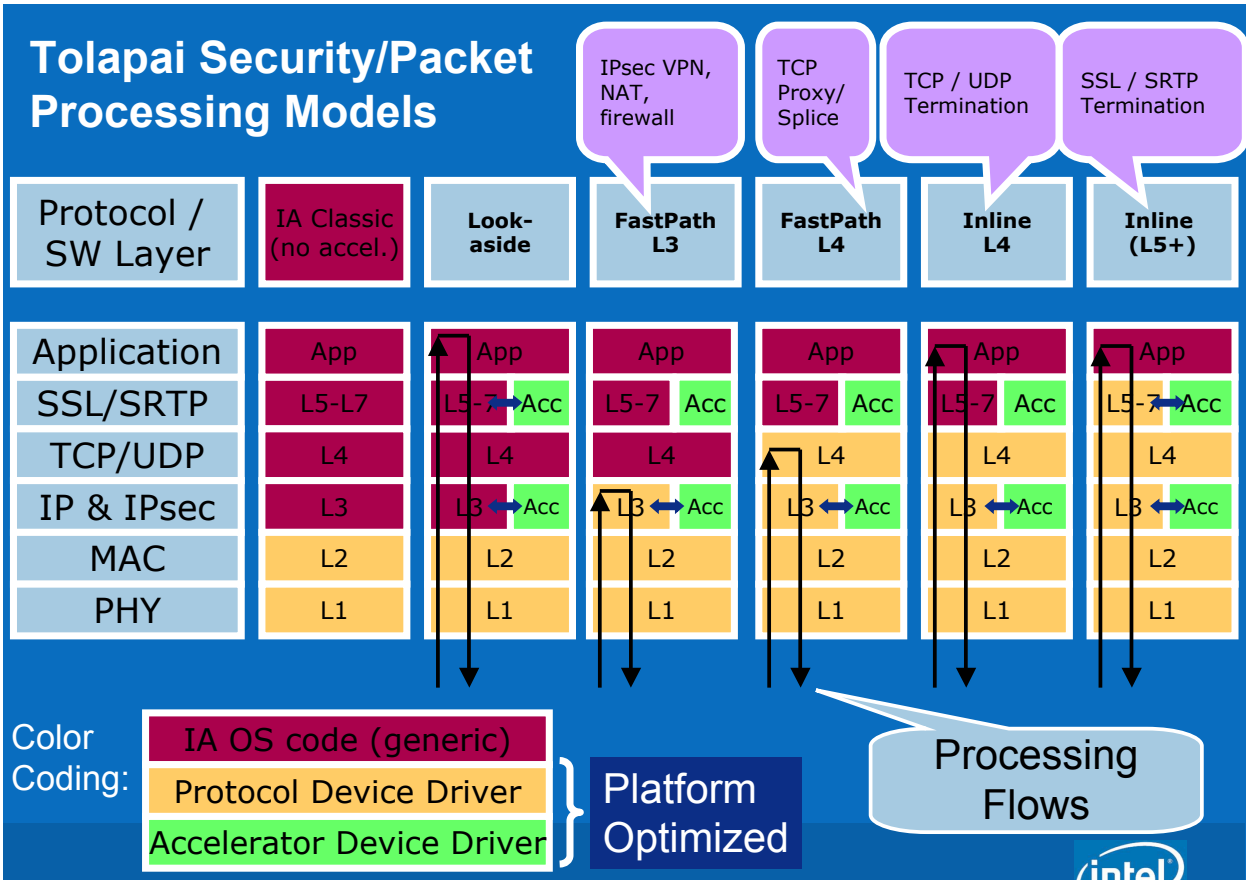


Packet Processing Flows

- Classic IA (blue)
  - GigE Rx DMA packets to DRAM (includes IA snoop)
  - IA interrupt
  - IA CPU runs protocol
  - IA CPU controls GigE TX
- Fastpath (red)
  - GigE Rx DMA packets to DRAM
  - Interrupt routed to accelerator
  - Accelerator operates on packet
  - Forwarding/filtering and security functions can be handled w/o IA CPU intervention
  - Accelerator controls GigE Tx
- Exception Packets (green)
  - Move packet to coherent DRAM (includes IA snoop)
  - Accelerator signals IA CPU



Tolapai Security/Packet Processing Models



How IA and Accelerators share Memory

Accelerators

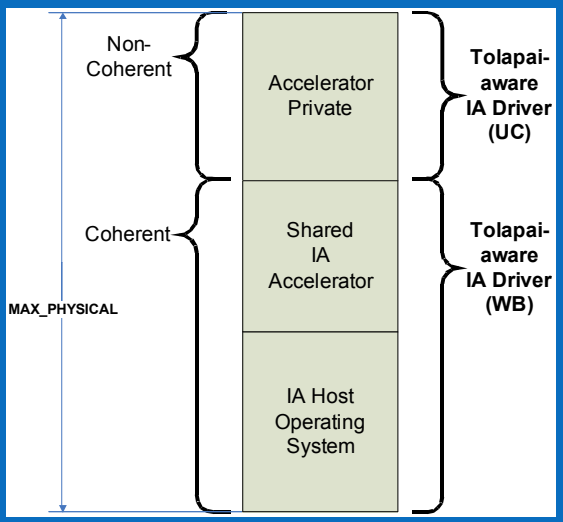
- Run in physical address space
- IA sees them as PCI device
  - Run concurrently, async. to IA CPU
  - IA CPU could be sleeping/throttled

IA and Accelerators share DRAM

- Most cost effective
  - Share devices, pins, i.e. bandwidth

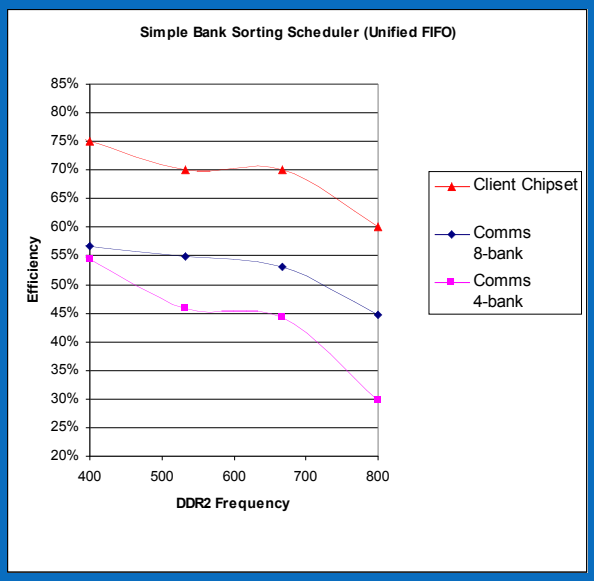
DRAM Partitioned

- Non-Coherent (Not Snooped)
  - Private to Accelerator
  - Physically contiguous portion hidden from OS
  - Accessible to Tolapai-aware IA driver
  - Separate high performance data path
- Coherent (Snooped)
  - Shared physical address space with IA



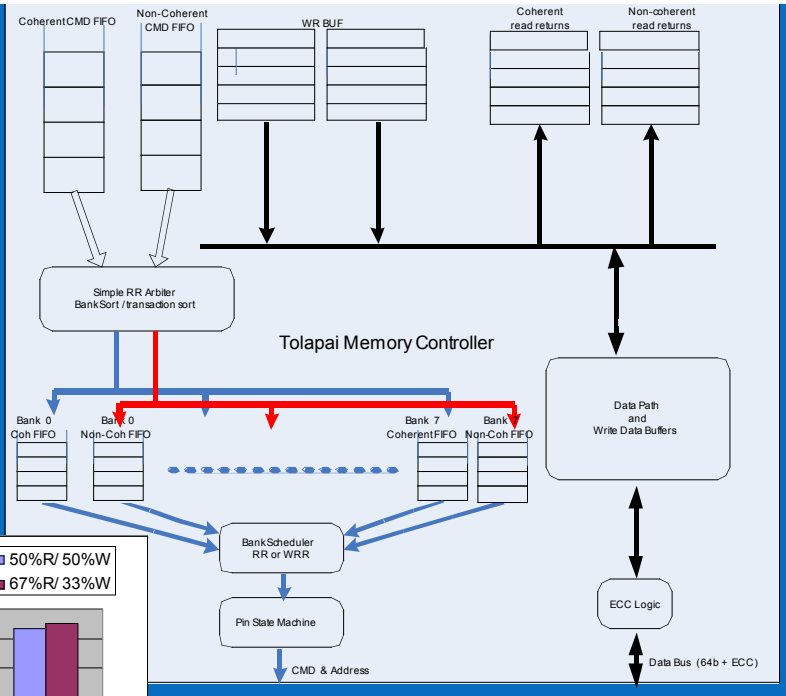
The need to optimize DRAM Efficiency

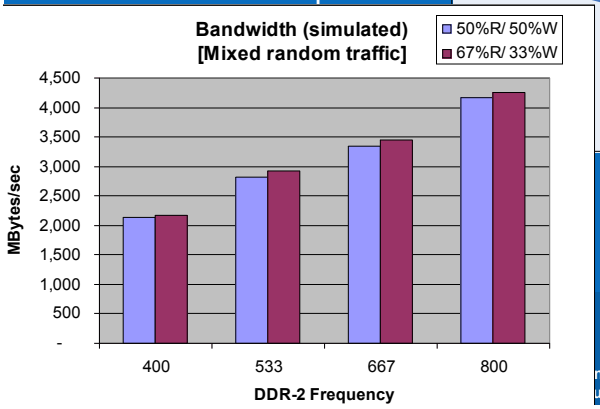
- **Typical IA chipset**
  - Optimized for 64B cache line bursts
  - Use page open policy (locality)
- **Typical Tolapai Access Pattern**
  - Comparatively I/O heavy
  - Highly interleaved address streams
  - DRAM controller is subjected to randomized address stream
- **Exploration**
  - Expect decreasing DRAM efficiencies
  - Tolapai cost-limited to single memory channel
  - Device Trc approximately constant (~50-60ns)
  - Development of Tolapai bank scheduling memory controller that overlaps per bank Trc



Tolapai Memory Controller

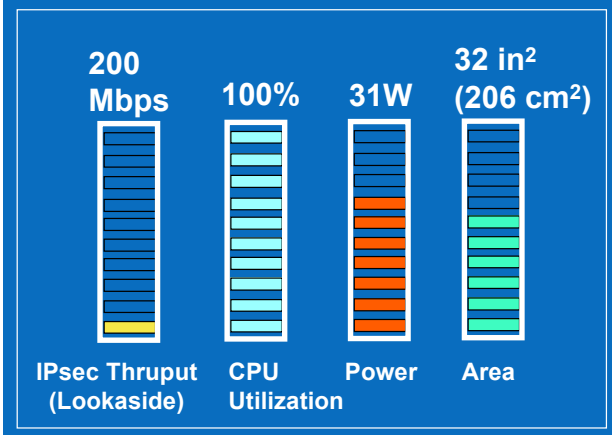
- Sort into independent bank FIFOs
- Interleave across banks
- Schedule each bank to maximize pin bandwidth
- Simulation shows 60-70% efficiency for mixed random address patterns

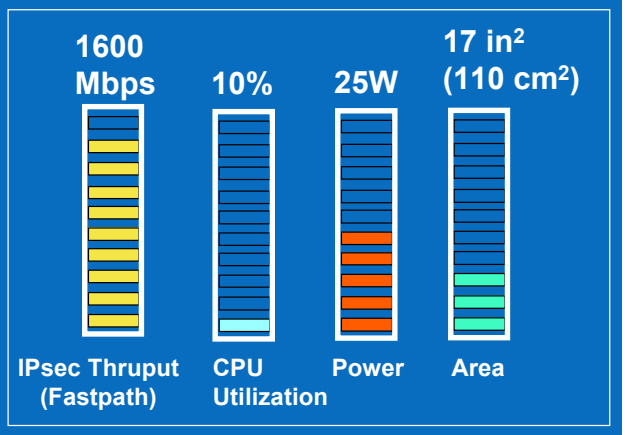




Expected Tolapai Benefits

Example - IPSec VPN Appliance using Tolapai





Traditional 4-chip IA Solution
(CPU + MCH + ICH + PCI Crypto Accelerator)

1-chip Tolapai Solution (simulated)

Estimated improvements based on simulation and are provided for informational purposes only. Results were derived using simulations run on an architecture simulator. Any difference in system hardware or software design or configuration may affect actual performance.

Assumptions:

- Compares Intel® Pentium® M processor-based platform with external PCI crypto accelerator to 1-chip Tolapai solution
- 256 byte packets with 2048 IPsec VPN tunnels

Summary

- Tolapai is a new Intel system-on-a-chip that integrates an IA core, an MCH, an ICH and Intel® QuickAssist Integrated Accelerators.
- Tolapai's accelerators focus on widely used Internet security functions.
- Accelerators provide power-efficient security performance and enable headroom for IA applications.
- Memory controller optimized to get maximum performance out of a single DDR2 memory channel for both IA processor and accelerator traffic.

The Tolapai platform helps customers to rapidly build cost-effective fully IA-compatible systems and embedded IP-enabled appliances.