IBM Research – T. J. Watson Research Center

CMOS Technology Nodes: Trends, Challenges, Opportunities?

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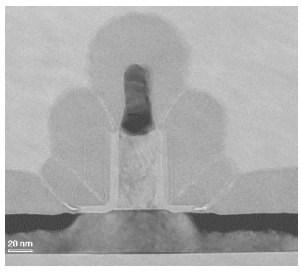
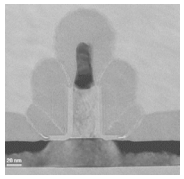
CMOS Scaling: Dennard's Theory

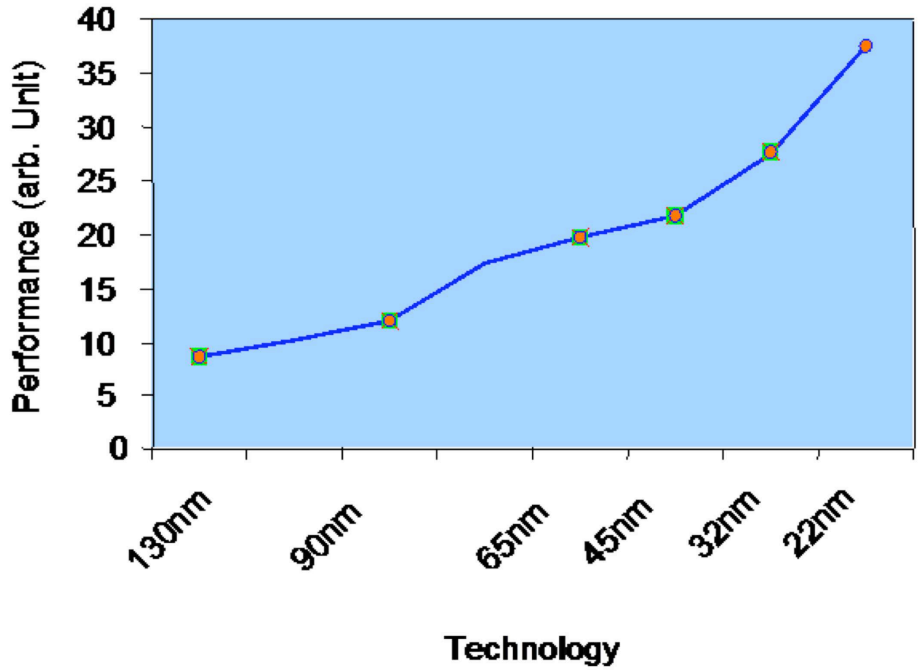
Scaled technology generations





Smaller
Faster
Lower Power

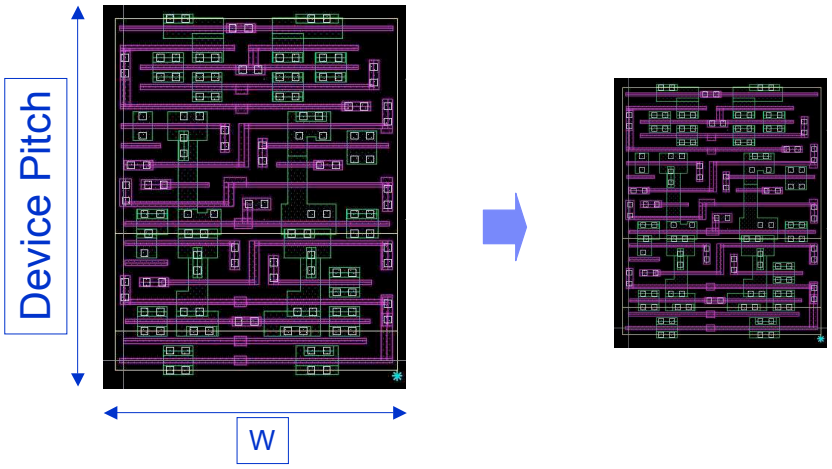
Device Performance: ~30% per Generation



Performance Challenge

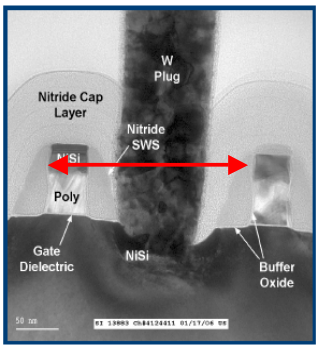
- Technology performance gain continuing
  - Through 32-22 nm nodes
  - Power-delay curve improving
- Issue: Supply voltage not going down
  - Power density (and power)
- Solution: Industry moving to multi "low-power" cores
  - Performance not through frequency
- Do we care as much about performance?
  - System performance: Number of cores vs. the frequency
- Drive to higher VT's and lower supply => Effectively devices not as fast

CMOS Density: Moore's Law



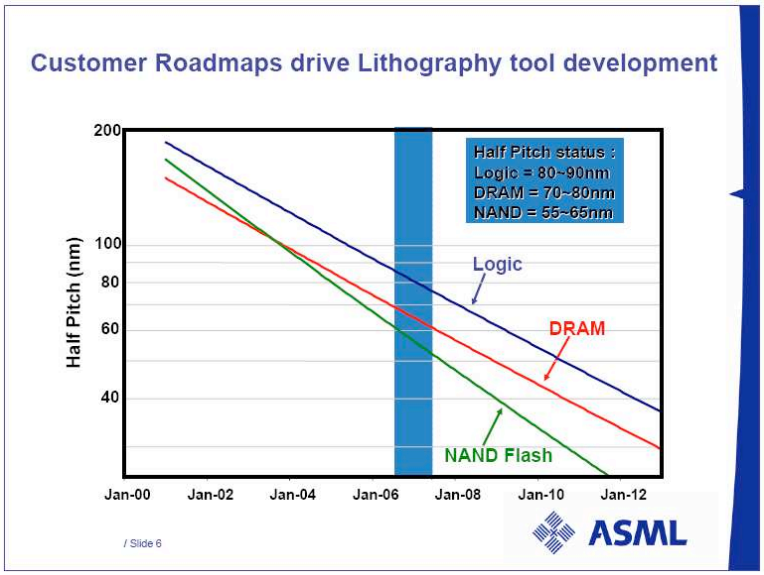
- 30% Reduction in W and device pitch
  - 50% area reduction
  - **2X device/area (every 2 years)**

Device Pitch Scaling



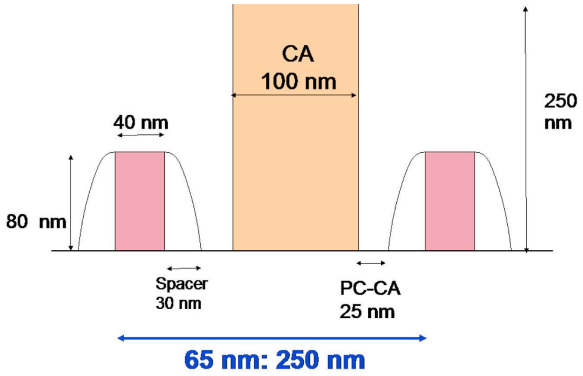
Node	Device Pitch (nm)	Year
65	230-350	2006
45	170-180	2008
32	120-130	2010
22	90-100	2012
15	**70-80**	**2014-15**
11	55-65	2017-18

Lithography Roadmap (ASML)



- 70-80 nm pitch (15 nm node) is feasible with immersion

15 nm (Post 22) Node Cross Section:



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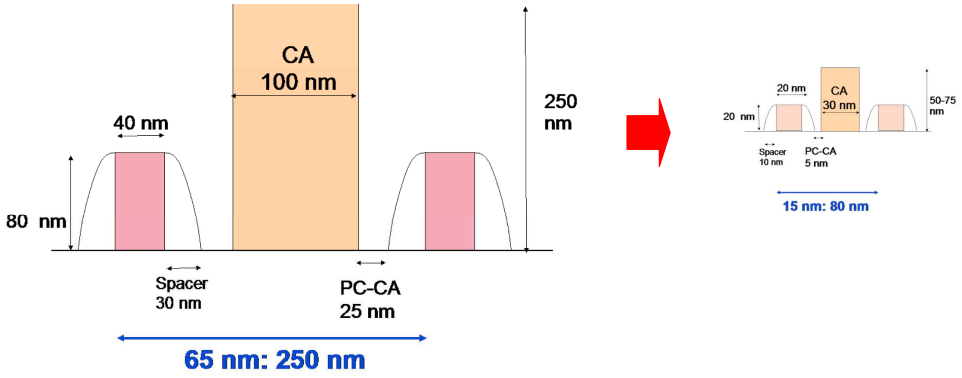

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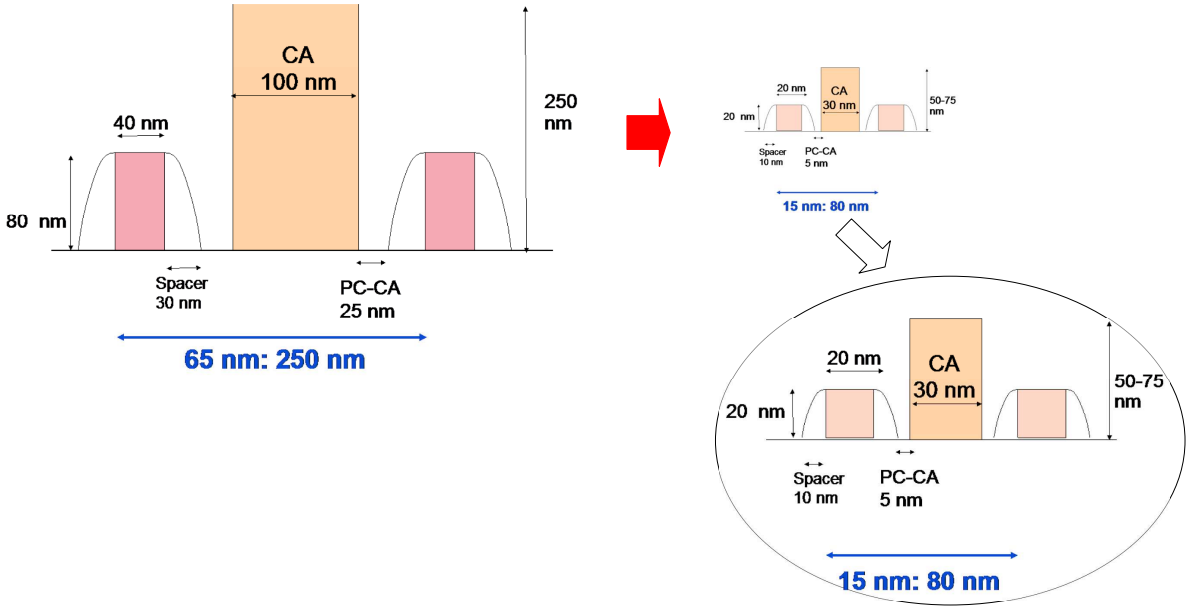
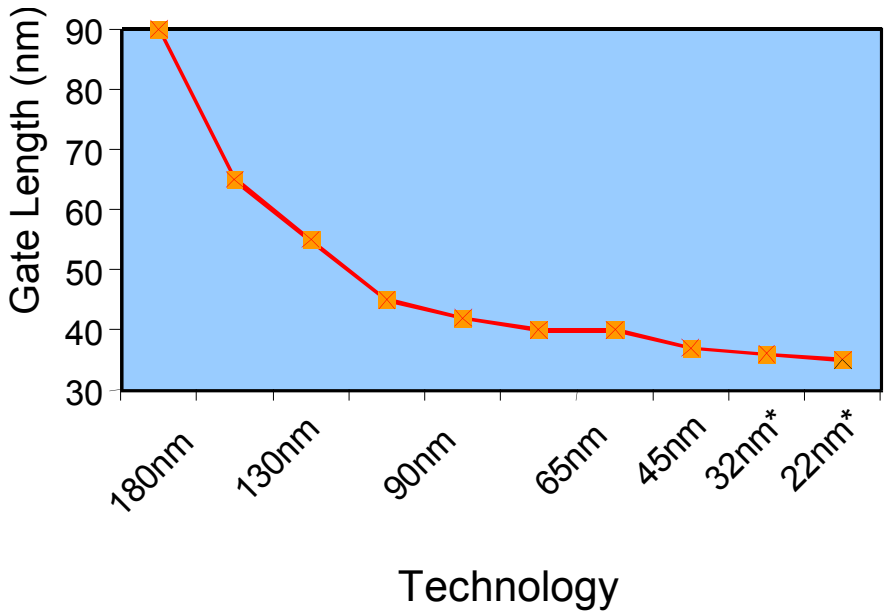


Challenge: L Scaling



Value of CMOS Scaling: Transistors/Unit Area

- Extrapolate from 65 nm Intel's Xeon and IBM's Power 6 dual cores

Node	Transistors / cm2	Transistors / 450 mm2
65	0.2 B	0.9 B
45	0.4 B	1.8 B
32	0.8 B	3.6 B
22	~1.6 B	7.2 B
15	~3.2 B	14.4 B
11	~6.4 B	25.8 B

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- 3D will add another 2-3X more transistors/unit area

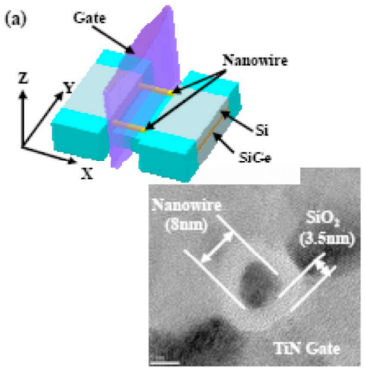
CMOS Paradigm Shift

- Device count will continue to go up
  - Moore's Law goes on

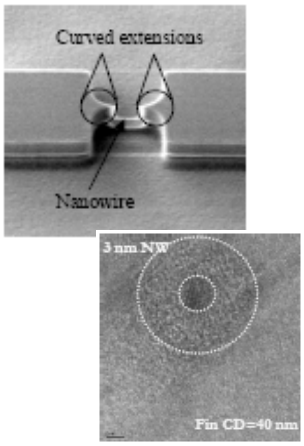
100's of Millions of high performance devices in 2D → 10's of Billion of low performance devices in 3D

- Key challenges:
  - What to do with multi billion transistors / cm2

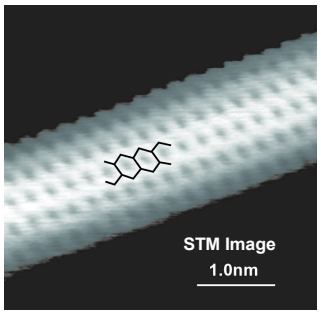
What About "Nano"-Devices?

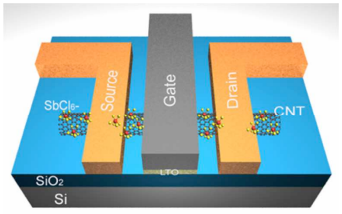


K. H. Yeo et al. (*IEDM* , 2006)



N. Singh et al. (*IEDM* , 2006)





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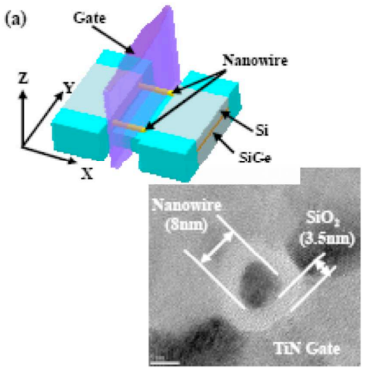
What About "Nano"-Devices?



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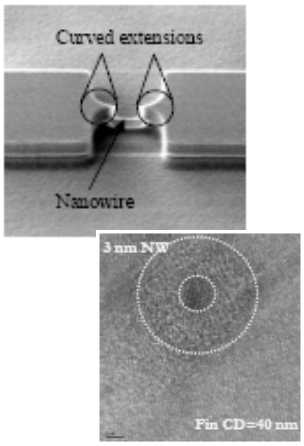

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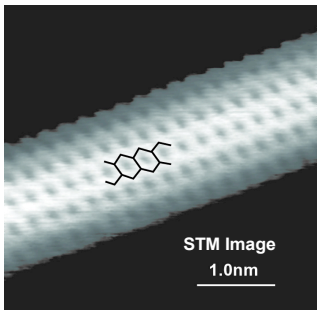

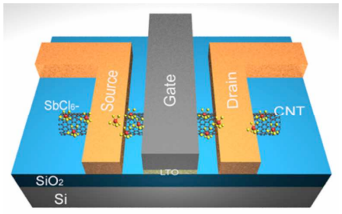

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Key Attribute: Small width

When Will We Get to Real Nano?

- Key Attribute: Small width

Node	Minimum W (nm)
45	70-80
32	50-60
22	35-45
15	25-35
11	16-25
8	10-16
5	7-10

- Nano-devices by 2020-2025 in production?