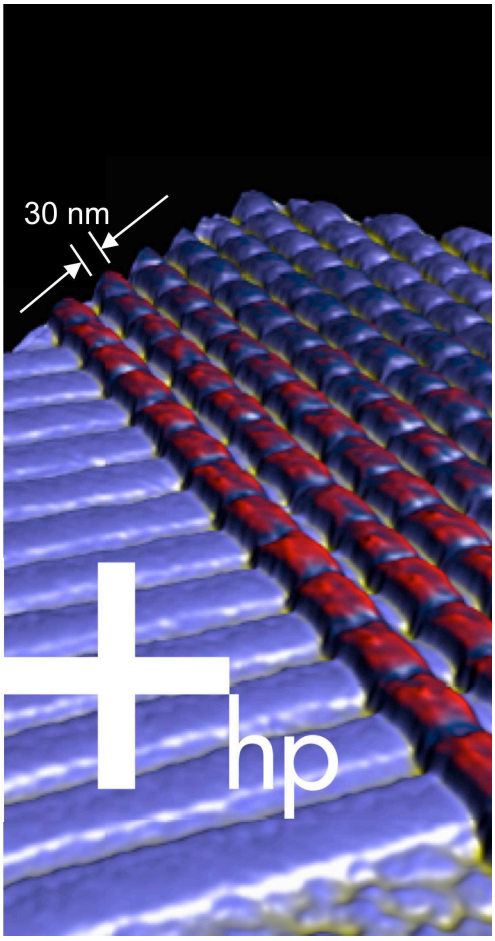
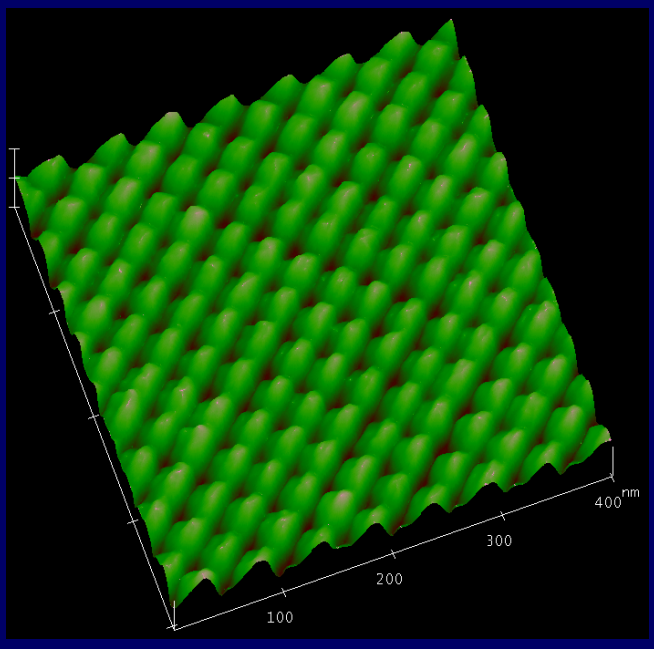
2007 Hot Chips

What's Next After CMOS?

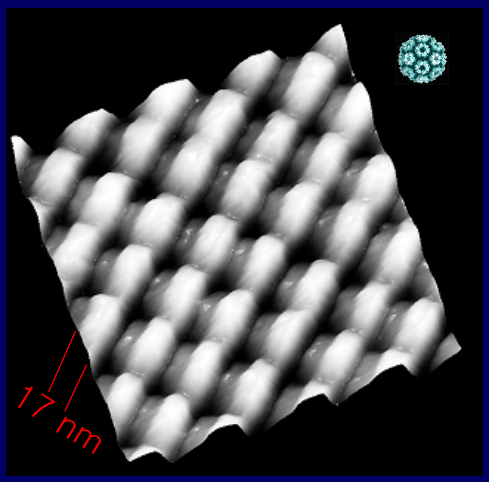


Stan Williams
HP

AFM image of crossbar structure at 17nm hp



The smallest virus: 20 nm in dia.



(cell density : 100 Gbit/cm^2)

The past 40 years has been about getting more transistors on a chip –

The next 40 years will be mainly about getting more out of each circuit component.

Two technologies will hybridize with Si to increase performance dramatically while keeping volume and power in check.

Photonics

nanoSwitches

photonic metamaterials — memrisive devices

higher bandwidth/power — high density memory

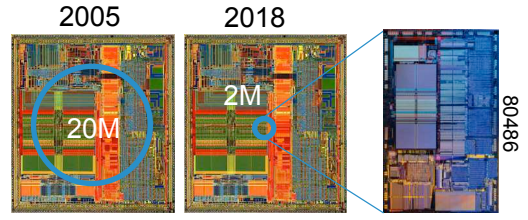
lower latency — configuration bits

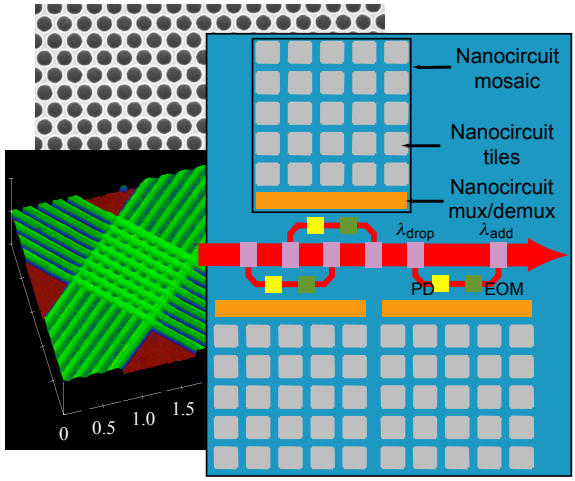
larger core area — circuit resiliency

new integrated opto-electronics architectures

Applications of nanophotonics to information technology

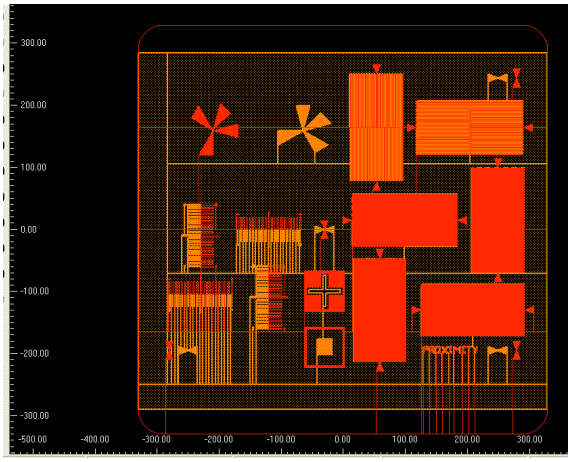
- ITRS Roadmap: performance limits
  - Global interconnect layer will drastically limit on-chip clock speeds and electrical power consumption
  - Information capacity of metal wires drops as A/L^2
  - Electronic clock domain will shrink from 2 mm (2005) to 125 μm (2018)
  - Accessible transistors per clock cycle will shrink from 20M (2005) to 2M (2018): Intel 80486
- Nanophotonics
  - Capacity independent of length
  - Area can be reduced using photonic crystals and other nanophotonic structures
  - Apply ITRS-planned fabrication advances (e.g., nanoimprint lithography) to reduce costs
  - Enables a "Moore's Law" for optics
- Massively parallel optical transceivers
  - Old: logical-to-physical (electronic)
  - New: logical-to-frequency (optical WDM)
  - All mosaics of nanocircuit tiles can be accessed in parallel → multi-terabit/second
  - Dramatically increases performance and reduces power consumption
  - Enables real-time world-wide command and control, real-time pattern matching





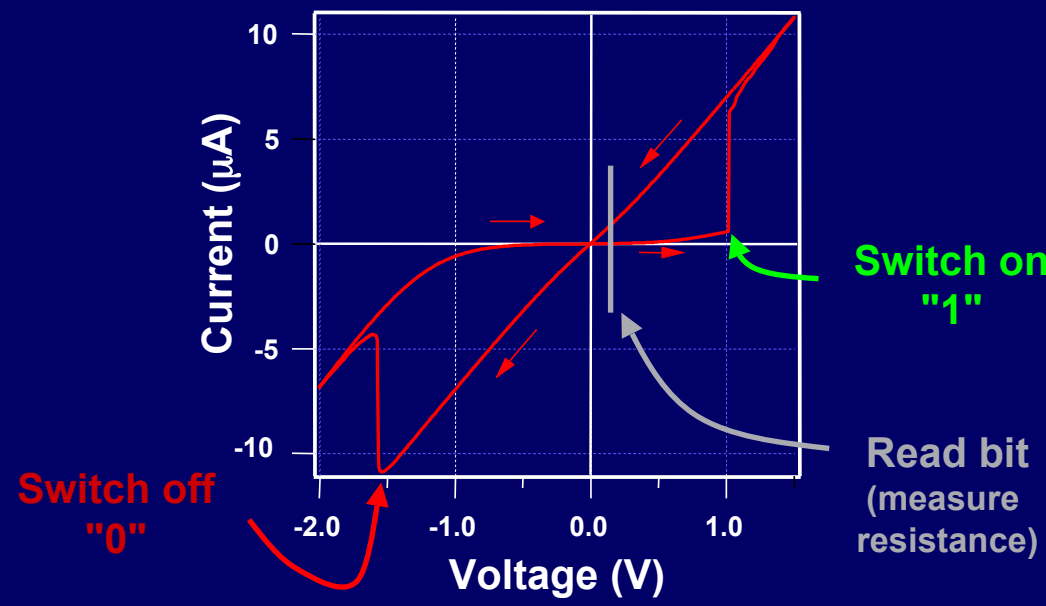
Photonic crystal integrated circuit

- Challenges (under test)
  - Template
    - E-beam litho to get round holes at proper exposure
    - Template etch profile
    - Template sidewall profile
    - Template CD bias
    - Scratch prevention at dicing vendor
  - Mix and match of litho tools
  - Dry develop CD bias and profile
  - Silicon dry etch of PhCs
  - Fragility after release

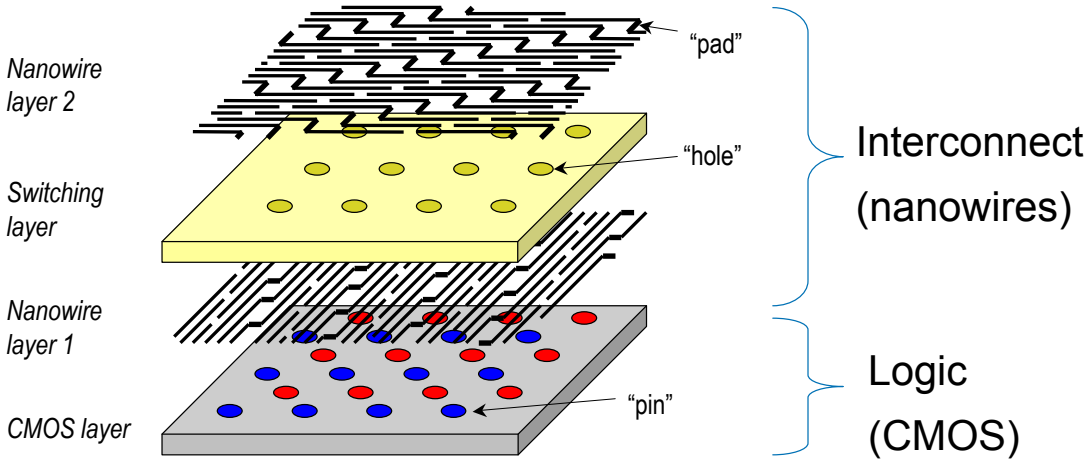


Technology transfer to HP development organization in progress

Memristive Tunnel Switch

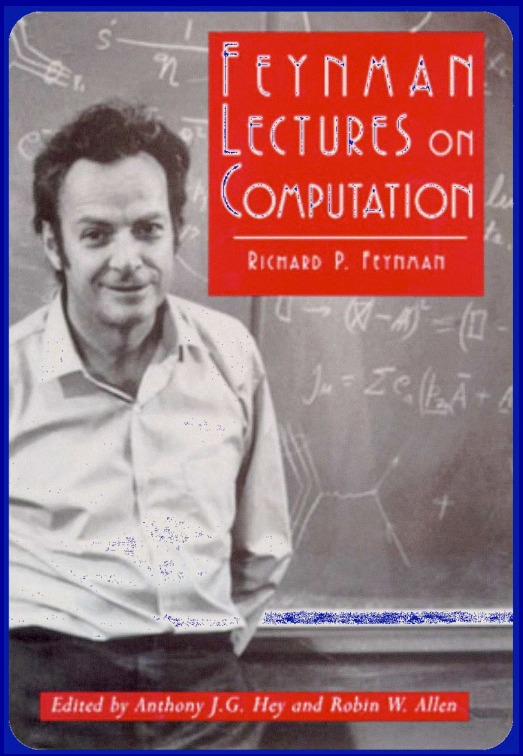


Field-Programmable Interconnect



1 nanowire → 1 pin

Age of Computing has not yet begun!



$P > n\nu \ln 2 \, k_B T$ *thermo*

$P > n\nu^2 \hbar$ *quantum*

- P = power
- k_B = Boltzman constant
- T = temperature
- $\hbar$ = Planck's constant
- ν = operating frequency
- n = number of parallel operations

Possible to improve efficiency by 10^8 x


invent