



## HotChips 2007



### An innovative HD video and digital image processor for low-cost digital entertainment products



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## Salient features of the SoC

- HD video encode and decode using 16-bit DRAM interface
- Up to 75 MP/s of image processing for fast picture capture, processing, and display
- Low-power consumption for portable end equipments
- Flexibility and programmability for implementing new use-cases
- High level of integration coupled with high performance to bring high-end features into low-cost products
- Belongs to the DaVinci™ family of digital video processors; products with this SoC shipping in the market today

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# Outline

- Target applications
- Block diagram of the SoC
- Architectural details of key components
- Performance and power specifications
- Software platform
- Example reference design (used for 2 target applications)
- Floorplan and key statistics of the SoC



# Target applications



Digital still camera



Solid state camcorder



HD docking station



Digital photo frame



IP security network camera



Photo printer



HDTV card reader

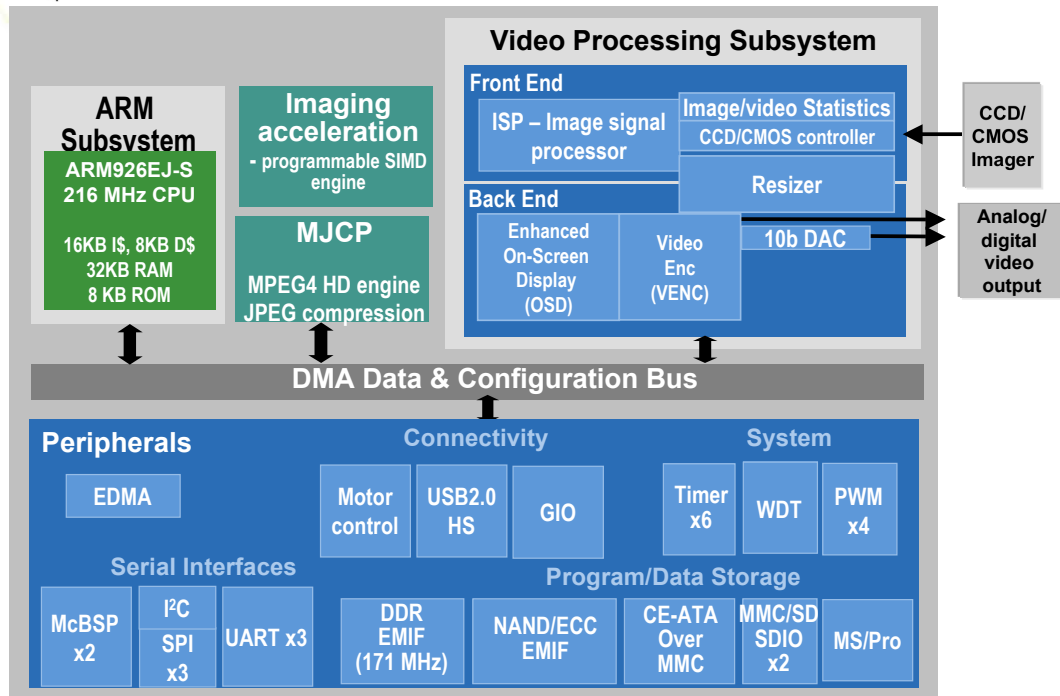


Low-cost portable media player





## Block diagram



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## Video processing subsystem

- State-of-the-art ISP for camera capture
  - **Advanced image processing algorithms in hardware with additional software programmable accelerators for flexibility**
    - **Handles any sensor read-out pattern**
    - **Latest generation of lens distortion/shading compensation, noise filters, CFA interpolation, color processing, edge enhancement, and resizing IP**
    - **Real-time statistics for auto focus, exposure, white balance, video stabilization, image classification, etc**
- Optimized display subsystem
  - **Multiple video and graphic window support for enhanced GUI**
  - **Integrated analog components for direct connect to a TV**
- System tailored master interface
  - **Multi-level arbitration to re-order and buffer various module commands/data to simplify SoC level interconnect**

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## Video and imaging coprocessors (1 of 2)

- Flexible SIMD engine
  - Allows for implementing differentiated algorithms at 5-10x speed of an ARM processor
    - high ISO (low light) noise filtering, redevye reduction, face tracking/detection and recognition, image stitching, adaptive contrast enhancement, motion estimation
  - Up to 8 ALUs used per cycle
    - MAC, absolute difference, table lookup, max/min, median, etc
  - Local SRAMs with multiple banks to achieve maximum memory performance
  - Programmed using vector style instructions with each instruction operating on a 2D block of data
  - APIs available for common functions



## Video and imaging coprocessors (2 of 2)

- MPEG4 compression engine
  - Processing at HD rates with margin to achieve 30 fps in a system
  - Programmable ME engine for resolution versus bit-rate/PSNR tradeoff
  - ME engine performs tasks of 422-to-420 conversion, full and half pel ME, inter/intra coding decision, Y and C prediction, and various block copies
  - 16-way SAD engine
  - Budget less than 1000 cycles per macro-block
- JPEG compression engine
  - Fixed function block
  - > 40 MP/s sustained performance in a system
  - Can be used for video as a mJPEG sequence



## Infrastructure components

- Shared across portfolio of DaVinci processors
  - Reuse at IP, SoC, drivers, and software
- On-chip bus
  - Split command and data to maximize performance for multiple masters at different priorities, latency & bandwidth requirements, and transfer sizes
- DRAM memory controller (DDR EMIF)
  - Multi-level arbitration schemes to achieve HD performance in a 16-bit DDR2 environment
- EDMA
  - Flexible DMA engine with 64 channels to simplify programming of slave data transfers

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## Key application performance specs

- Raw image processing (ISP and JPEG compression)
  - 75 MP/s
- Sustained image processing (limited by overall system not the SoC)
  - > 5 fps at 8 MP resolution
- HD video encode and decode (720P)
  - > 30 f/s MPEG4 in full system including digital video stabilization
- Advanced image processing (using programmability in the SoC)
  - High ISO image capture (10000)
  - Red-eye removal (< 400 ms for 10MP image)
  - Fast face-tracking (> 30 f/s)
  - Adaptive image contrast enhancement (< 500 ms for 10 MP image)
  - Panoramic image stitching (3 images < 1 second)

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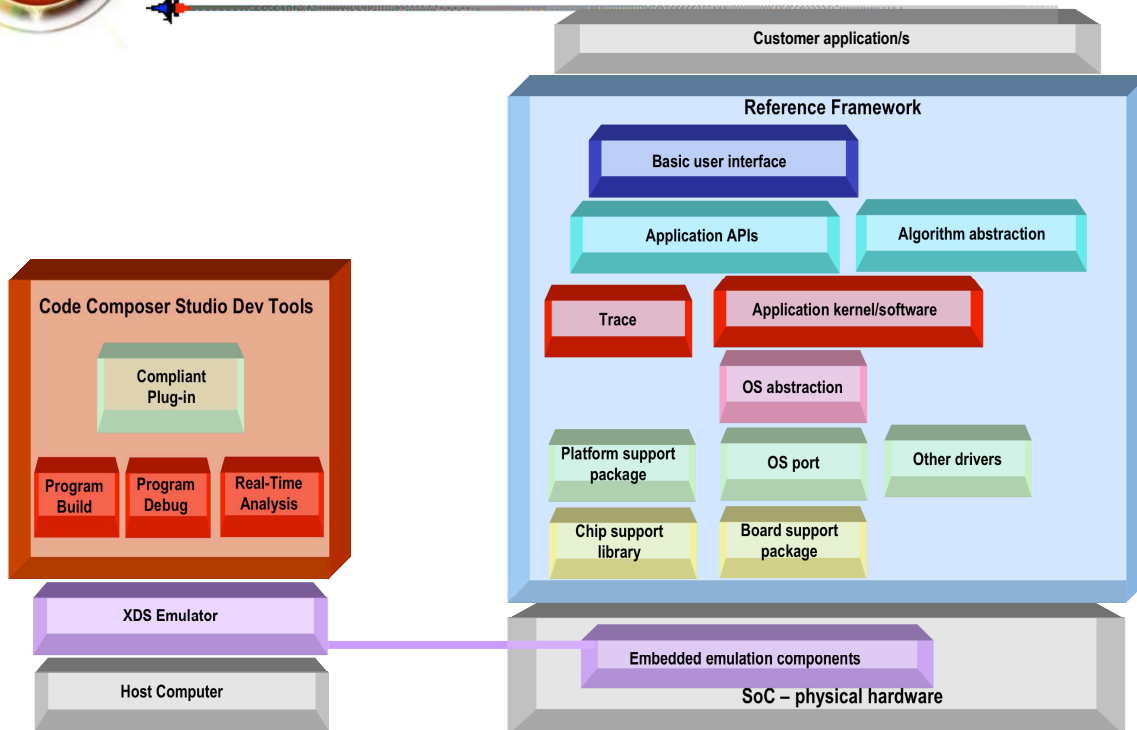


# Power consumption

- Standby power (deep sleep mode)
  - 1 mW
- Image and video preview
  - < 200 mW without DRAM power; < 250 mW including DRAM power
- SD video encode and playback
  - < 250 mW without DRAM power; < 330 mW including DRAM power
- HD video encode (720P)
  - < 400 mW without DRAM power; < 550 mW including DRAM power
- High speed image processing (> 50 MP/s)
  - < 300 mW without DRAM power, < 400 mW including DRAM power



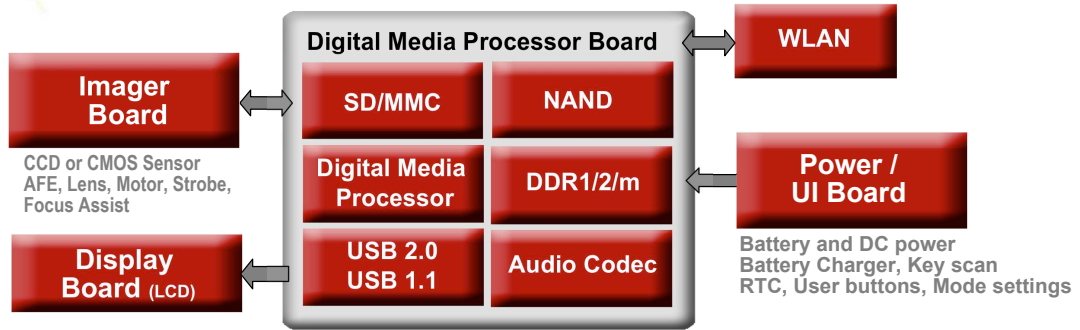
# Software platform overview







# Example: HW + SW turnkey reference design for digital imaging products (DSC, DVC)



## Hardware

- Processor Board
- LCD Board
- Imager Board
- Power / UI Board

## Software

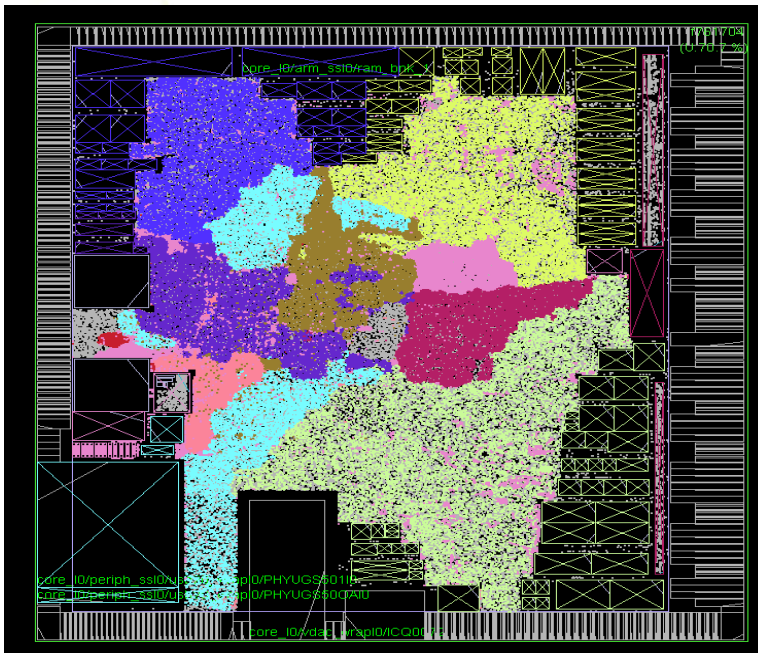
- Drivers
- Chip Support Libraries
- Operating System
- Image Pipeline
- Image Quality & Tuning Tools
- QA Testing Support

## Defined API

- Video and Audio Codecs
- Customers can customize or use their own codecs and algorithms



# Floorplan



- 90nm with 5 metal layers
- 1.3V core voltage
- ~2.6 million gates
- ~1.7 Mbits of memory
- 12x12 package
- Major blocks
  - Dark blue – ARM subsystem
  - Yellow – Imaging and video compression
  - Light green – Video processing subsystem



## References

- SoC press release:  
<http://focus.ti.com/docs/pr/pressrelease.jhtml?prellid=sc07043>
- DaVinci technology overview and specifications:  
<http://focus.ti.com/lit/an/sprt401a/sprt401a.pdf>
- DaVinci technology – digital video innovation product bulletin:  
<http://www.ti.com/litv/pdf/sprt378d>