Hot Chips 2007
ASICs to ASSPs for Working Engineers

Building the OMAP 3430

David Witt
Texas Instruments

BOILER PLATE – Framing the Problem -

	Ch. BW	Data Rate
2G	1X	1X
3G	25X	100X (~50X)
4G	100X	1000X (~8X)

1G — Analog Cellular
- Voice
- AMPS, TACS

2G — Digital Cellular
- Voice
- Pager
- 10kbps data
- GSM, TDMA
- CDMAOne

2.5G/ 2.75G — Digital Cellular
- Voice
- Email
- Photos
- Web
- ~100kbps data
- GPRS/EDGE
- CDMA 2000 1X

Today

3G — Wide-Band Digital Cellular
- Video
- M-pixel cam.
- 3D
- 300kbps
  - 14Mbps
- UMTS, HSDPA
- CDMA 1X EVDO

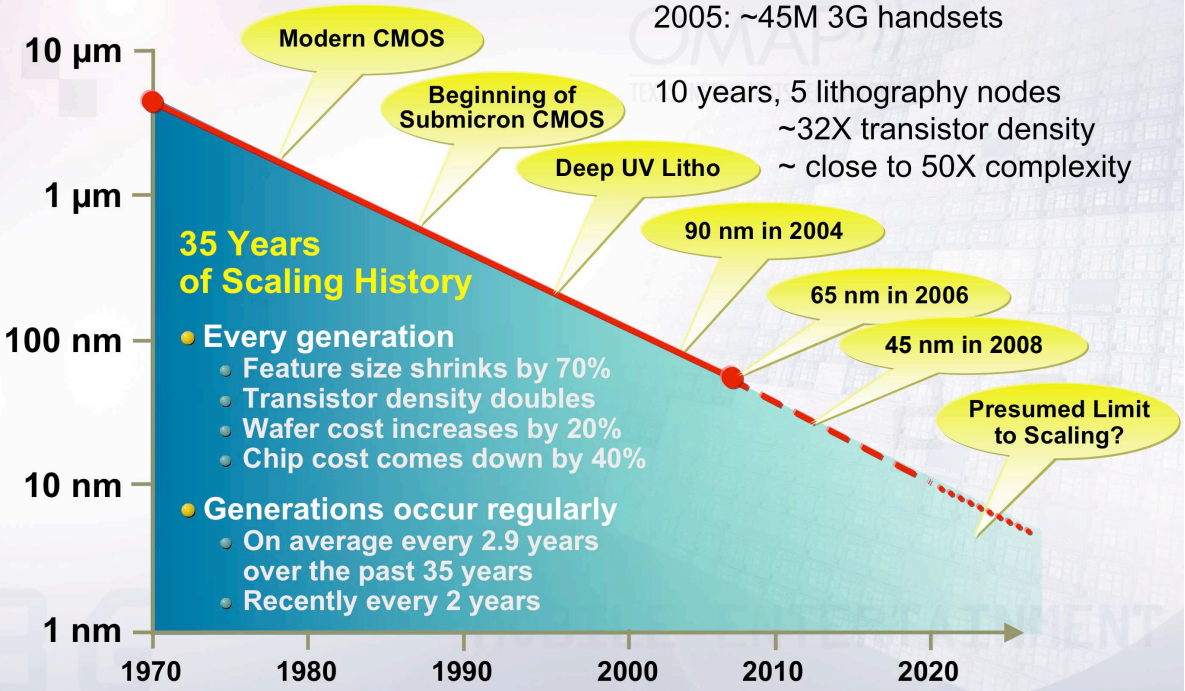
3.9G/ OFDM — Wide-Band Digital Cellular
- Video
- High-end gaming
- 100 Mbps, 10msec
- Flexible bandwidth
- All IP Network
- Super 3G/LTE
- OFDM (MIMO)
- WiBro/WiMAX

4G — Wide-Band Network
- Ubiquitous data
- Flexible Spectrum use
- Enhanced apps.
- 100Mbps – 1Gbps
- OFDM

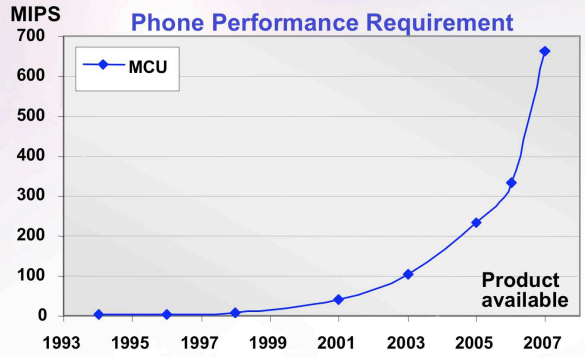
BOILER PLATE – Process Migration

1995: ~20M 2G handsets
2005: ~45M 3G handsets

10 years, 5 lithography nodes
~32X transistor density
~ close to 50X complexity



BOILER PLATE – Advanced Process and Leakage – and a Phone

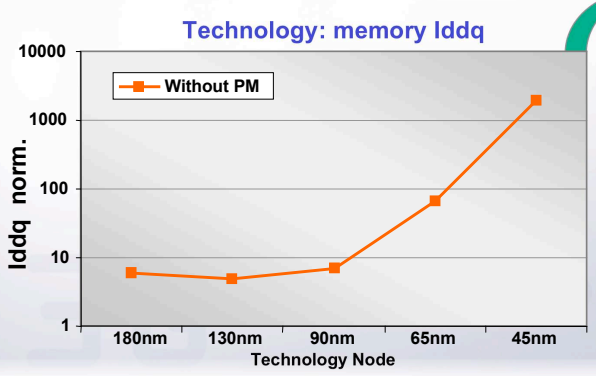


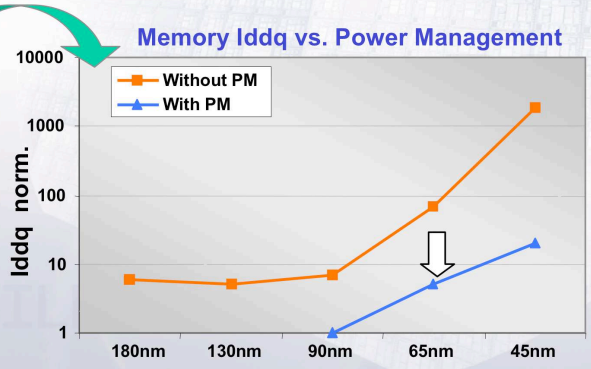
Talk Time: Pwr_Active = CV^2F + Leakage

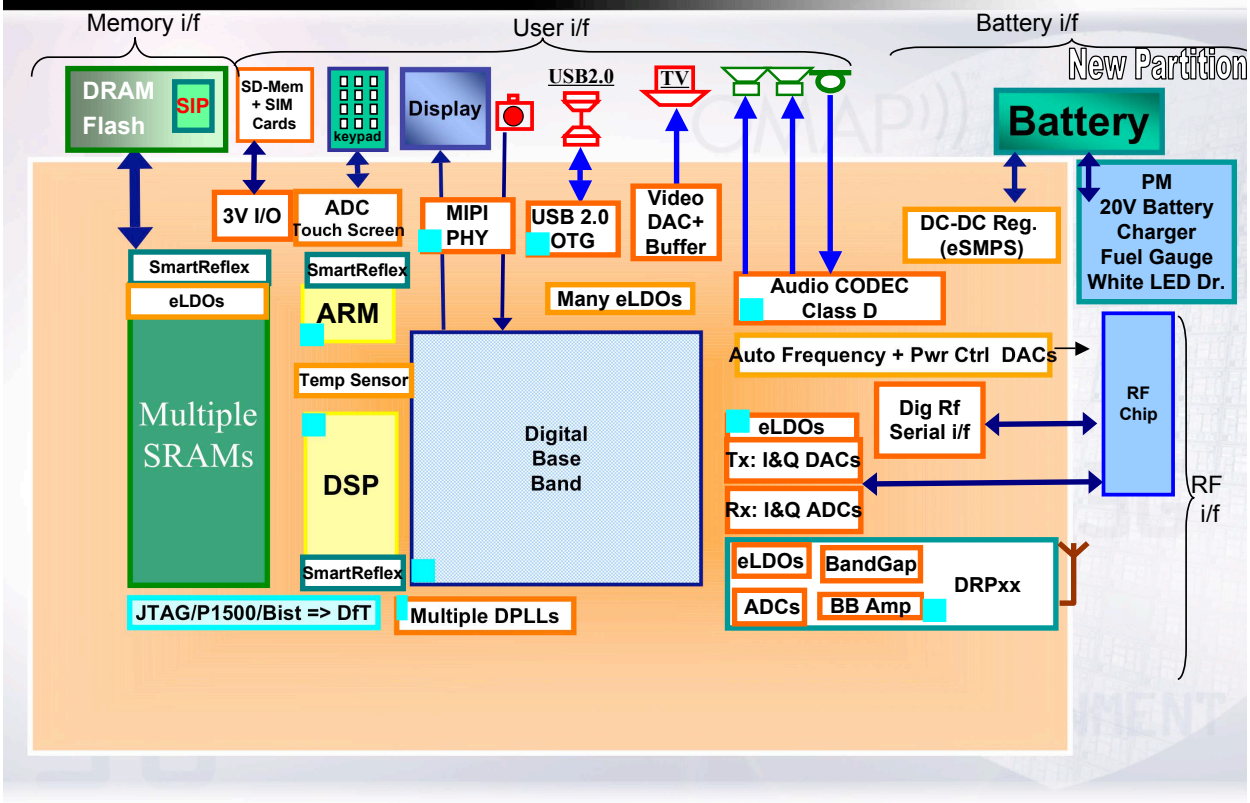
- C: Decrease/node,offset by complexity
- F: Increases/node
- Leakage: Increases/node, temp.

Standby Time: Pwr_Idle = Leakage

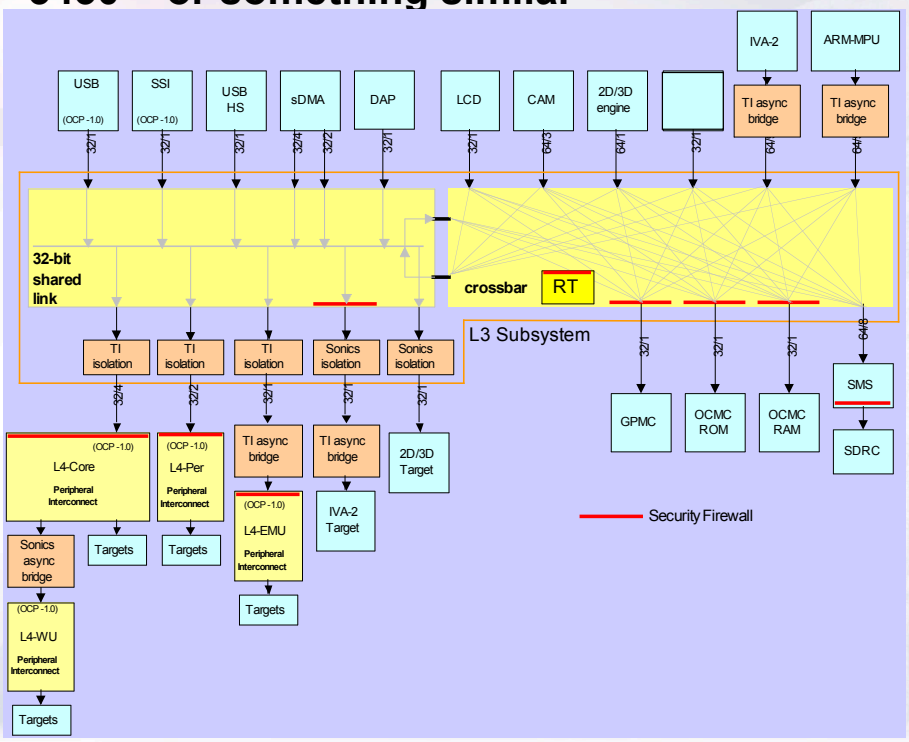
- Leakage: Increases/node, temp







OMAP 3430 – or something similar –



Walk thru the past in building ASIC "complex things"

- What killed us in the past??
  - Predicting performance – and trends in applications
  - Verification – many IPs / many teams
  - Hookup errors – 100 IPs 10K to 100K signals
  - Arch /spec – what is it you really wanted
  - Standards for power/security
  - Timing closure – guidelines/predictability
  - Process – advanced/models/stability
  - Analog/ESD and the integration of same

MakingWireless

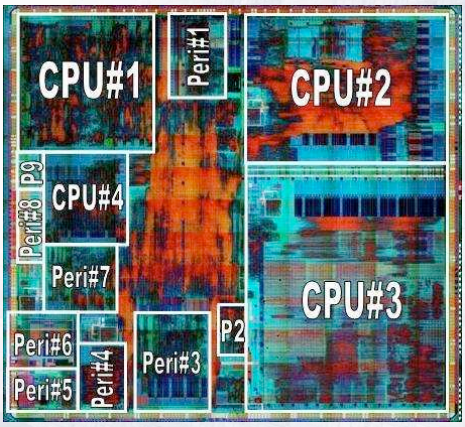
OMAP/application modeling – ASIC 101..

- Level set architecture before "aircraft carrier gets going"
- System C based models
  - Processors
  - Accelerators
  - Caches
  - On chip interconnect
- Enough insight to predict direction
- About 1.5 year MAX – prediction to tape
- We must understand and close in this time or die..
- We think things are IP – or SOC – not both ..

Technology for Innovators™ Texas Instruments

What was new in the OMAP 3430 and why??

- Cortex A8 – CPU
  - ARM v7 ISA
  - 2 issue very high clock/low power
  - NEON dsp/ float extensions..
  - First to deploy..
- Programmable DSP accelerators..
  - Audio/video/imaging
  - Flexibility/high performance
- New 3G graphics core
  - Open GLS2.0
- Camera high speed interface
  - With sensor/lens preprocessing
- Latest and greatest displays
- Software upgrades from 2430
- 65nm 7LM LP TI process
  - Advanced process
  - Advanced power management
  - Only way to fit in all “stuff” and still be able to ship high volume..



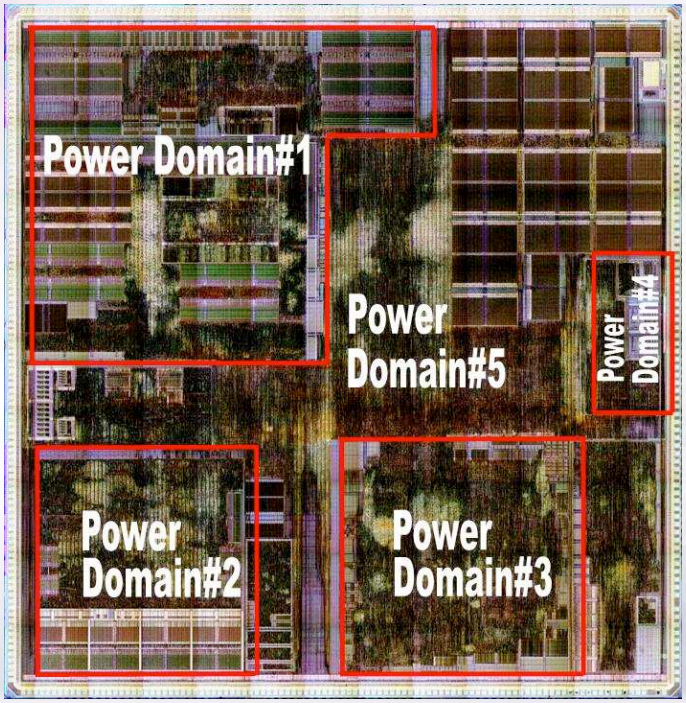
OMAP 3430 ES1

Sept 2006

Our ASIC – OMAP/Modems - Manage Power

- See first slides
  - Model
    - Use case scenario
    - Spreadsheet/and early model
  - Variables on chip
    - Voltage domains – 4 to 10 to ??
    - On chip voltage – 3
  - Interfaces – Bring up/down
    - Important to find a way to manage
      - Power off/good – and State Machine
      - Standardize /automate – or bug farms
  - Defined standards – handling power and control
    - Nobody can roll your own -

Power Management – 90nm=50x – today at 65nm=10Kx



- One Voltage Domain
- SRAM Retention
- 5 Power Domains
  - #1: MCU Core
  - #2: DSP Core
  - #3: Graphic Accelerator
  - #4: Core + Periphery
  - #5: Always On logic
- 90 nm CMOS Technology
- ~90M transistors

OMAP 2420 circa 2004

OMAP/Modem ASICs - Security

- Another standardization/requirement
  - GSM standard for my flash/modem authenticity and encryption
  - Digital contents Rights management standards
  - Secure transaction etc etc etc..
- Our ASICs
  - Designs must reflect a method of standardizing
    - Software/firmware/common platform
    - Hardware accelerators/on chip firewalls/propagated secure mode
    - We must insure – no hackers in phones /apps – this is real money ..
- Technique
  - Define well thought out mechanism and just evolve it
  - Do not break system/software migration- this is where TI $$$

Clocks/Reset/DFT

- This gets hard as designs get complex
- For TI ASIC
  - Many PLLs on chip 3 to 7 to ??
  - Standardize clock control structure/control
    - IP/top level constraints on CTS to close
  - One way to do reset – asynchr. Rest/synch set –
- DFT
  - Always adapting to new standards
  - Achieve wireless <200 to 300 DPM and low cost test
  - Design must be defect density limited – driven by volume

ASIP verification – IP and SOC – managing the bug farm…

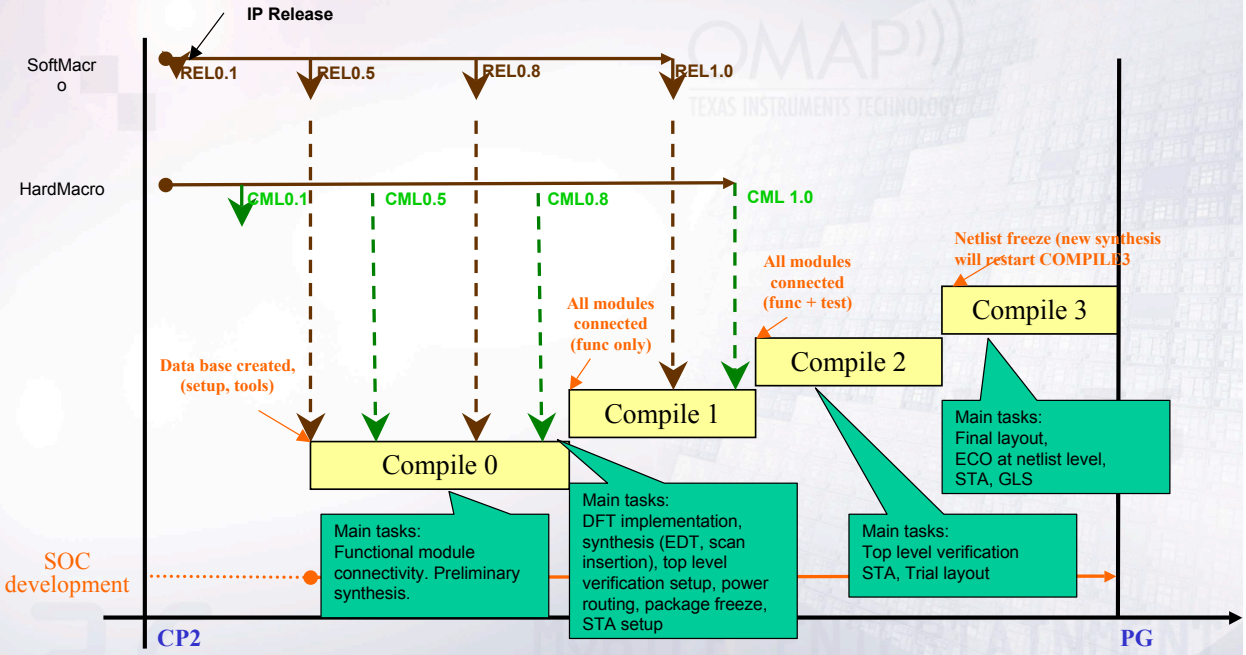
Verification Process – checkpoints / audit / reviews

Regression Manager / Verification Dashboard – DV / Defect tracking

Verification Metrics – coverage, bugs, regression, formal, cycles, efficiency tracking

Functional Coverage driven	Functional Scenario driven	Application driven
HVL test bench / scoreboard / checker / assertions	HDL test bench	
Constraint random testing Reusable test environment Reusable stimulus Exhaustive black/grey box	Directed and Random testing Mimic chip level constraints Reuse module level environment	C/ASM based directed testing Reuse from module Synthesizable test bench	Same environment as chip level Application threads Operating System boot up
Module/Block	Subsystem	Chip	Hardware

SOC and IP Release/Compiles – How we coordinate designs in flight



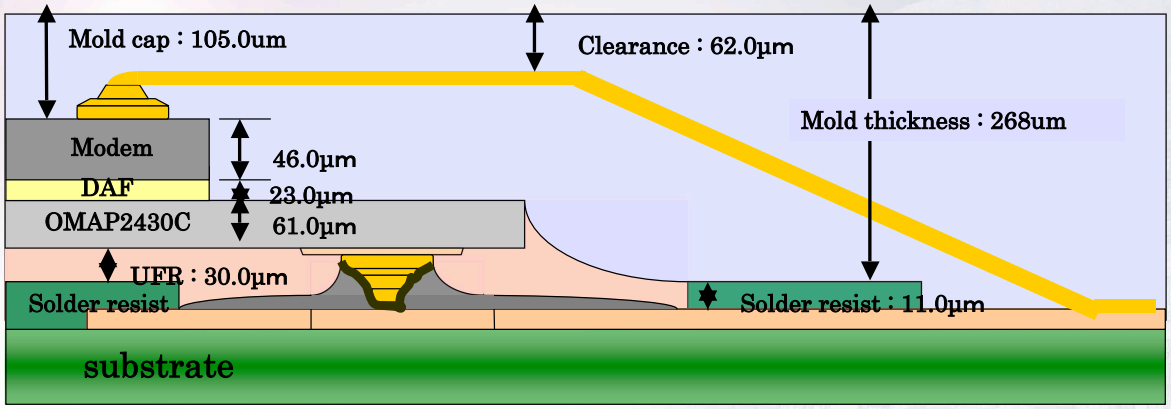
MakingWireless

Automation Tools – Avoid mistakes spec to tape

- Automated
  - Spec to SOC hookup and simple test read/write/reg
  - OCP centric IP and top level interconnect
  - Power / reset/control management
  - Configuration management/regression/progress
  - Legacy IP blocks
  - Standard tool flow RTL creation/track front end
  - Standard tool flow backend/floorplan/STA/closure
  - IP delivery and checklists/regression/

Technology for Innovators™ Texas Instruments

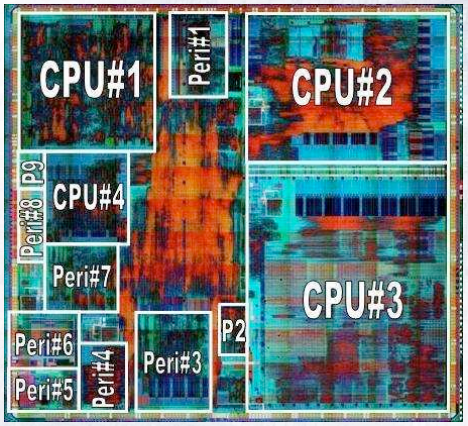
OMAP/Modem ASIC – it is not just a digital problem..



ACTUAL PACKAGE X-SECTION

OMAP 3430 ES1 First Silicon – a picture/snapshot

- Tape Aug 2006
- First Silicon Oct 2006 – ES1
  - At typical process
  - Cortex A8 >700MHz
  - Booted all major O/S off first silicon
  - Full 3d/video/O/S – 3GSM @ 1GHz
- Coming to a phone in 2008
- A successful apps part
- A successful flow



Lessons learned OMAP 3430…

- What worked
  - Almost everything
  - Digital design becoming predictable – just big verif tasks.
- What do we need to focus on
  - ESD – still a bit of a black art – better models/rules especially analog /complex/high speed I/O
  - Analog/digital integration – “boundary” models
  - Routing/utilization/area prediction – new tools
  - Packaging – mixing analog/PM/RF/memory
  - Modeling – especially analog/PM/RF/memory
  - Yet another process – 45nm/32nm..

Making Wireless

Thank you
And thanks to WW OMAP 3430 team -

Technology for Innovators™ Texas Instruments