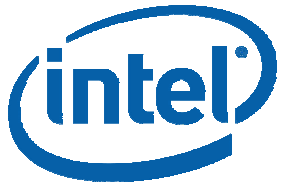

Inside Intel® Core™ Microarchitecture

Jack Doweck

Lead Architect

Intel® Corporation

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64-bit Intel® XeonTM processors with Intel® EM64T requires a computer system with a processor, chipset, BIOS, OS, device drivers and applications enabled for Intel EM64T. Processor will not operate (including 32-bit operation) without an Intel EM64T-enabled BIOS. Performance will vary depending on your hardware and software configurations. Intel EM64T-enabled OS, BIOS, device drivers and applications may not be available. Check with your vendor for more information.

SPECint2000 and SPECfp2000 benchmark tests reflect the performance of the microprocessor, memory architecture and compiler of a computer system on compute-intensive, 32-bit applications. SPEC benchmark tests results for Intel microprocessors are determined using particular, well-configured systems. These results may or may not reflect the relative performance of Intel microprocessor in systems with different hardware or software designs or configurations (including compilers). Buyers should consult other sources of information, including system benchmarks; to evaluate the performance of systems they are considering purchasing.

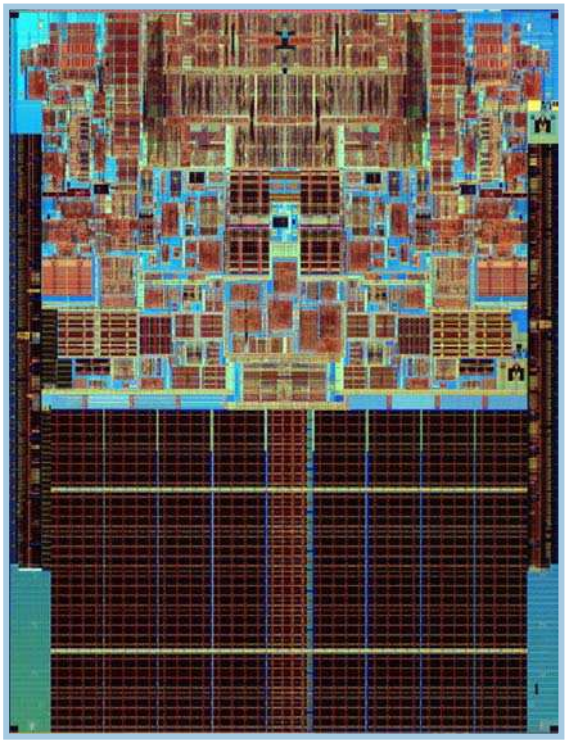
Agenda

- Processors and main specifications
- Performance data
- Intel® Core™ Microarchitecture Overview
- The Level 1 Memory subsystem
  - Structures and dimensions
  - Memory order buffer and Memory Disambiguation
  - Prefetchers
  - Shared L2 cache
- Summary

What is Intel® Core™ Microarchitecture?

The Intel® Core™ Microarchitecture is a new foundation for Intel® architecture-based desktop, mobile, and mainstream server multi-core processors

Designed for efficiency and optimized performance across a range of market segments and power envelopes



2006 Intel Core Microarchitecture based processors:

DP Server:
Dual-core Intel® Xeon® 51xx Processors
Quad-core codenamed *Clovertown*

Desktop:
Dual-core Intel® Core™ 2 Duo Processors
Quad-core codenamed *Kentsfield*

Mobile:
Dual-core Intel® Core™ 2 Duo Processors

Codenames are used for referring the products to indicate that the products and the tests are prerelease version and will change any time without further notice. Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance.

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Process:
65nm

Die size:
143 mm²

Transistor count:
291 M

Execution core area:
36 mm²

Execution core transistor count:
19 M

2006 Intel Core Microarchitecture based processors:

DP Server:
Dual-core Intel® Xeon® 51xx Processors
Quad-core codenamed *Clovertown*

Desktop:
Dual-core Intel® Core™ 2 Duo Processors
Quad-core codenamed *Kentsfield*

Mobile:
Dual-core Intel® Core™ 2 Duo Processors

Product specifications (Preliminary)

A variety of products with different specs will be available

Spec \ Codename	Xeon™ 5100 servers	Core™2 Duo desktops	Core™2 Duo mobility
Max frequency	3.00 GHz	2.93 GHz	2.50 GHz
Max Front Side Bus frequency	1.333 GT/s	1.066 GT/s	0.667 GT/s
TDP	80 W for the 3Ghz version, 65 W for lower frequency versions	75 W for the 2.93Ghz version, 65 W for lower frequency versions	34 W
Max VID	1.325V	1.325 V	1.300 V

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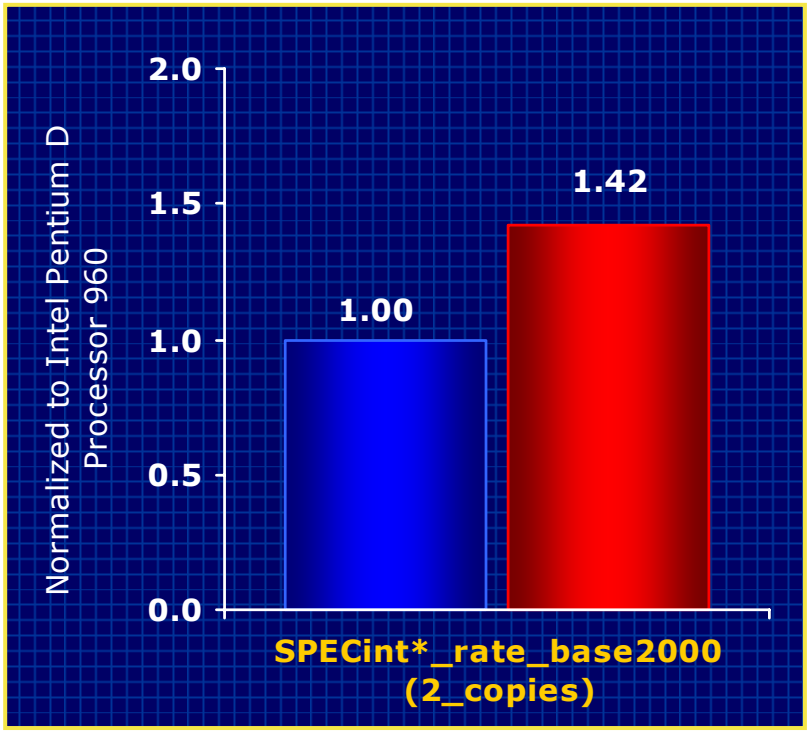
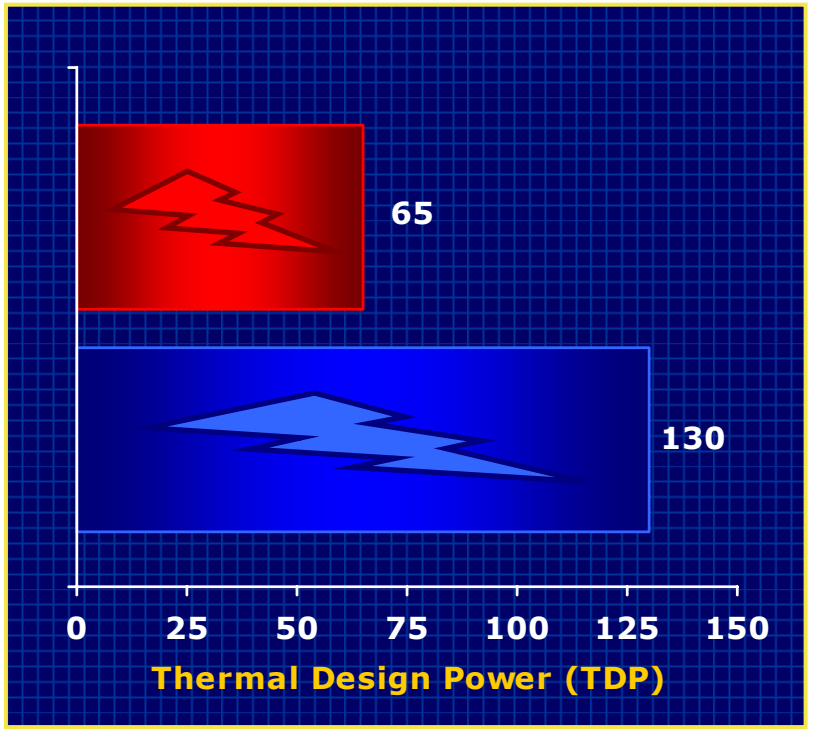
Intel® Core™2 Duo Processor:

Intel® Core™2 Duo E6700 (4 MB L2 Cache, 2.66 GHz, 1066 MHz FSB)

Intel® Pentium® D Processor 960 (2X2 MB L2 Cache, 3.6 GHz, 800 MHz FSB)





The Intel Core 2 Duo E6700 delivers +40% performance while requiring +40% less power than the Pentium D Processor 960

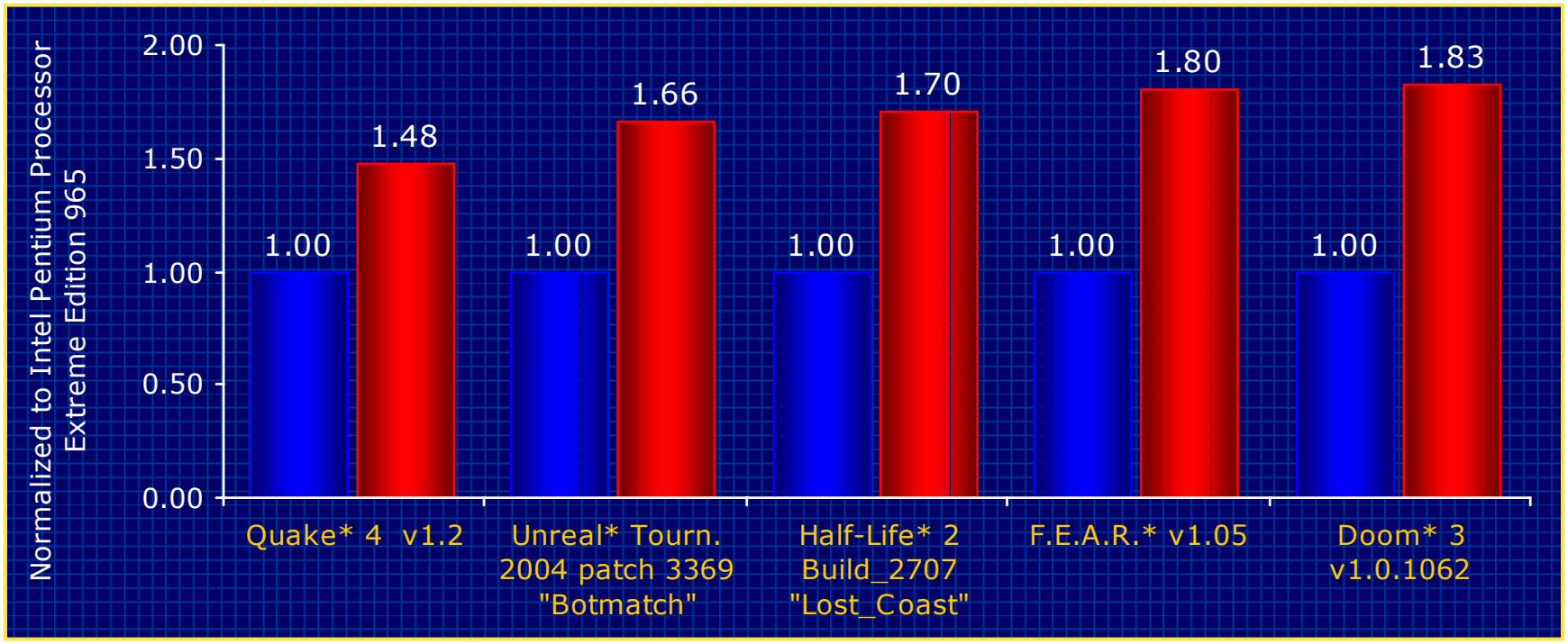
Source: Intel. **Configuration:** Processor as listed above, Intel 975X Express Chipset on Intel D975XBX board, Intel chipset software installation file 7.2.2.1006, 2x512MB Micron* DDR2 667 5-5-5-15, Intel Matrix Storage Manager 5.5.0.1035 RAID-0 Ready, Maxtor* DiamondMax* 10 300GB NCQ Serial ATA 7200 RPM, ATI* Radeon* X1900 XTX PCIe, ATI Catalyst 6.3 Driver Suite 8.23.1, Windows* XP Professional Build 2600 SP2 NTFS, DirectX 9.0c. *Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. Buyers should consult other sources of information to evaluate the performance of systems or components they are considering purchasing. For more information on performance tests and on the performance of Intel products, visit http://www.intel.com/performance/resources/index.htm*

Extreme Gaming
Intel® Core™2 Duo Processor:

Intel® Pentium® Processor Extreme Edition 965 (2x2MB L2, 3.73GHz, 1066MHz FSB) with dual graphics

Intel® Core™2 Extreme Processor X6800 (4MB L2, 2.93GHz, 1066MHz FSB) with dual graphics

Games used medium settings and 1024x768x32 resolution. These settings are used for comparing CPU contribution to game performance.



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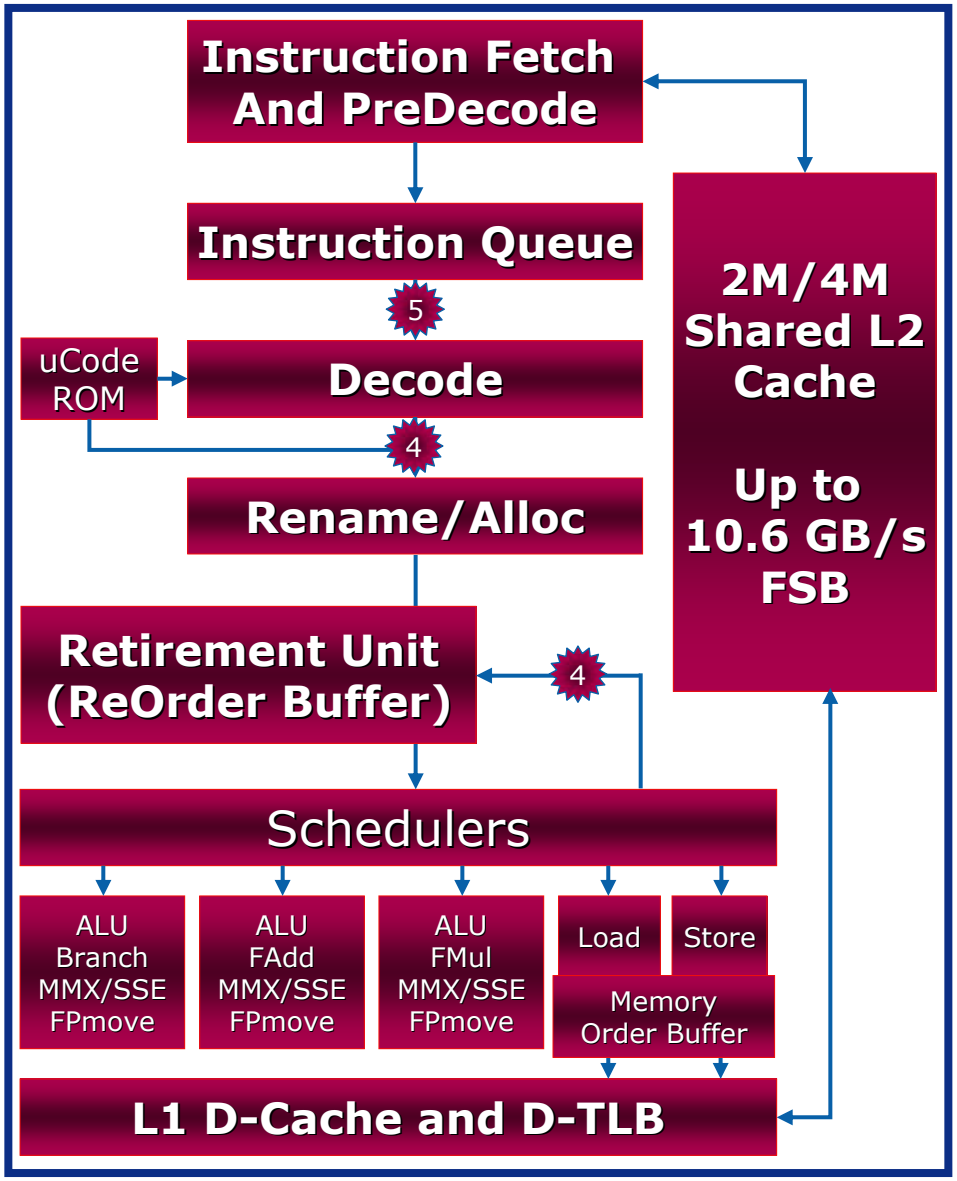
Intel® Core™ Microarchitecture - Overview



Intel® Wide Dynamic Execution

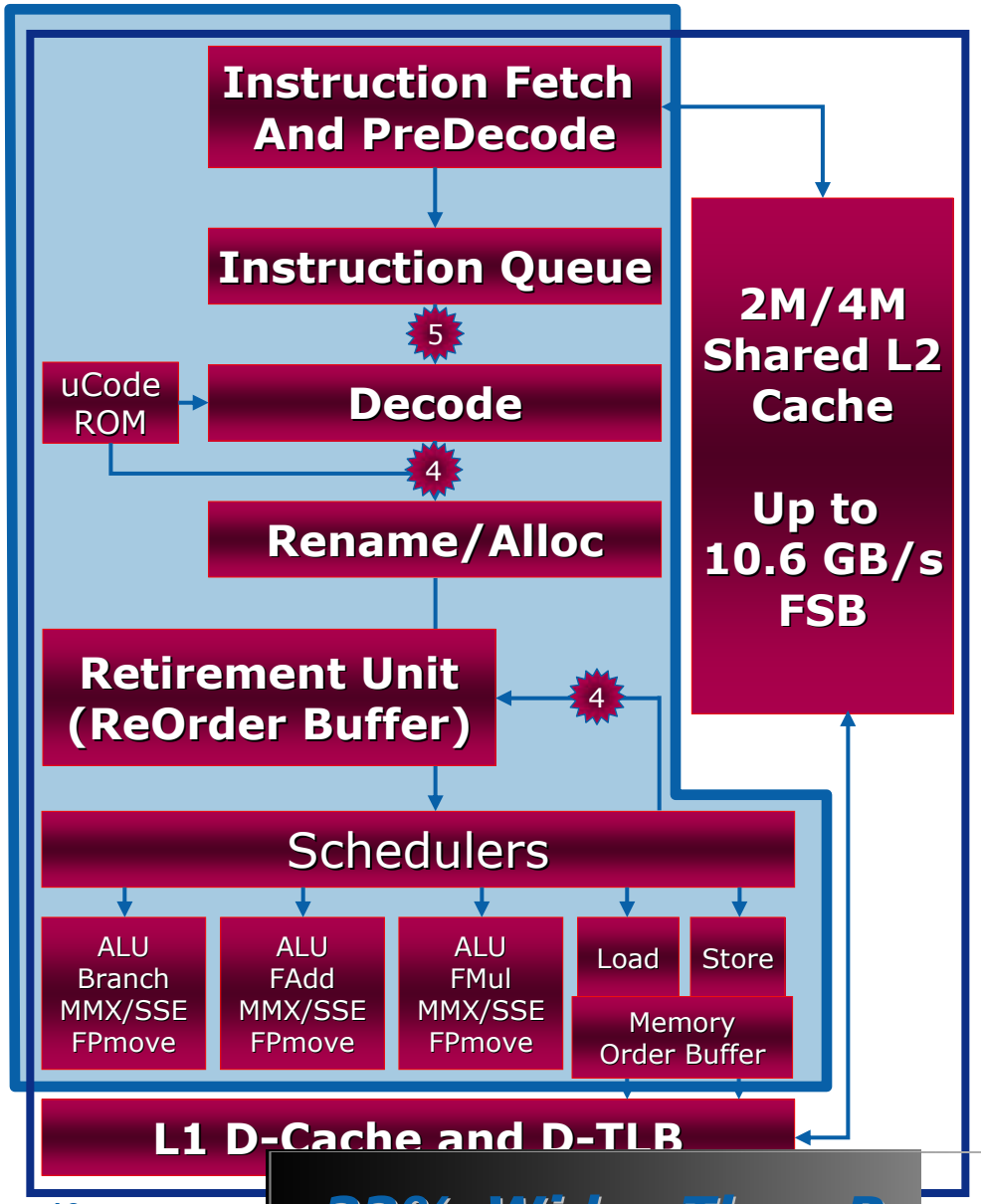
Intel® Advanced Digital Media Boost

Intel® Smart Memory Access

Intel® Advanced Smart Cache

Intel® Intelligent Power Capability

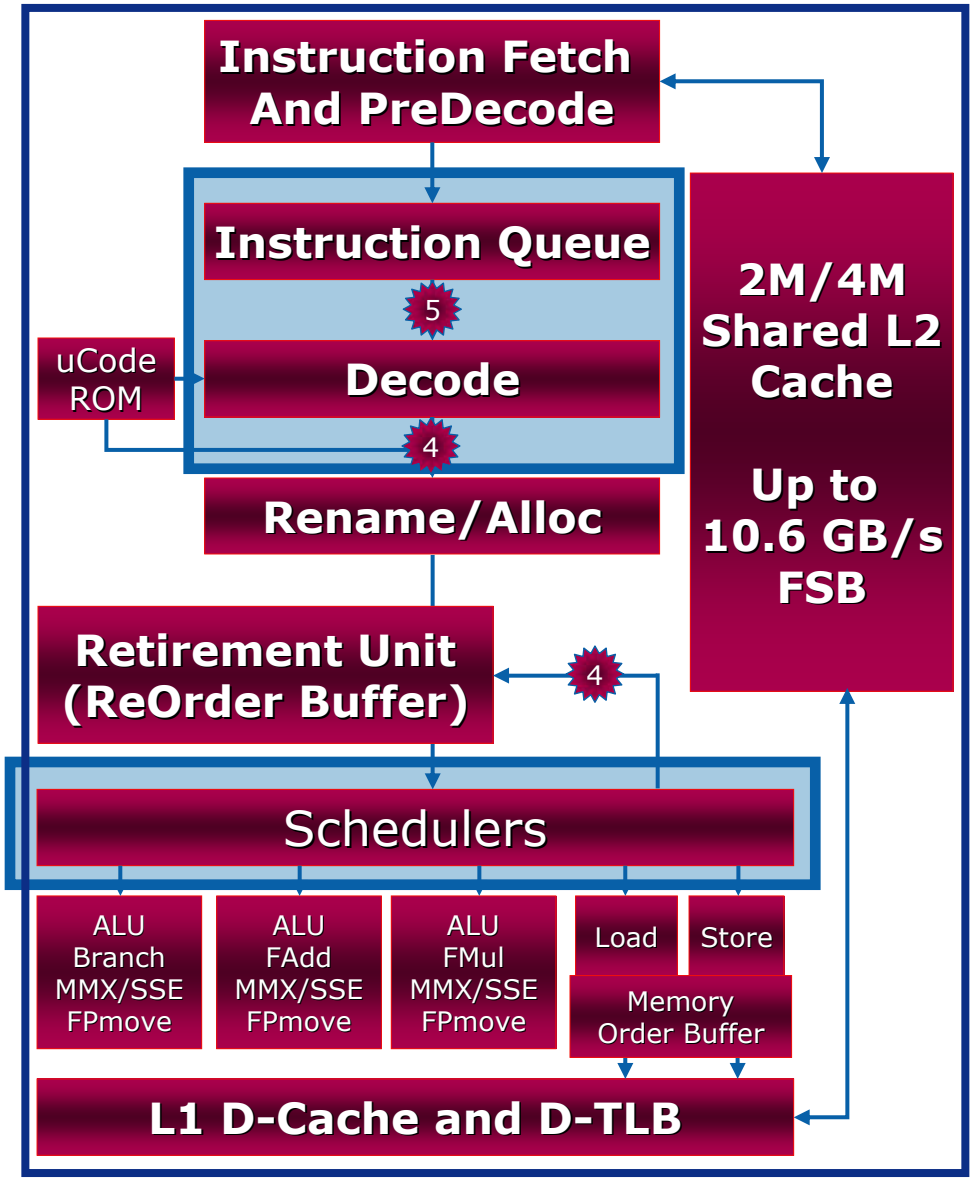
Intel® Wide Dynamic Execution



- 4 (5) wide decode
- 4 wide rename
- 4 (5) wide retire
- 5 (6) instructions/clock
- 32 entry scheduler
  (32 micro-ops considered for dispatch each cycle)
- Deep out of order storage

33% Wider Than Previous Generations

Intel® Wide Dynamic Execution (cont ..)



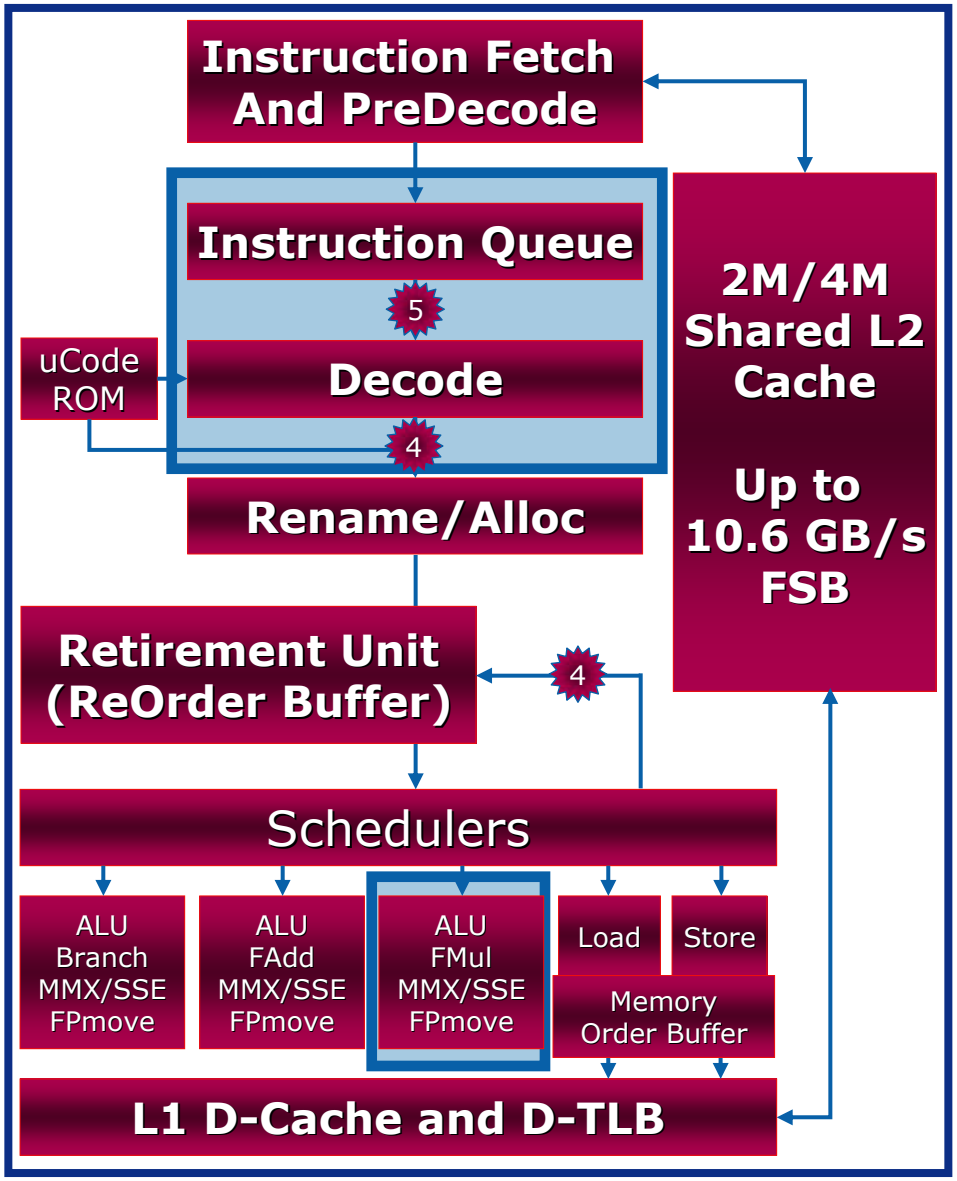
Extended Stack Pointer (ESP) tracker

- Stack Pointer updated by dedicated hardware
- SP BW increased by 33% over Core™ Duo processor

Micro-Op Micro-Fusion

- Single Uop representation of "multi-uop" instruction
- 4 instructions per cycle
- Extended to additional cases

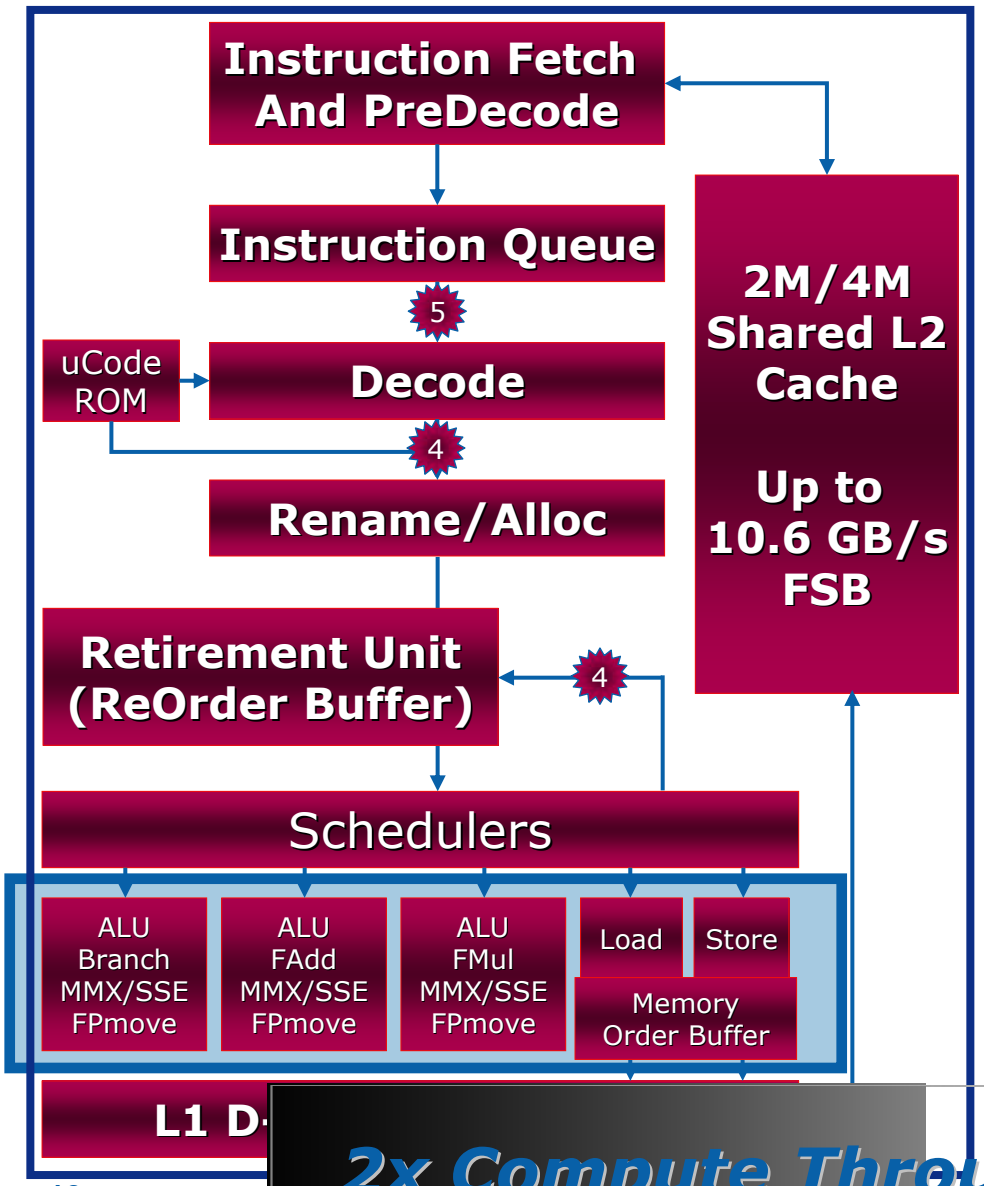
Intel® Wide Dynamic Execution (cont ..)



Macro-Fusion

- Represent most frequently used IA32/Intel® 64 instruction pair as single micro-op
- Enhanced Arithmetic Logic Unit (ALU) for macro-fusion
  - To execute new compare and jump (CMPJCC) micro-op in one clock

Intel® Advanced Digital Media Boost



128-bit packed Add

plus
128-bit packed Multiply

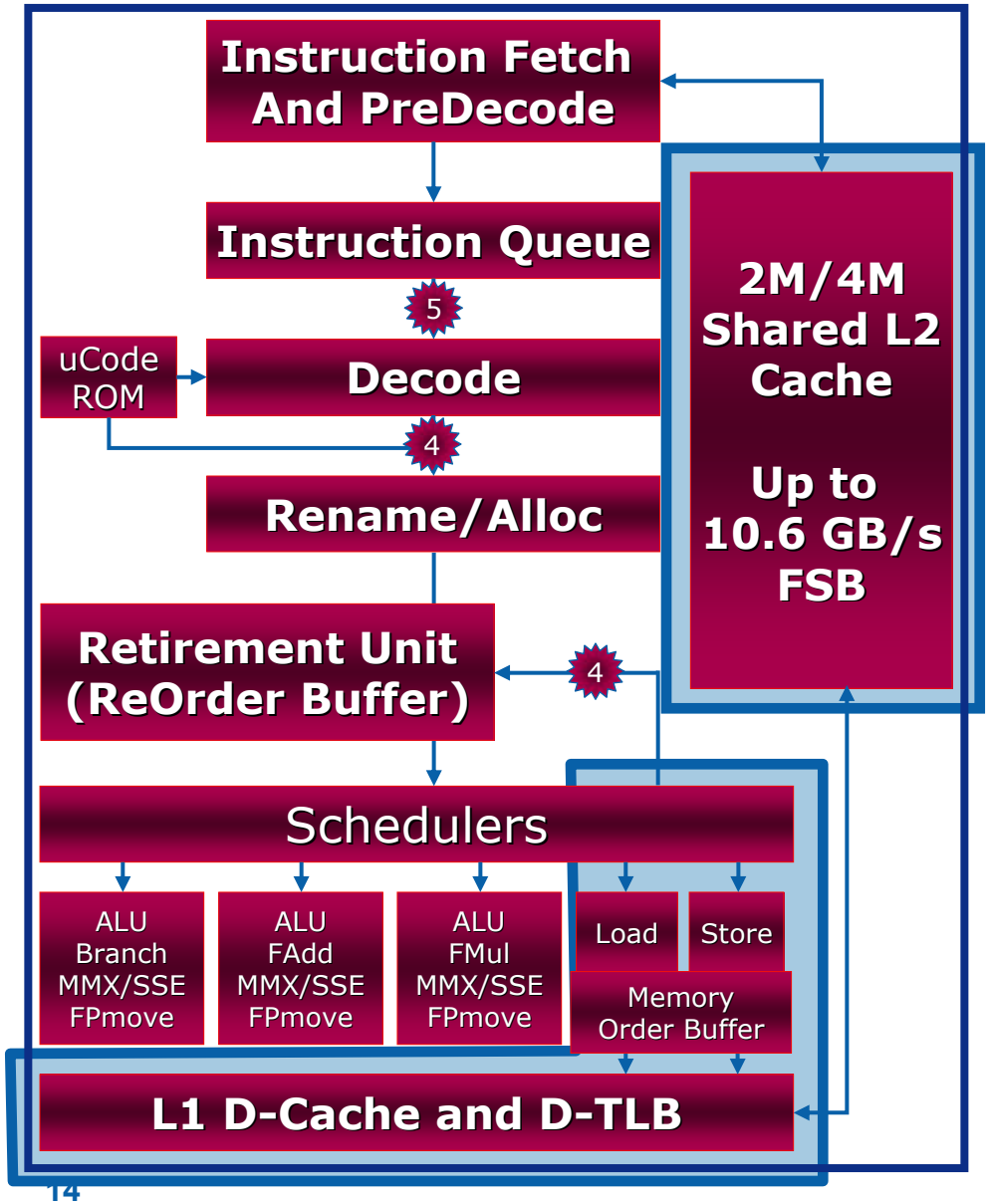
plus
128-bit packed Load

plus
128-bit packed Store

plus
one Integer instruction
(e.g.: a CMPJcc)

2x Compute Throughput / Clock

Intel® Smart Memory Access

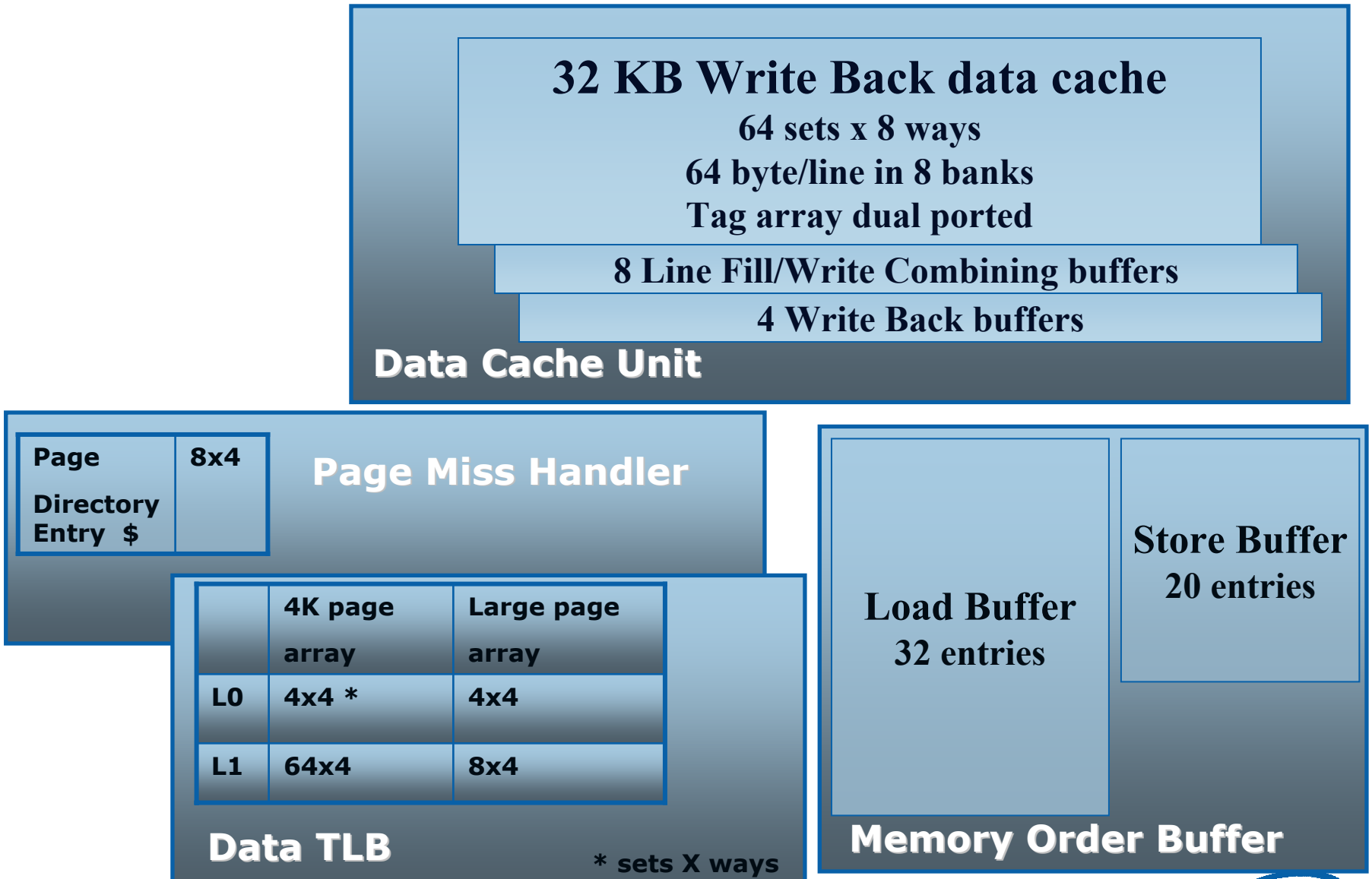


Memory Disambiguation

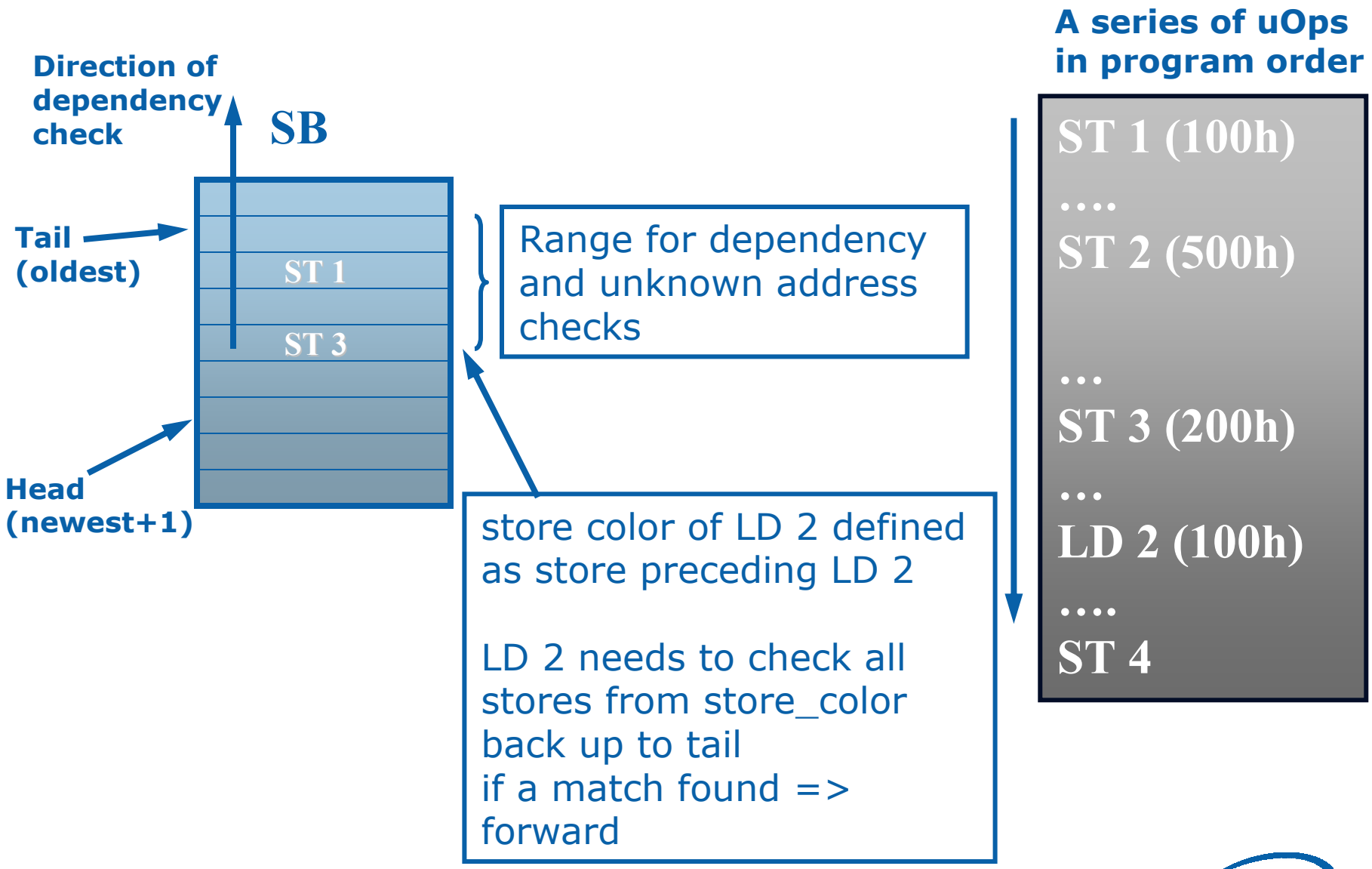
Improved Prefetchers

Hiding Latency of Memory Subsystem

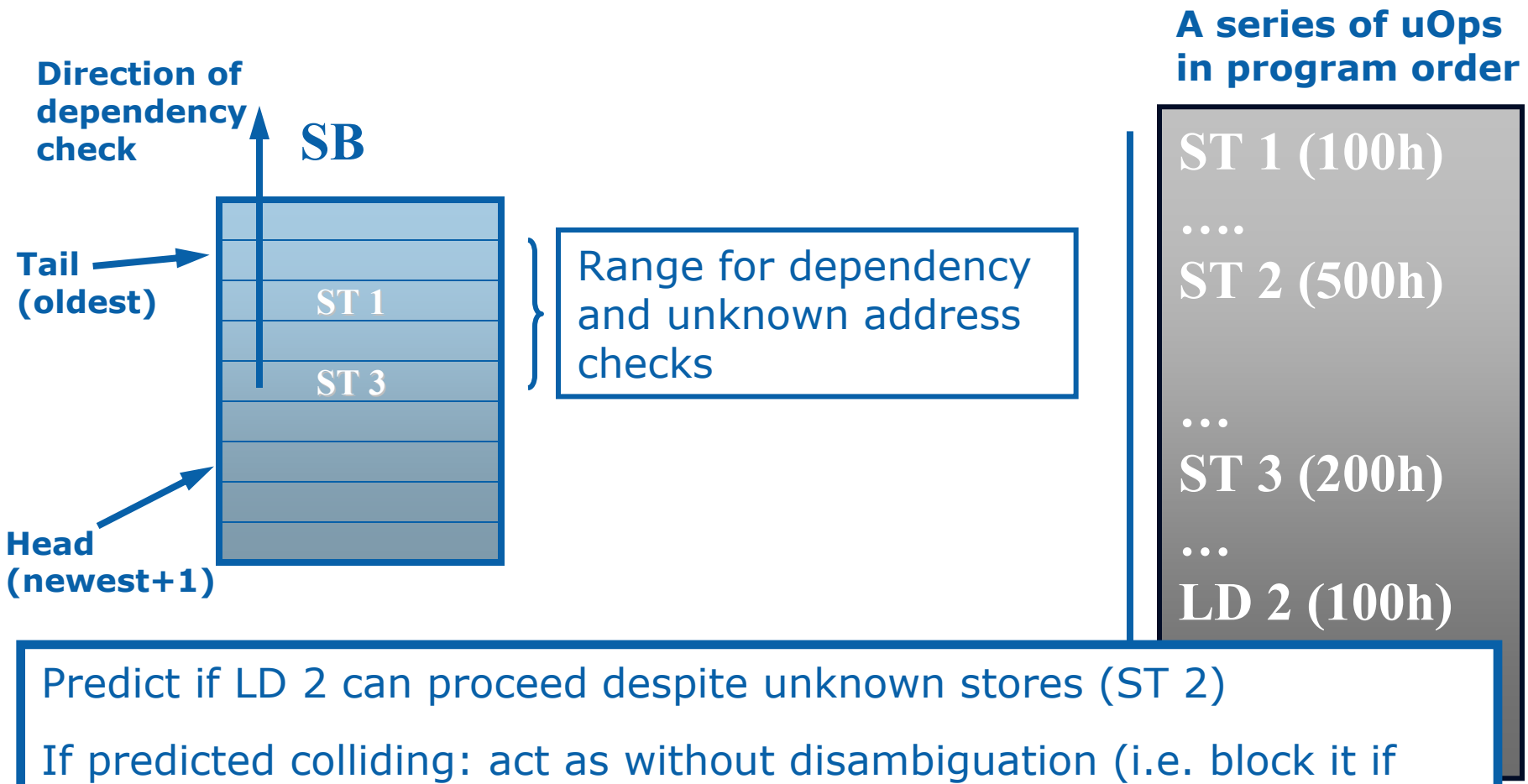
L1 memory subsystem – arrays dimensions



Example of basic MOB's ordering operation



MOB operation with Memory Disambiguation



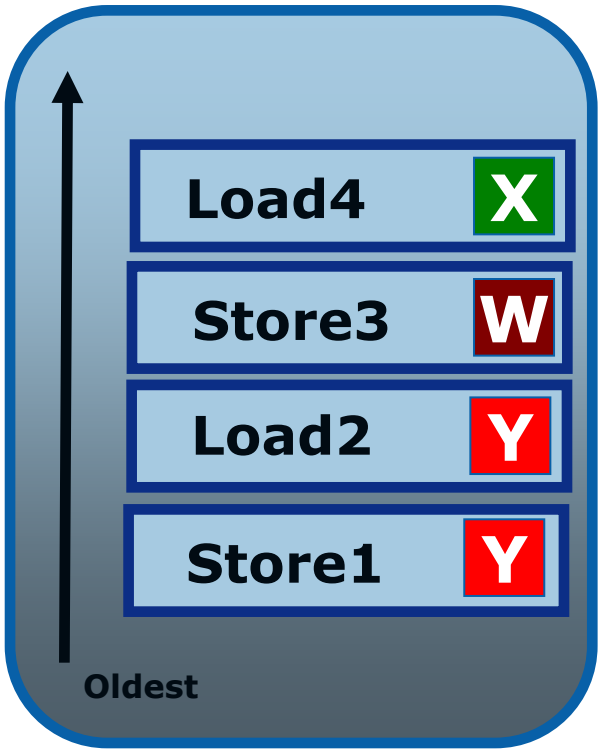
Predict if LD 2 can proceed despite unknown stores (ST 2)

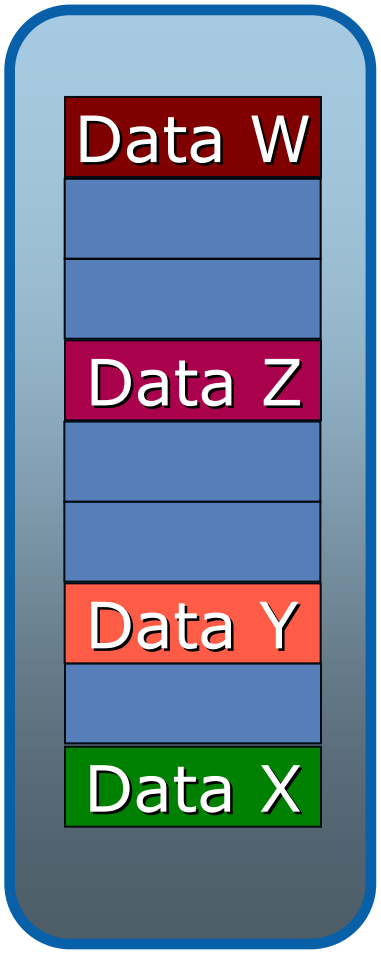
If predicted colliding: act as without disambiguation (i.e. block it if store address unknown)

If predicted non colliding:

- Let the load proceed even if unknown store address
- If actually colliding, restart the load and all successive instructions

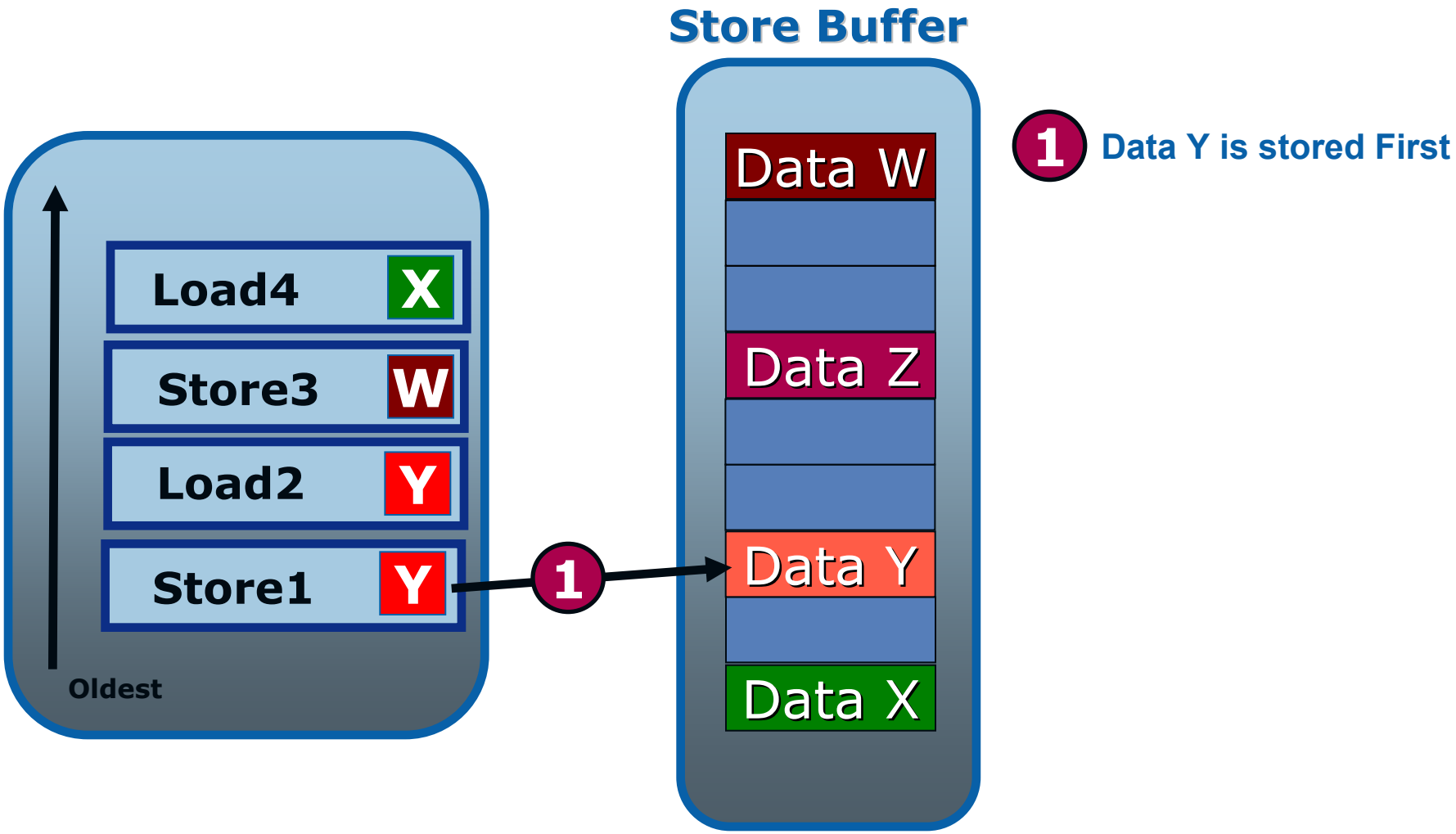
Without Memory Disambiguation



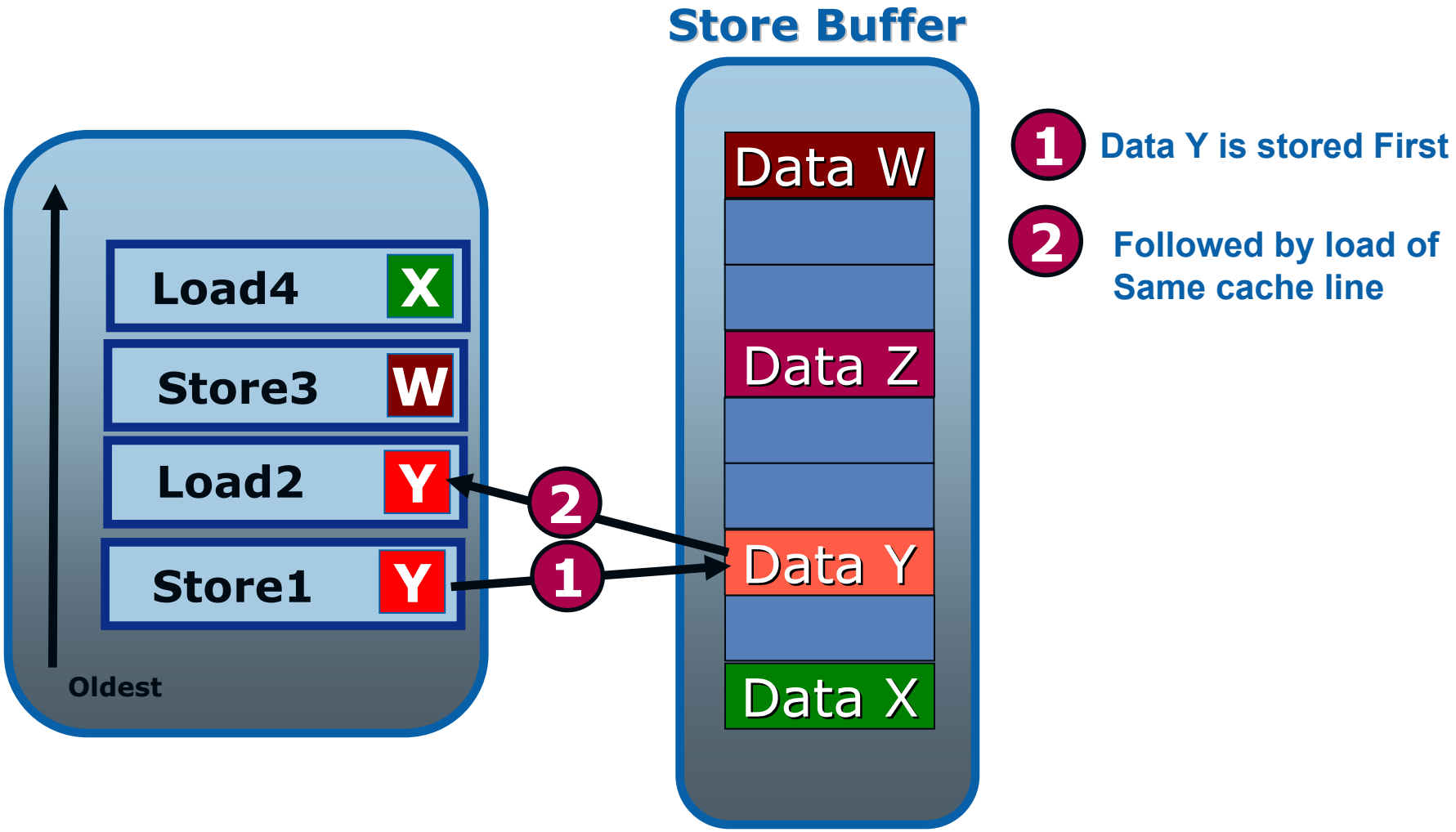


Instruction using Data X is almost ready to go, all it needs is X from memory

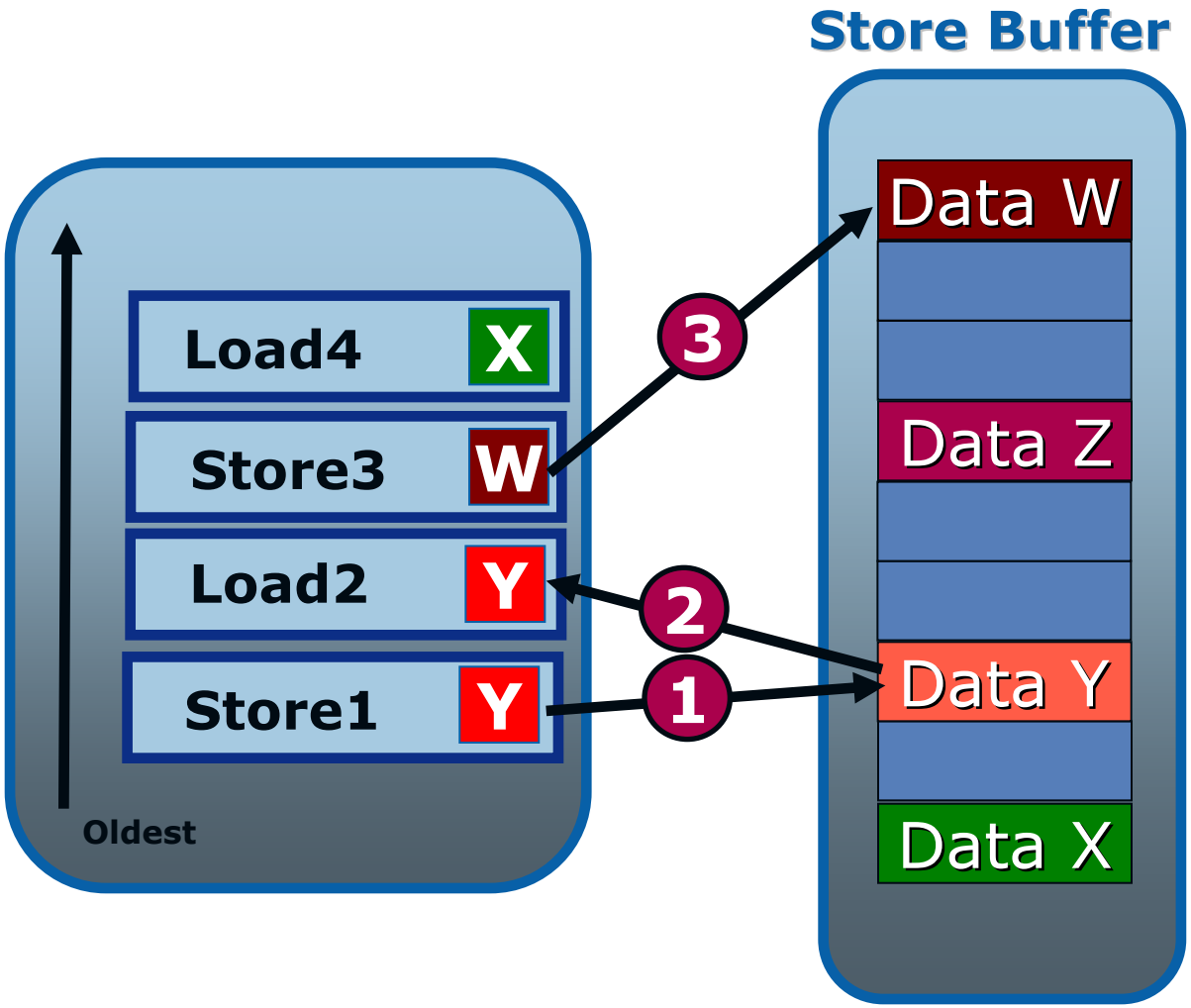
Without Memory Disambiguation



Without Memory Disambiguation

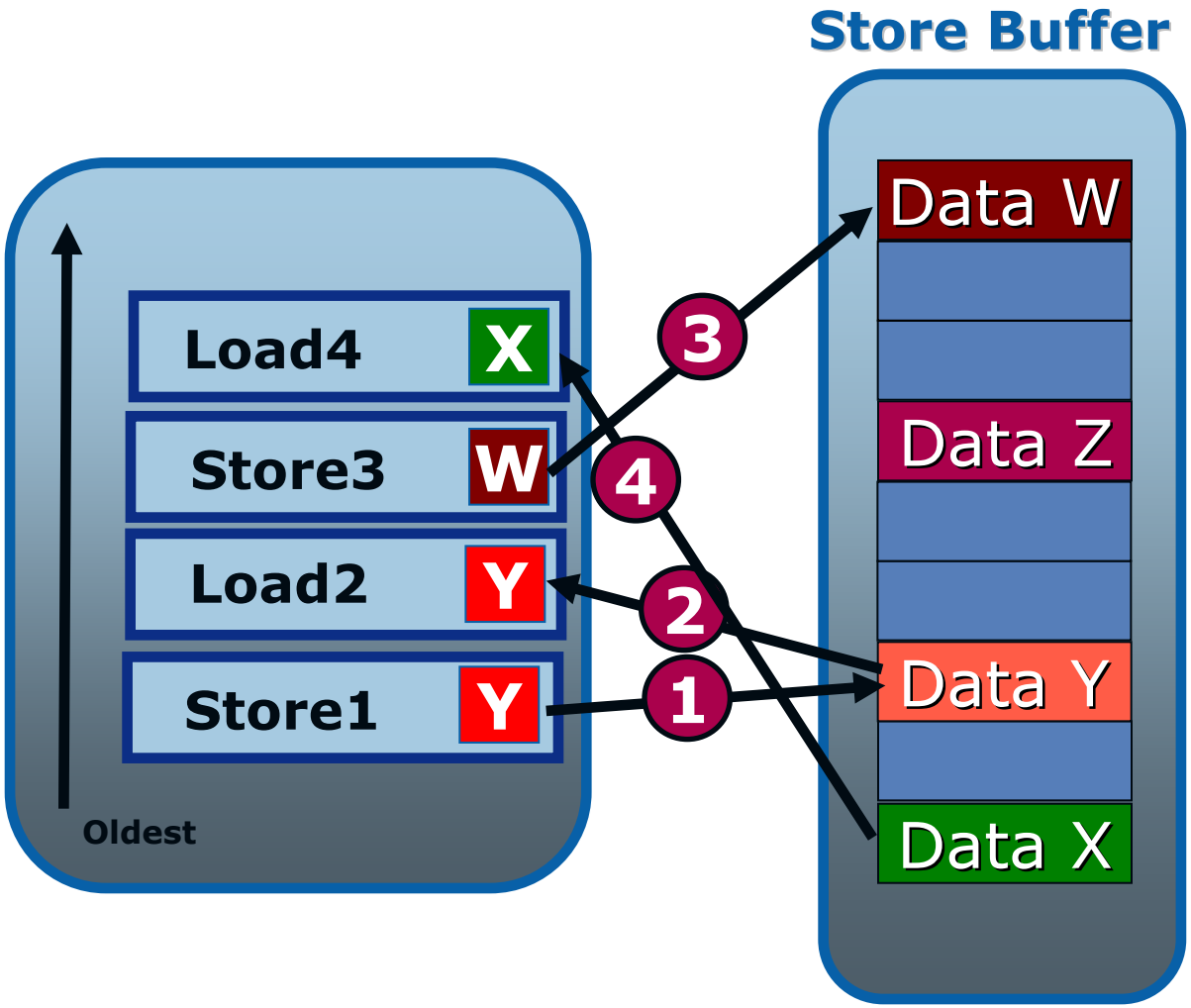


Without Memory Disambiguation



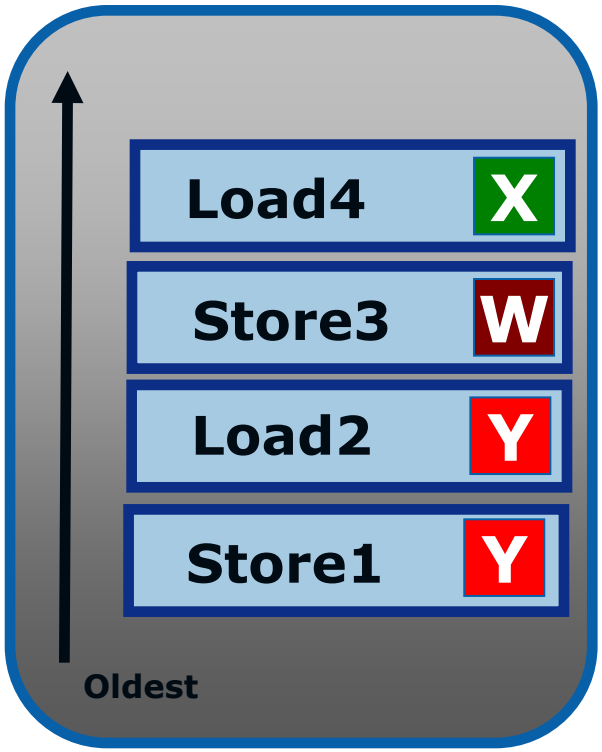
1. Data Y is stored First
2. Followed by load of Same cache line
3. Data W Store Next

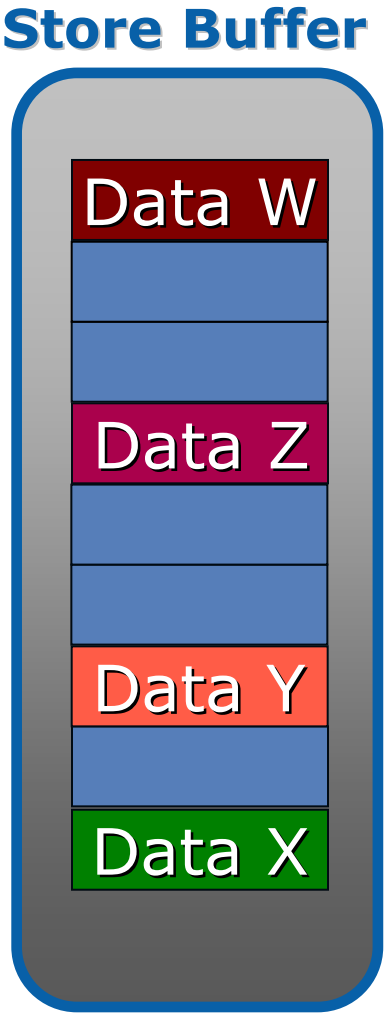
Without Memory Disambiguation



1. Data Y is stored First
2. Followed by load of Same cache line
3. Data W Store Next
4. Finally Load of X Takes place

With Memory Disambiguation

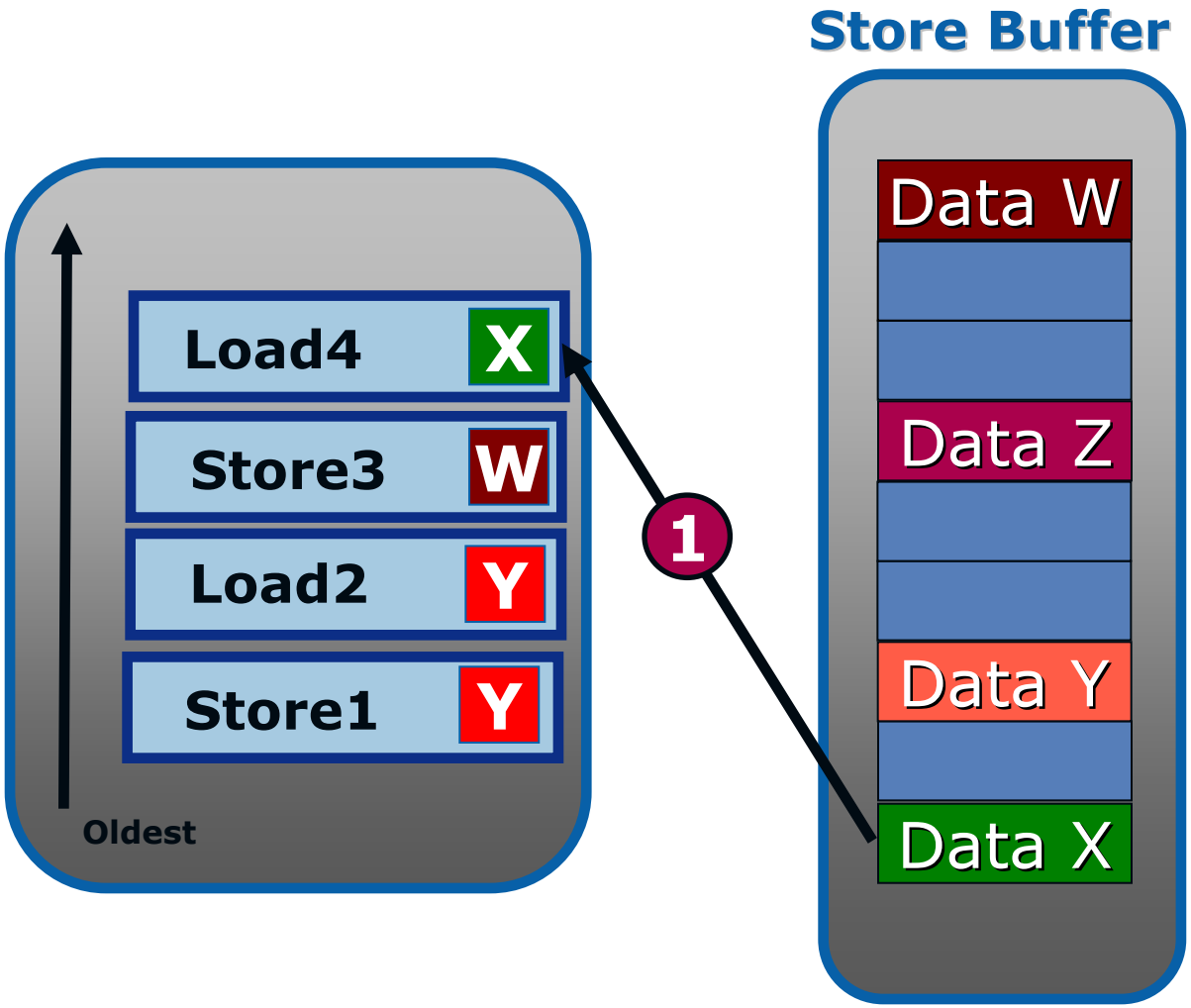




Loads can decouple from Stores.

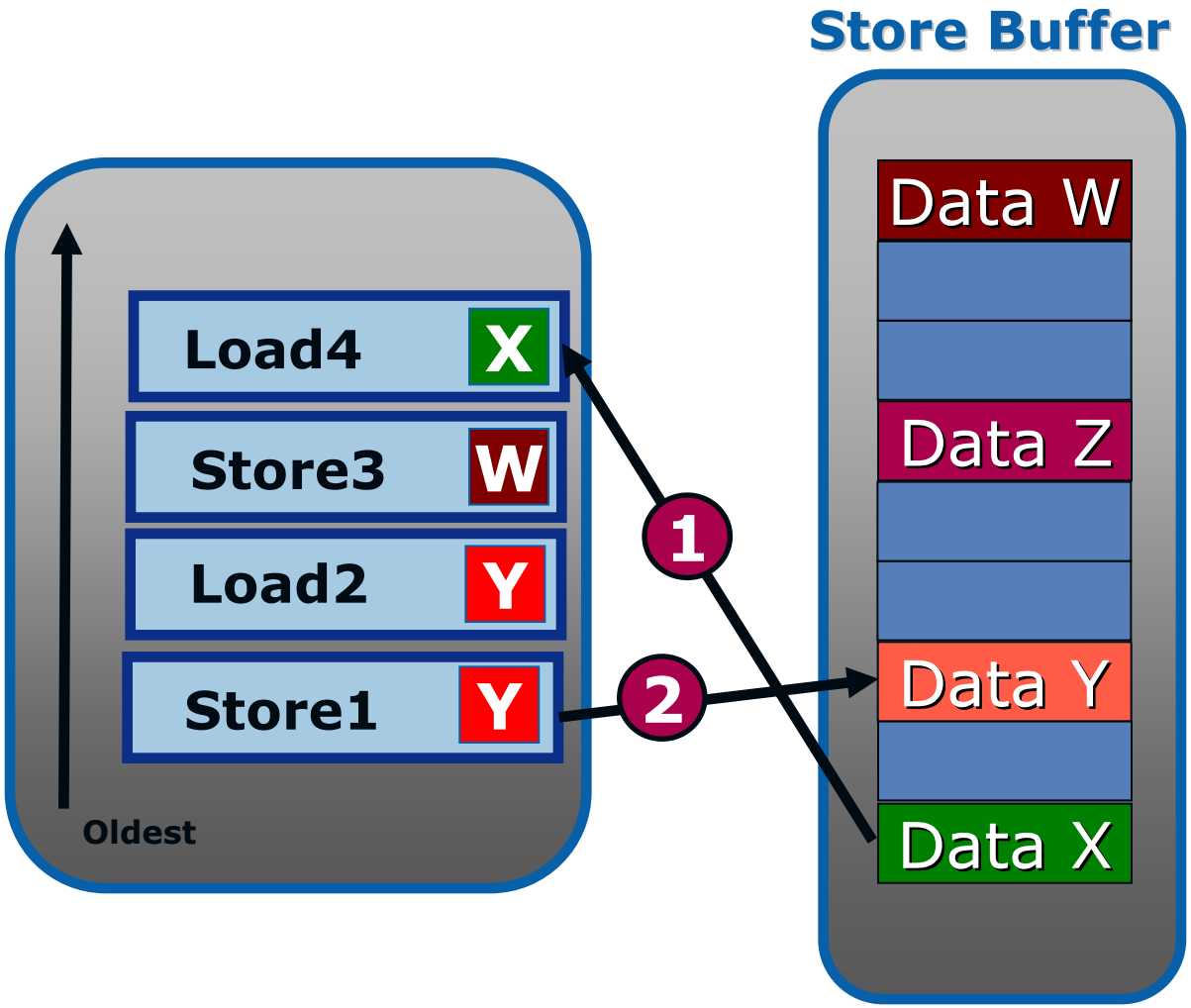
Load4 can get its data FIRST

With Memory Disambiguation



1 **Memory Disambiguation enables Load4 to go earlier**
- The dependency shadow of Load4 starts executing earlier

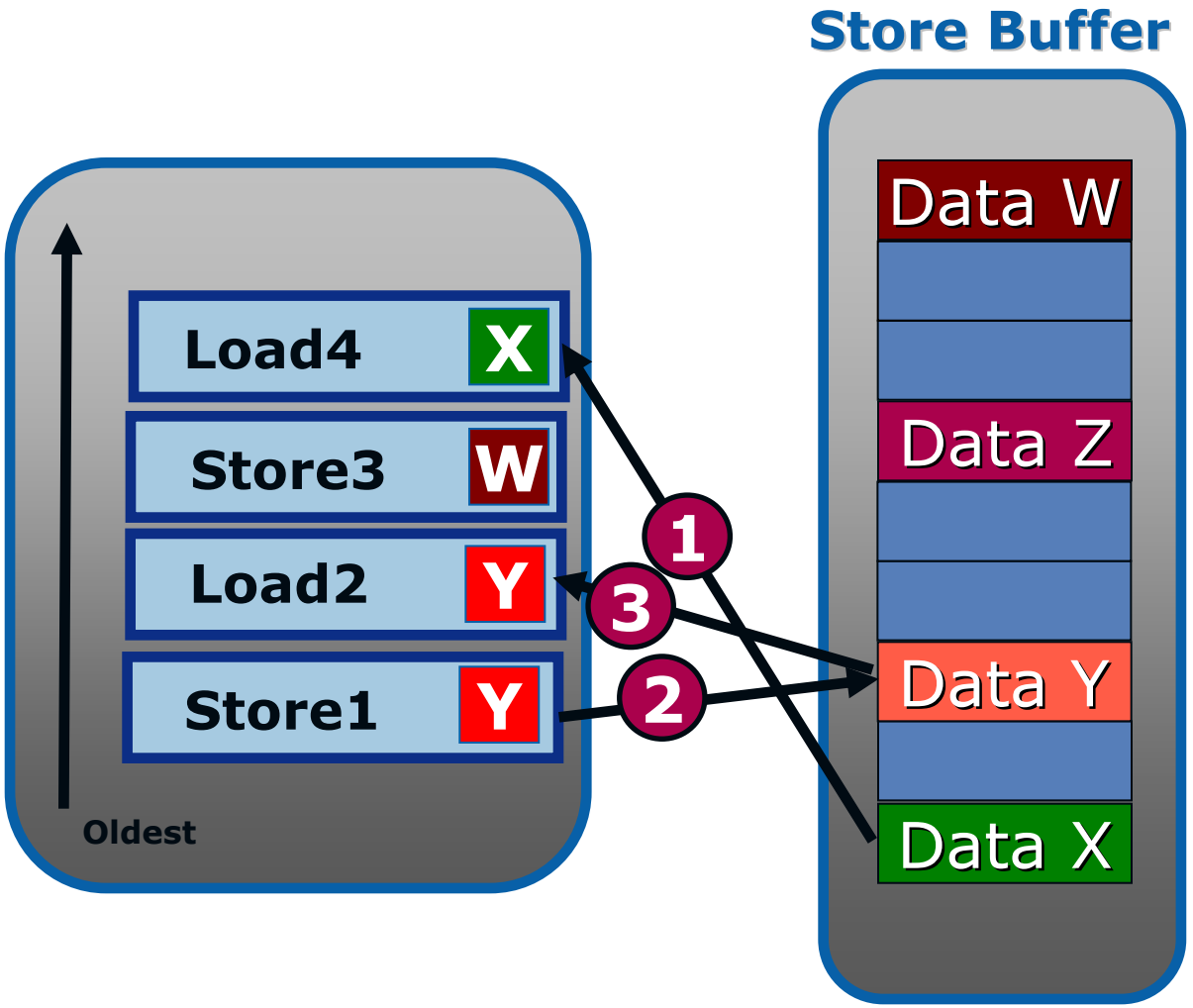
With Memory Disambiguation



1. Memory Disambiguation enables Load4 to go earlier
   - The dependency shadow of Load4 starts executing earlier

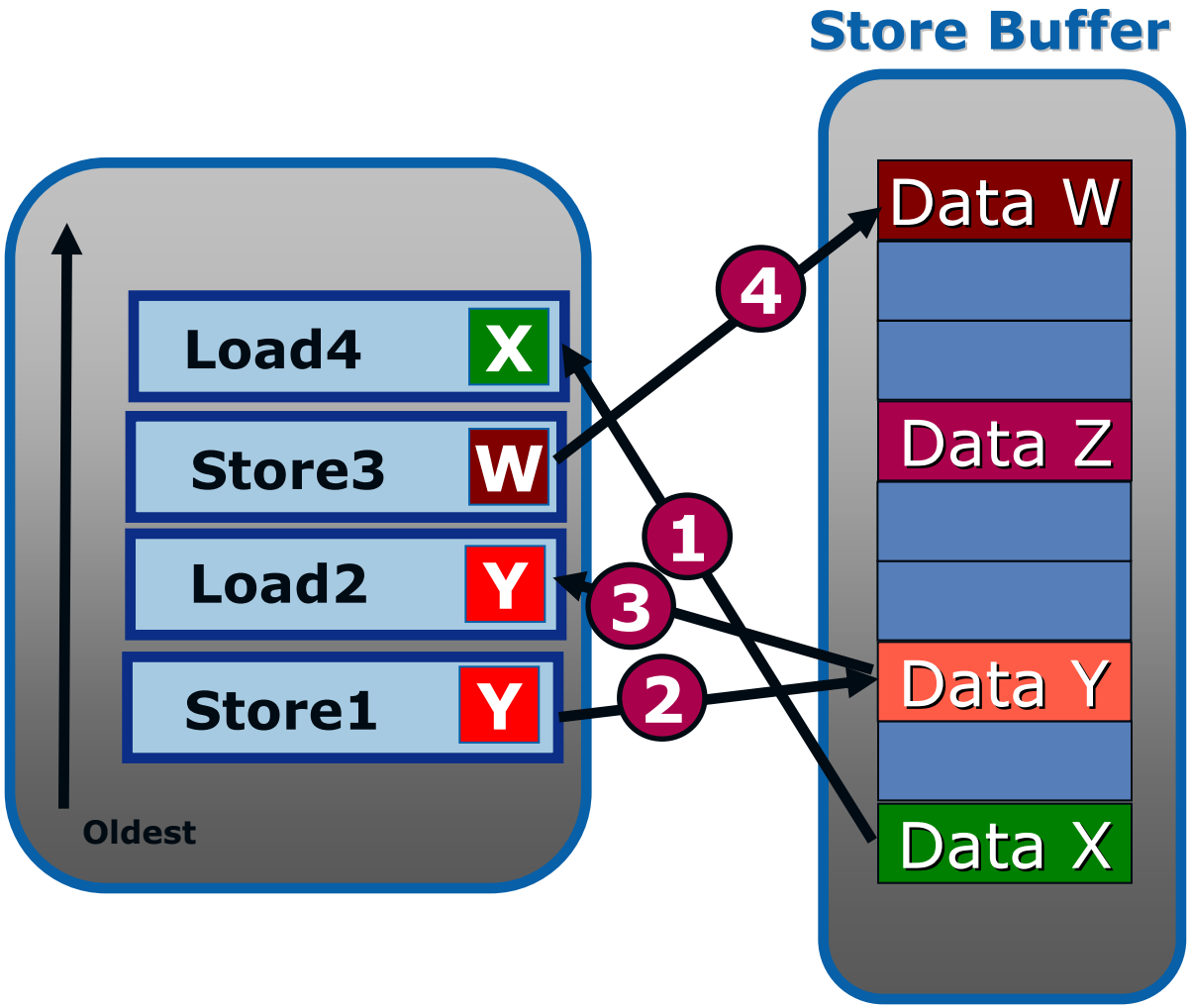
2. Store of Y can now take place and does not delay any other instructions

With Memory Disambiguation



1. Memory Disambiguation enables Load4 to go earlier
   - The dependency shadow of Load4 starts executing earlier
2. Store of Y can now take place and does not delay any other instructions
3. Load of Y is next

With Memory Disambiguation



1. Memory Disambiguation enables Load4 to go earlier
   - The dependency shadow of Load4 starts executing earlier
2. Store of Y can now take place and does not delay any other instructions
3. Load of Y is next
4. Store of W is last

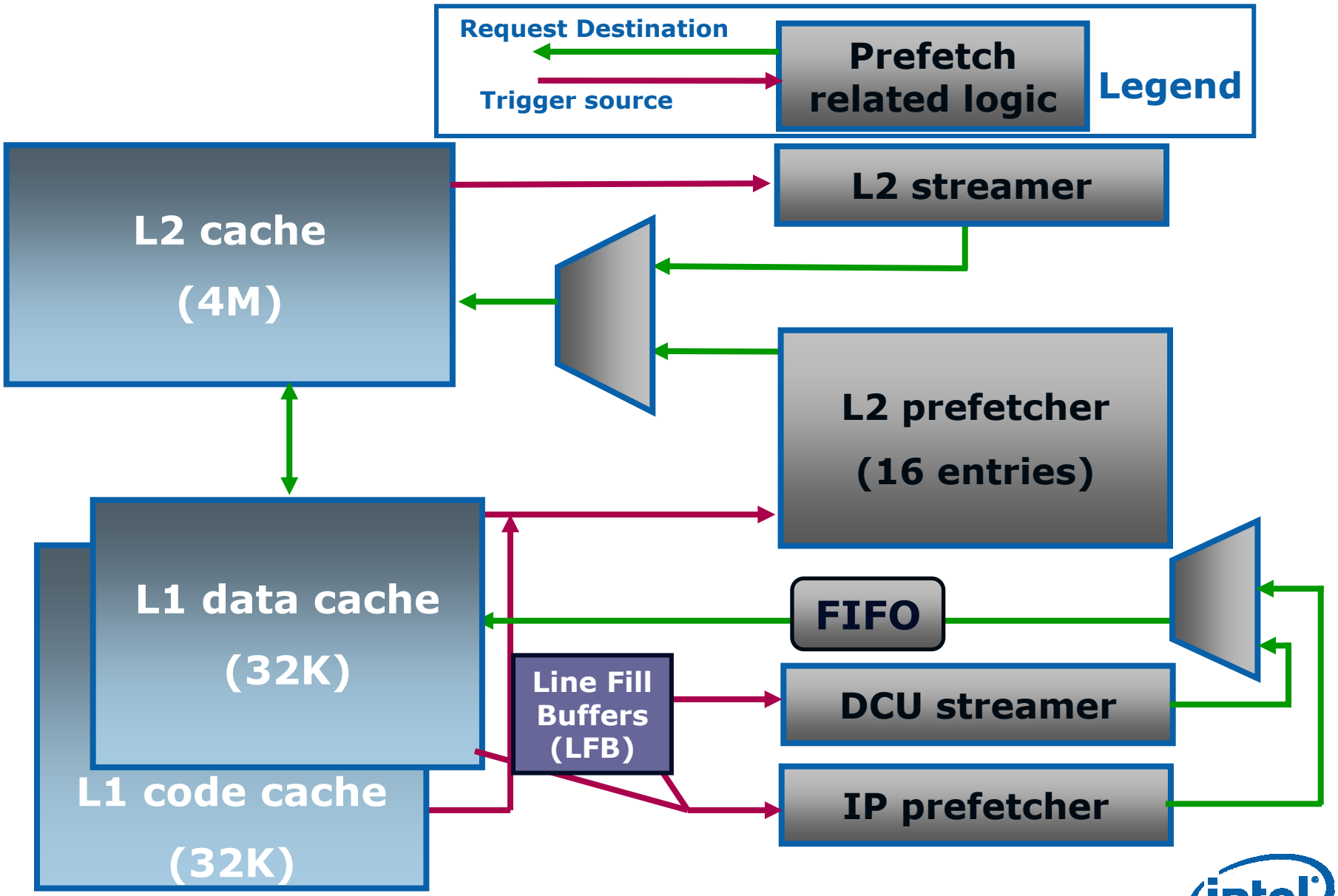
How is the prediction done?

- Using an history array indexed by Instruction Pointer
- An entry in the history array consists of a saturating counter
- When a particular load “failed” or “would have failed” disambiguation: reset its counter
- Each time a particular load could have been correctly disambiguated: increment counter
- If counter saturates: disambiguation possible on this load (starting from next iteration)

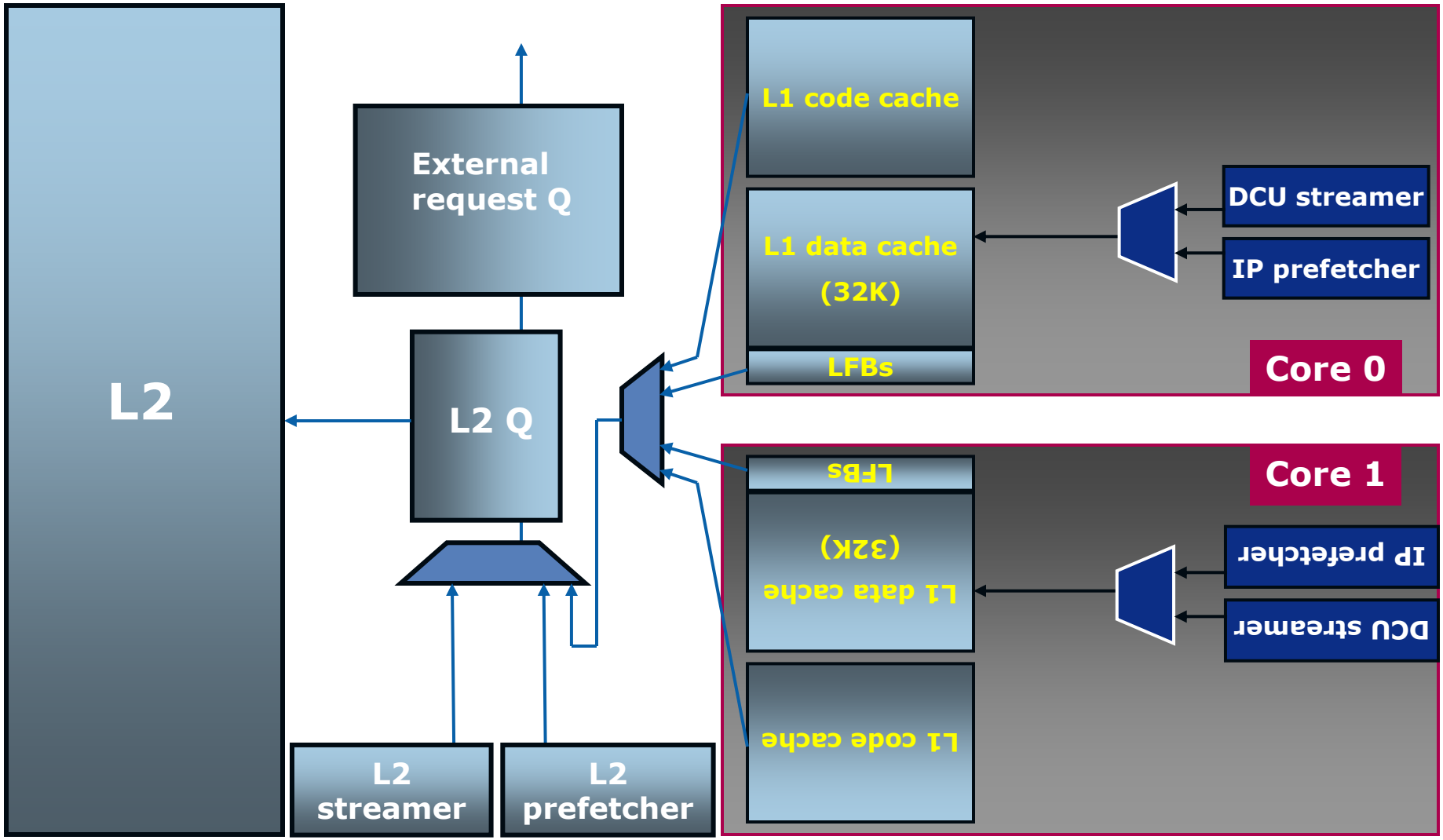
How is the prediction verified against the actual outcome?

- History update done at load's retirement based on control bits in the Load Buffer
- When a store is executed, scan all younger loads in the Load Buffer and mark conflicting cases:
  - Predicted colliding / actually colliding => reset
  - Predicted not colliding / actually colliding => reset, restart
- Disambiguation is disabled/suspended in some cases, either to enforce ordering, for implementation reasons, or to prevent performance loss

High level view of prefetchers

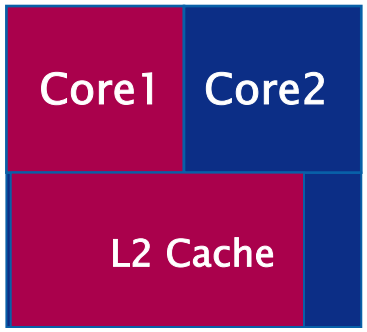


Map of Prefetchers and Multi-core

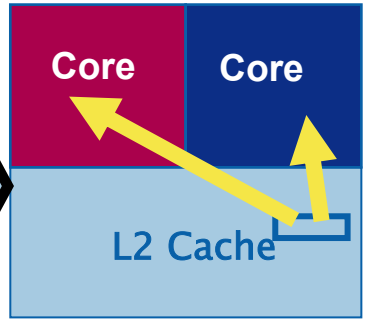


Intel® Advanced Smart Cache

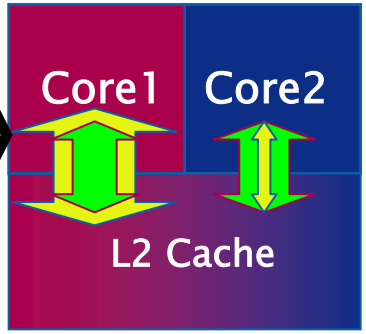
Dynamic Cache Allocation:
Shared cache enables each core to have access to full cache for faster data access



Large Shared Cache:
Only one copy of shared data is kept in the cache and can be accessed by both cores



Dynamic Bandwidth Allocation:
High bandwidth application can borrow L1 to L2 bandwidth from the other core's application



2X L2 to L1 Bandwidth
Sustained rate of 2 cycles per cache line

Summary

Intel® Core™ Microarchitecture is a new foundation for Intel® architecture-based mobile, desktop, and server processors

Incorporates advanced innovations which optimize performance over a range of market segments. Among them:

- **Memory disambiguation increases performance by eliminating false memory dependencies, improving latency associated with memory accesses**
- **Advanced prefetchers successfully place data in caches for "just-in-time" execution, hiding memory latencies**
- **Advanced Smart Cache provides flexible performance for both single and multi threaded applications**

A microarchitecture which delivers increased energy efficient performance

Links

Intel® Core™ Microarchitecture:

http://www.intel.com/technology/architecture/coremicro/

Intel® Energy-Efficient Performance:

http://www.intel.com/technology/eep/index.htm

Intel Product Benchmark Details:

http://www.intel.com/performance

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