SH-MobileG1: A Single-Chip Application and Dual-mode Baseband Processor

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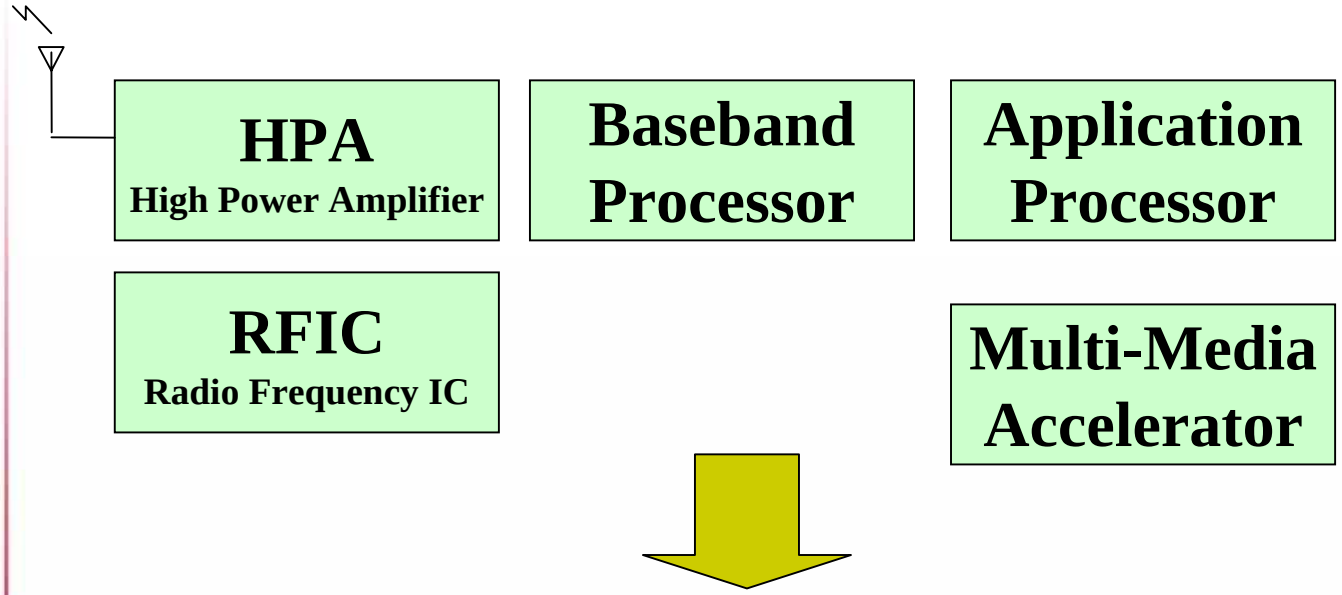
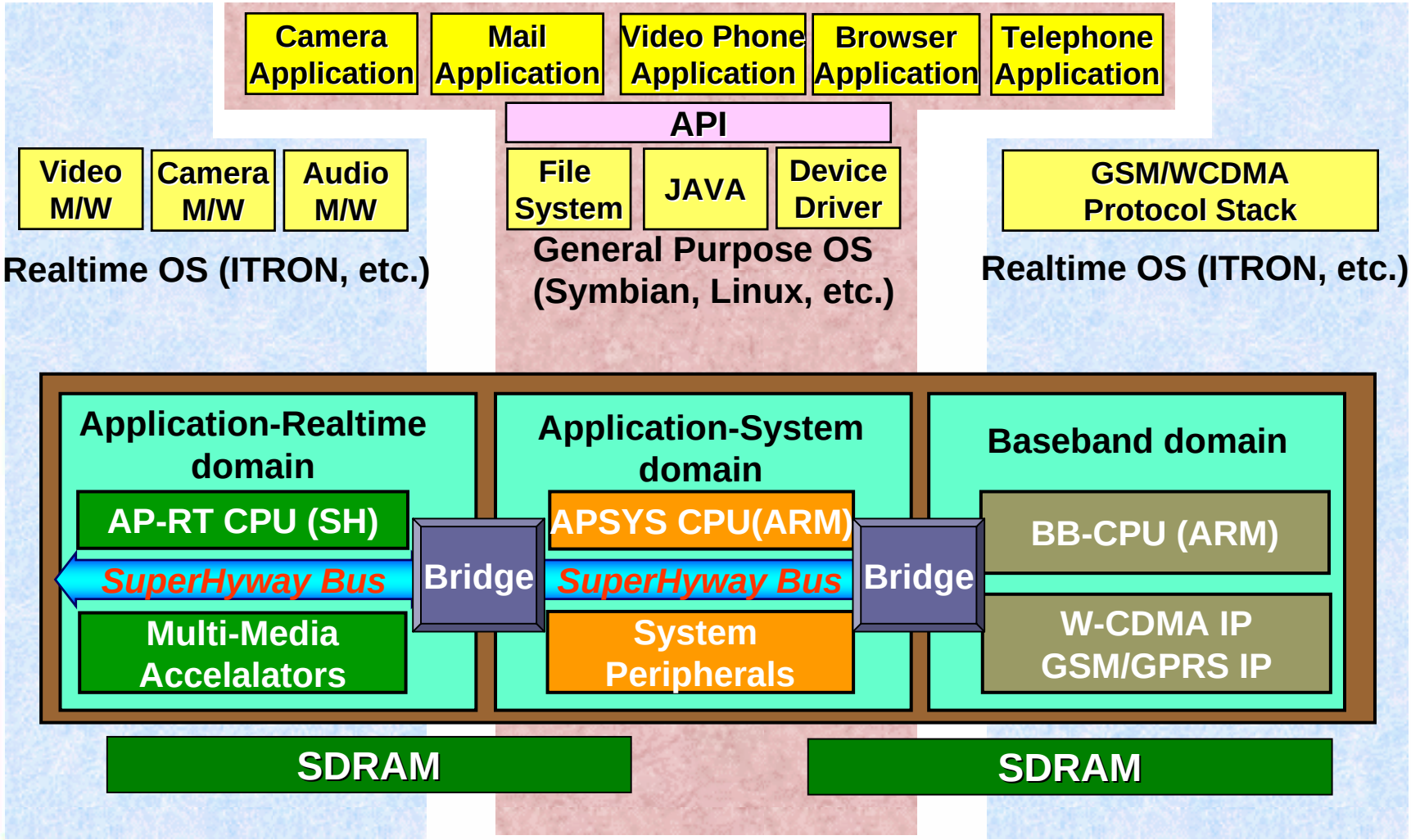
Outline

- Overview
- SH-MobileG1 Architecture
  - 3 CPU Configuration
  - Communication Architecture
  - Interrupt Control
  - System Control
  - Power Control and Leakage Current
- Summary

3G Multi-Media Cellular Phone System



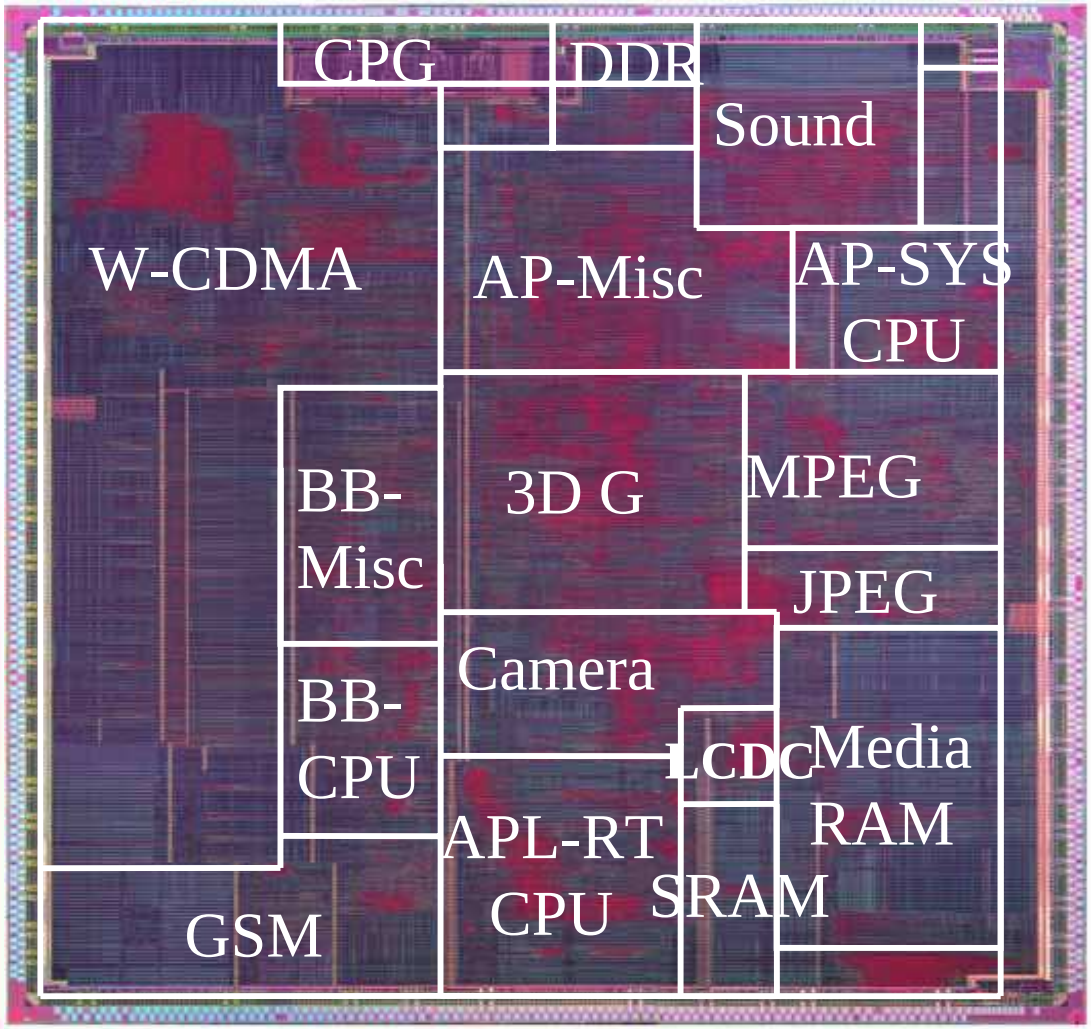
A Sample of System Architecture using G1



Motivation for One Chip Integration

- Chip-set cost will be down
- Mount area will be decreased by sharing common peripherals
- Performance will be up by wide data throughput
- Dynamic power will be saved by low-load inter-domain signals
- Static power will be saved by leakage current shut-off for unused domain

Chip Overview



Die size	11.15mm x 11.15mm
Process	90nm LP 8M(7Cu+1Al) CMOS dual-Vth
Supply voltage	1.2V(internal), 1.8/2.5/3.3V(I/O)
# of TRs, gate, memory	181M TRs, 13.5M Gate 20.2 Mbit mem

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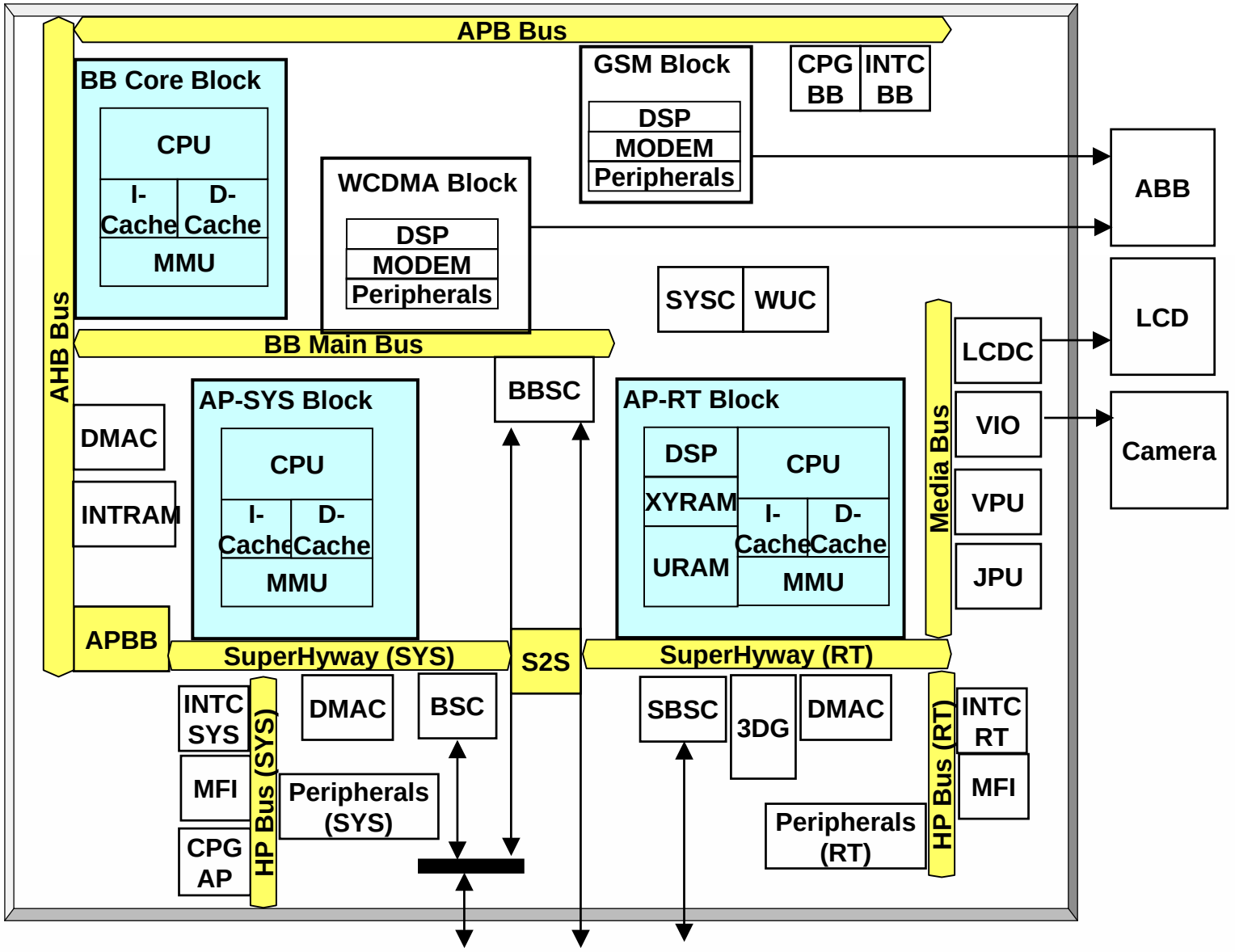
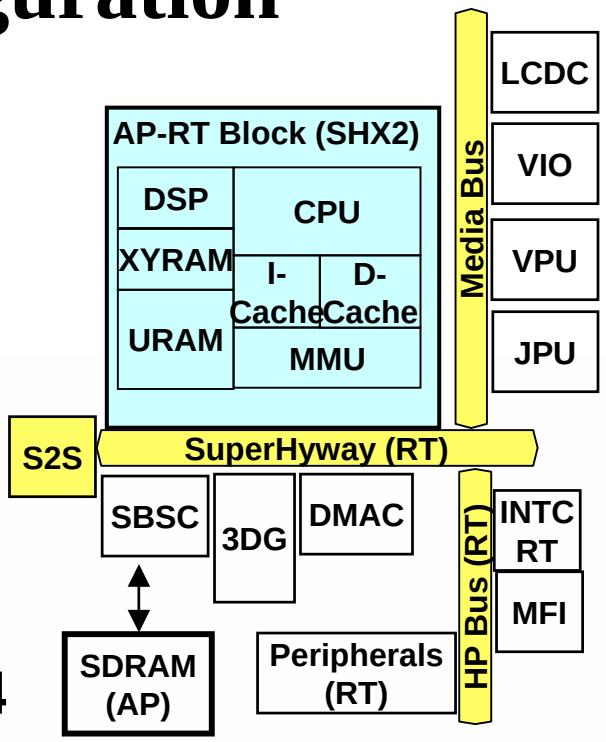
G1 Module Diagram



AP-Realtime Domain Configuration

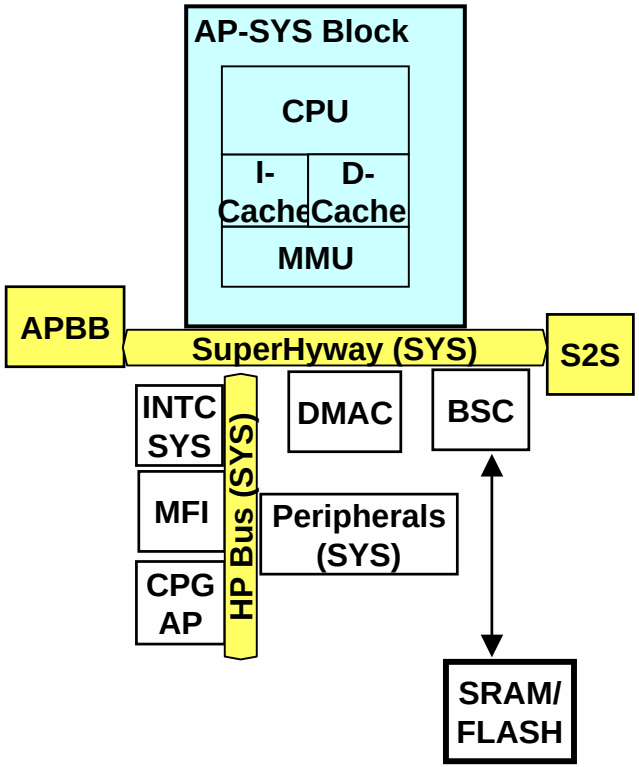
- **SHX2 runs on RT-OS**
  - 2-way superscalar up to 312MHz
  - 32KB-I$ and 32KB-D$
  - 512KB onchipRAM
- **Media IPs**
  - VPU encodes MPEG4 and H.264
  - VIO handles up to 5M pixel camera.
  - 3D graphic accelerator



S2S: SHwy-SHwy bridge
SBSC: SDR/DDR-SDRAM Controller
LCDC: LCD Controller
VIO: Camera I/F with Image-Processing Engine
VPU: Video Processing Unit (MPEG-4 Accelerator)
JPU: JPEG Codec Unit
3DG: 3D Graphics Accelerator
INTC: Interrupt Controller
MFI: Multi-Functional Interface

AP-System Domain Configuration

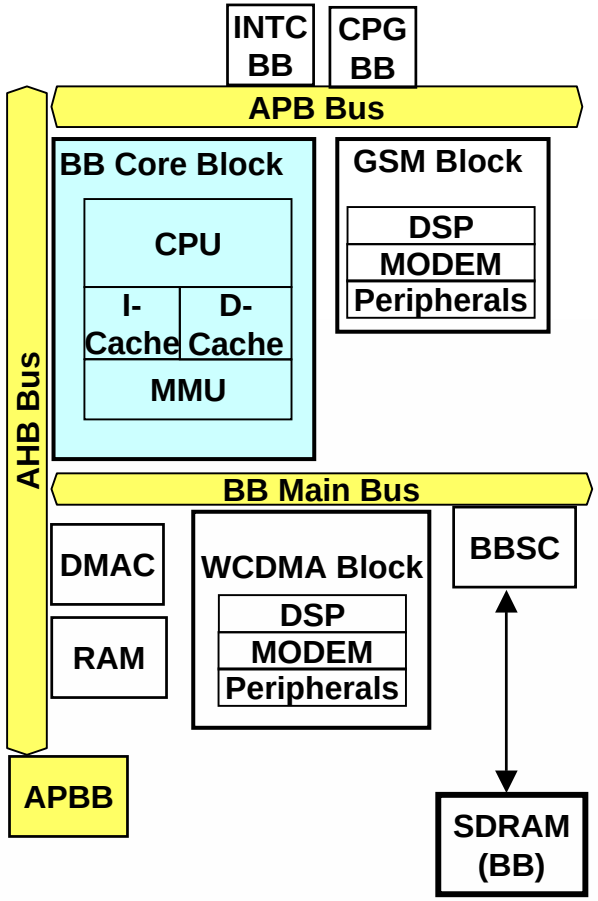
- **ARM926EJ-S runs on general-purpose OS**
  - **Up to 208MHz**
  - **32KB-I$ and 16KB-D$**
- **Peripherals**
  - **Sound handling**
  - **SDcard, IIC**
  - **Flash Control**
  - **USB**
  - **BB communication serial**



S2S: SHwy-SHwy bridge
APBB: AP-BB bridge
BSC:: SRAM/FLASH Controller
CPG: Clock Pulse Generator
INTC: Interrupt Controller
MFI: Multi-Functional Interface

Baseband Domain Configuration

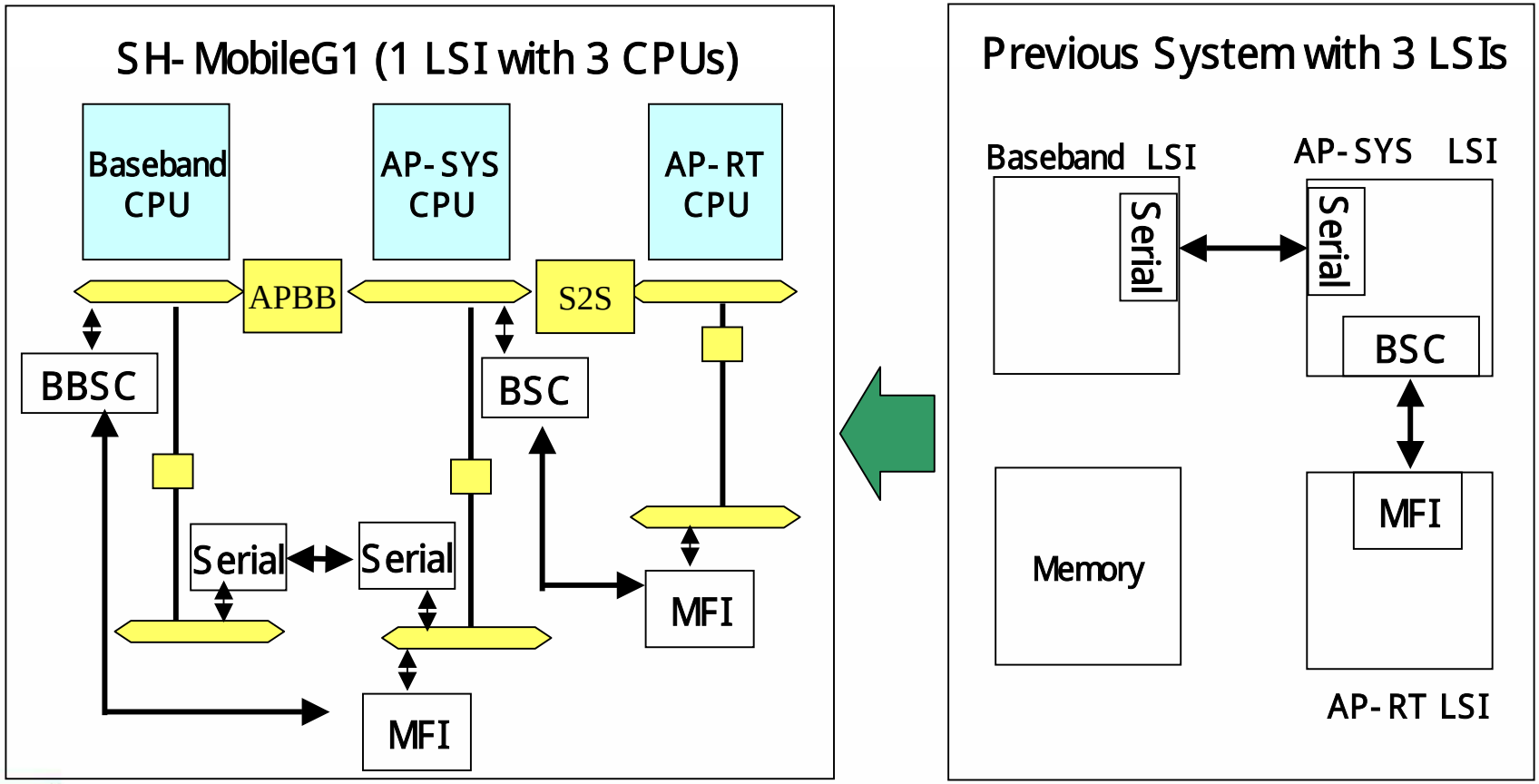
- **ARM926EJ-S runs on RT-OS**
  - **Up to 104MHz**
  - **16KB-I$ and 4KB-D$ with TCM**
- **W-CDMA and GSM/GPRS**
  - **DSP accelerates the modem protocol handling**
  - **One can be cut-off where only the other is available**
  - **Only small logic is awake for tracing the timing of each radio**



APBB: AP-BB bridge
BBSC: Baseband Bus Controller
CPG: Clock Pulse Generator
INTC: Interrupt Controller

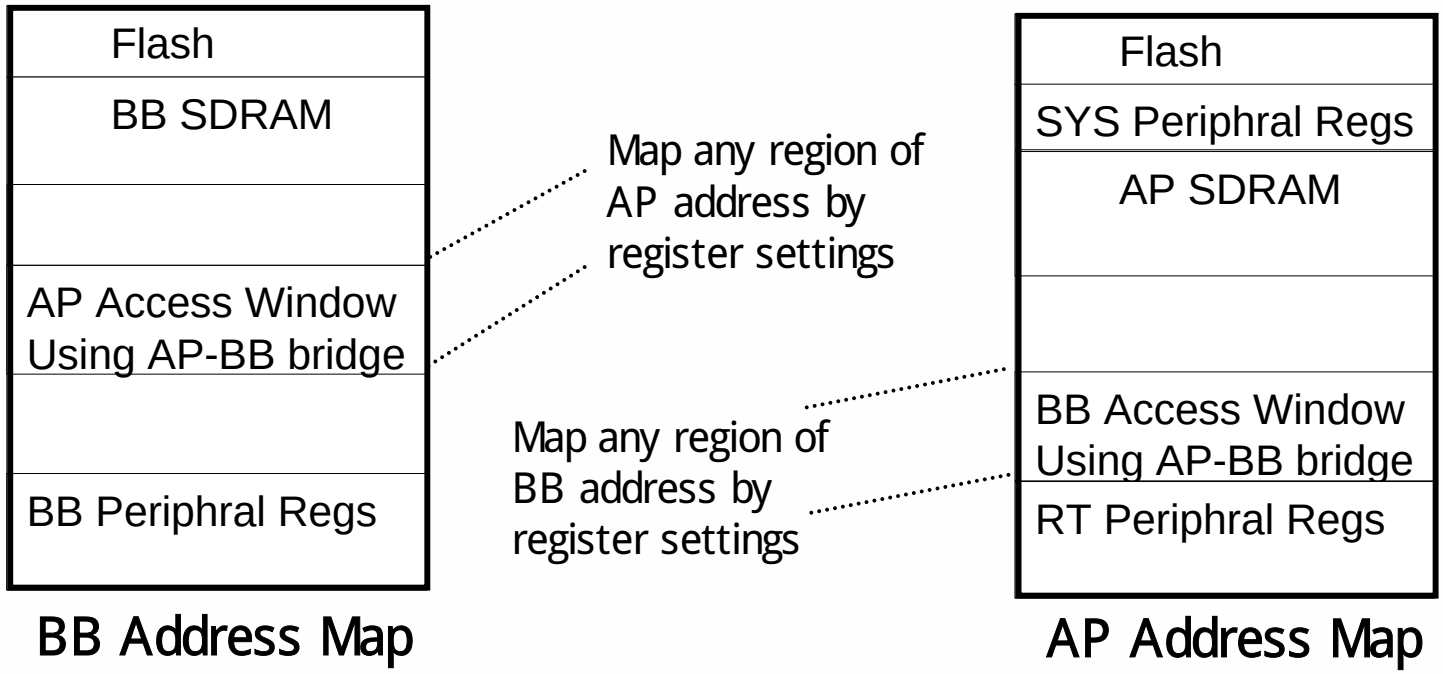
Communication Architecture

- G1 keeps the communication paths (MFI and Serials) used in the previous system for software reuse



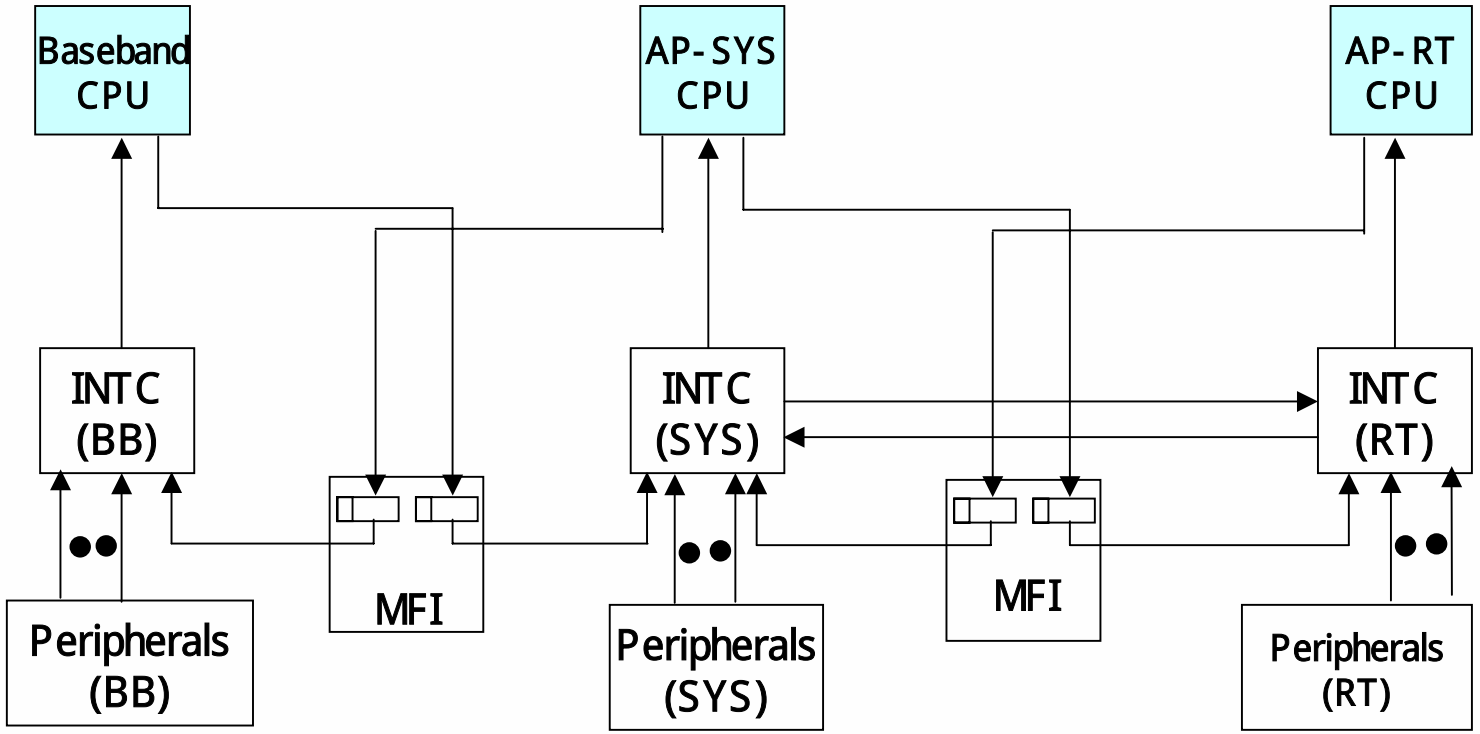
Communication Architecture (Cont'd)

- **AP-SYS and AP-RT share SDRAM and memory map**
- **AP and BB have different SDRAM and memory map**
- **APBB bridge supports access window scheme to access the resource in the other memory map**

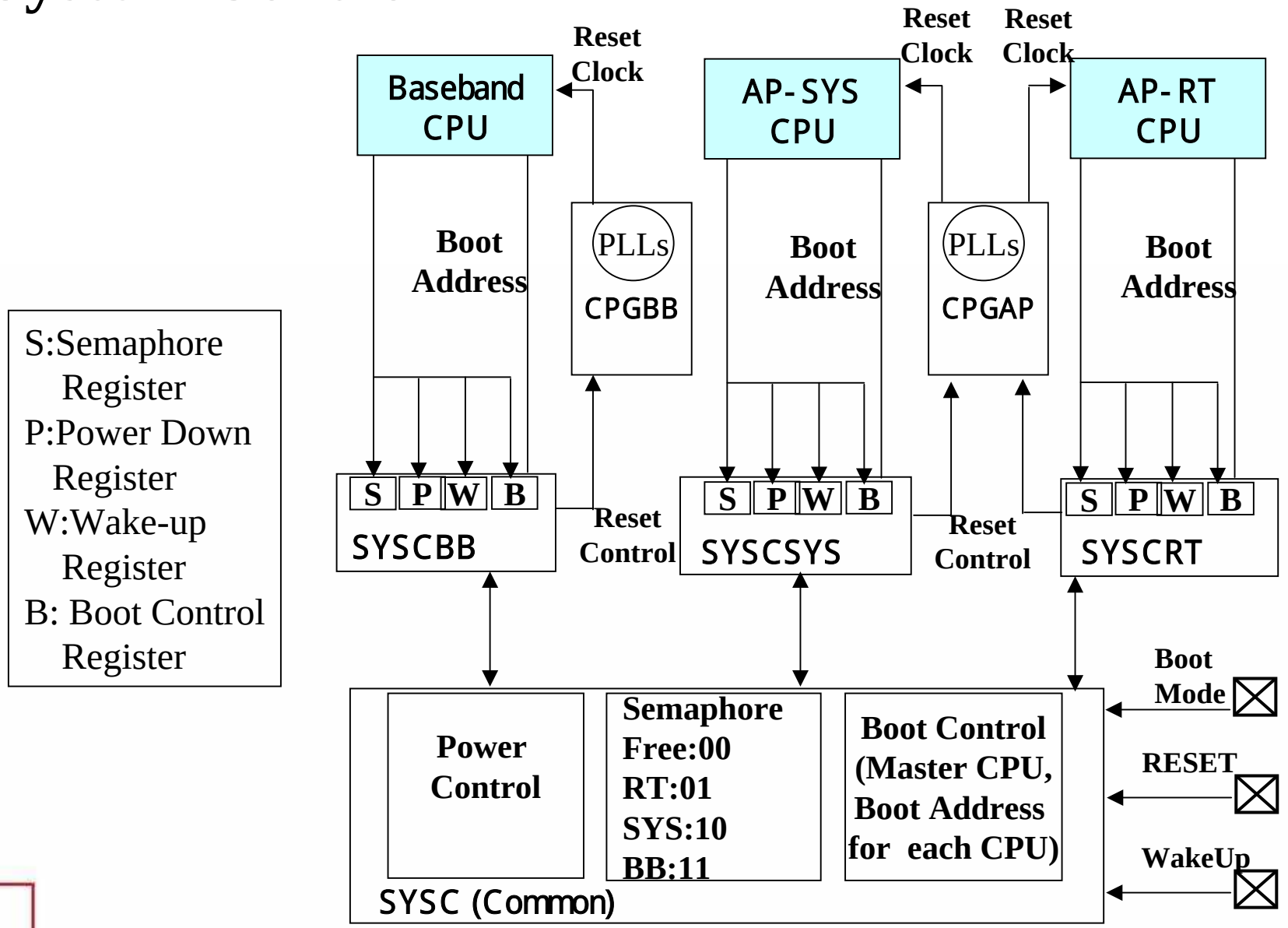


Interrupt Control

- Each CPU has its INT controller
- MFI can generate inter-domain interruptions
- Some external pins generate interrupts for each CPU



System Control



System Control (Cont'd)

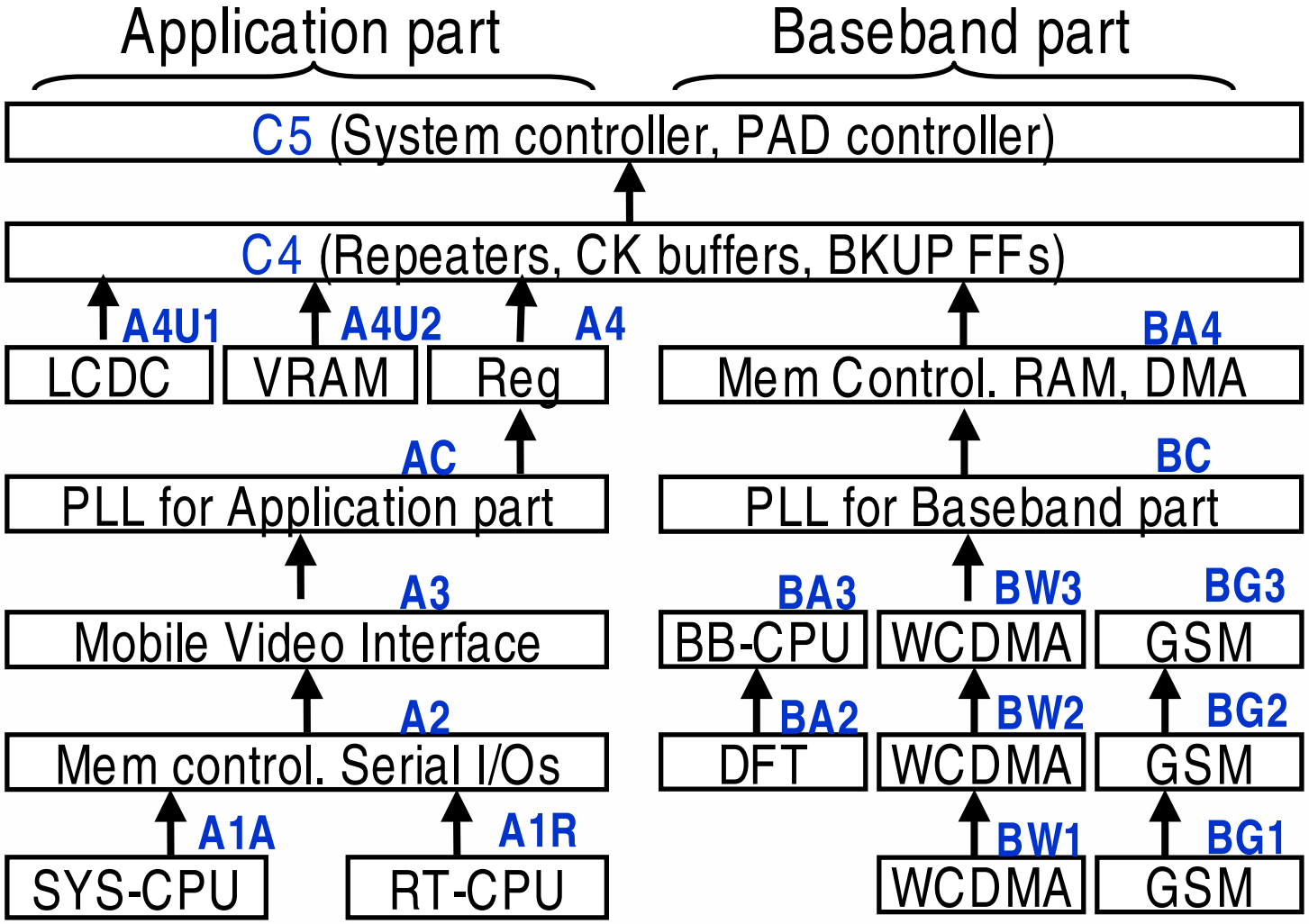
- **Boot Control**
  - **One master CPU defined by pin settings boots first and specifies the other CPUs' boot addresses**
  - **Various boot modes are supported for system configurability and debuggability**
    - **(1) BB Master External Memory Boot**
    - **(2) BB Master Internal ROM Boot**
    - **(3) BB-Alone Mode (for Test)**
    - **(4) AP-SYS Master External Memory Boot**
    - **(5) AP-SYS Master Internal ROM Boot**
    - **(6) AP-RT Master Boot**
    - **(7) AP-Alone Mode (for Test)**

System Control (Cont'd)

- **Power Control**
  - **Each CPU can read and write SYSC registers from each domain, which are reflected into the common SYSC**
  - **Power up/down can be controlled by each CPU that gets the semaphore**
- **Clock Control**
  - **AP and BB have separate Clock Pulse Generator**
  - **Many variations of clock configuration and gear changes are supported for dynamic power reduction**
  - **Clock for some IPs remains the fixed frequency**

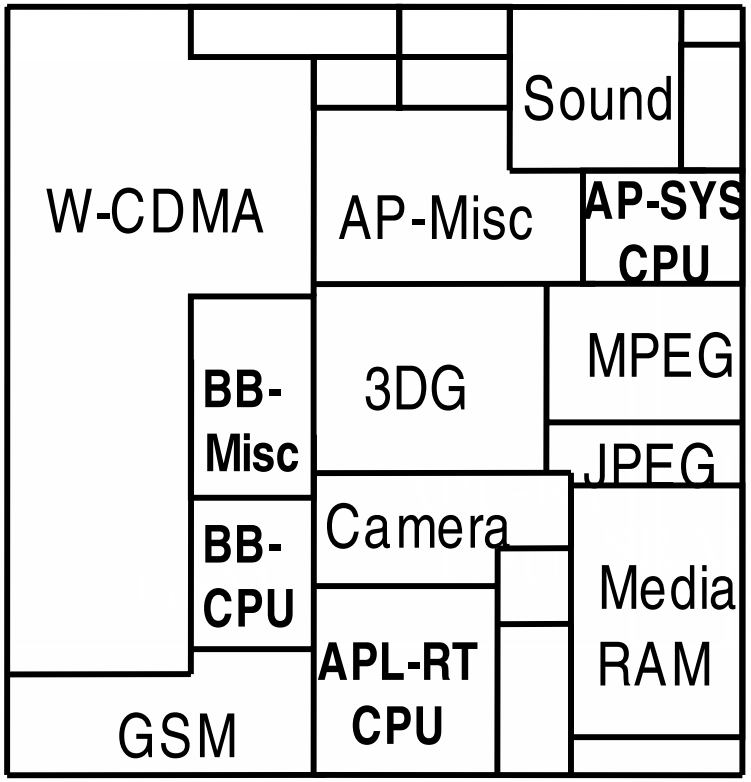
Power Domain

- **20 hierarchical domains for partial power-off**

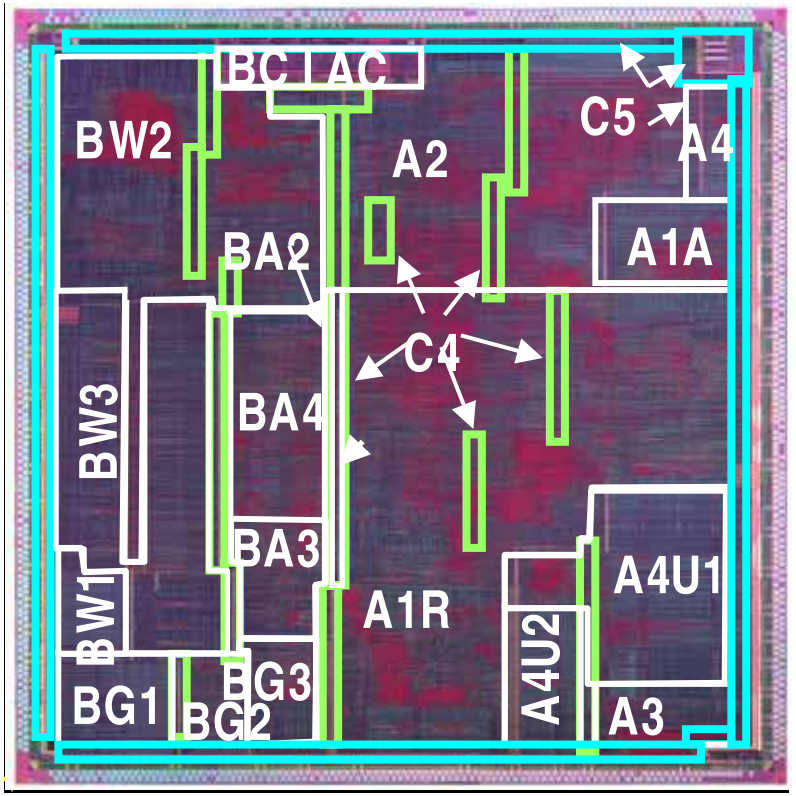


Power Domain (Cont'd)

Chip Floorplan



Power Domains

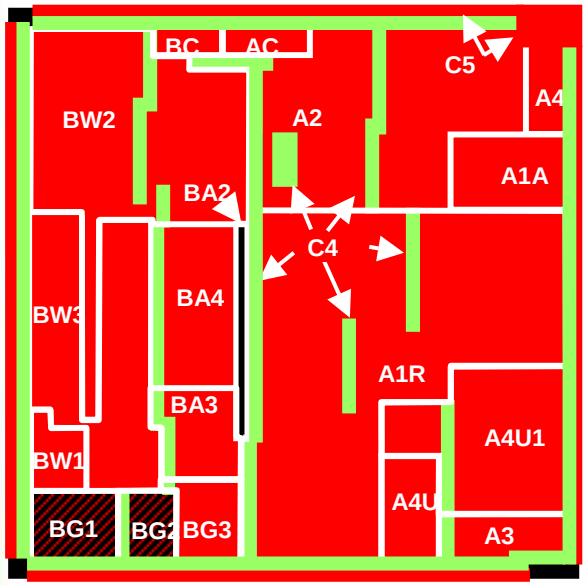


Implementation Results of Power Domains

# of Power domains	20 domains
# of Islands for C4 (Repeaters,CK buffers, BKUP FFs)	19 islands
# of Repeaters in C4 domain	3100 cells
# of Clock buffers in C4 domain	1600 cells
# of Backup FFs in C4 domain	2300 cells
# of mIOs (isolation cell)	20000 cells
Total area of power switch	4.2 mm^2

Leakage Current in Usage Scenes

(1) Video telephony



Power on

Power off

Baseband part	Control	ON
	W-CDMA	ON
	GSM	ON / OFF
Application part	System-domain	ON
	Realtime-domain	ON
Measured Leakage Current (@ Room Temp, 1.2V)		849 μA

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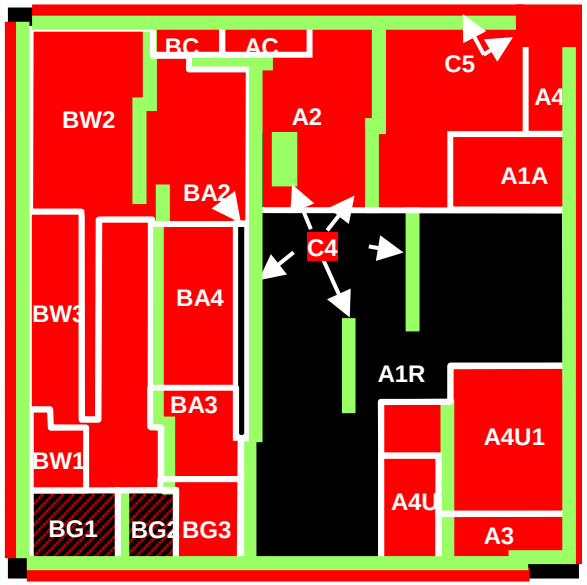
Leakage Current in Usage Scenes

(2)Telephony (W-CDMA)



Power on

Power off

Baseband part	Control	ON
	W-CDMA	ON
	GSM	ON / OFF
Application part	System-domain	ON
	Realtime-domain	OFF
Measured Leakage Current (@ Room Temp, 1.2V)		407 μA

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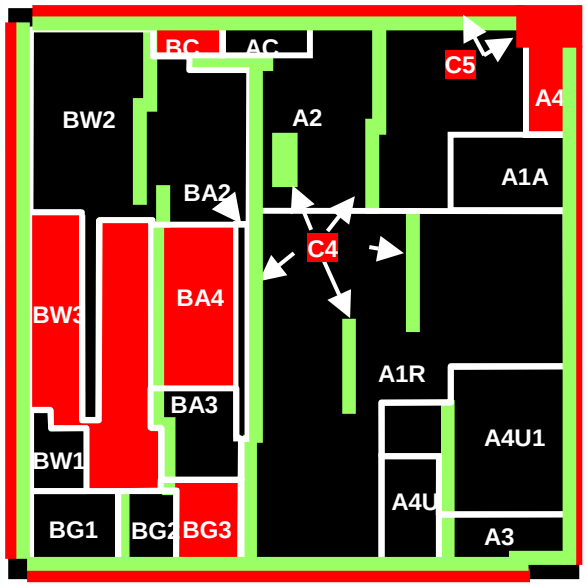
Leakage Current in Usage Scenes

(3)Waiting for Calling



Power on

Power off

Baseband part	Control	ON
	W-CDMA	OFF *
	GSM	OFF
Application part	System-domain	OFF
	Realtime-domain	OFF
Measured Leakage Current (@ Room Temp, 1.2V)		299 μA

*: Intermittent Operation

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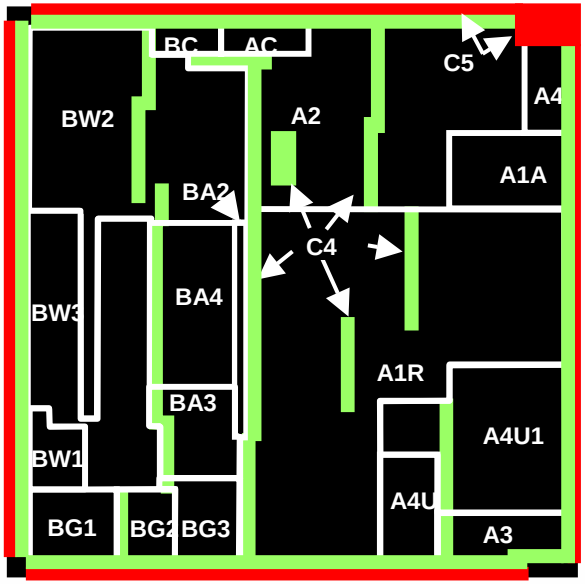
Leakage Current in Usage Scenes

(4) Power off (I/O fixed)



Power on

Power off

Baseband part	Control	OFF
	W-CDMA	OFF
	GSM	OFF
Application part	System-domain	OFF
	Realtime-domain	OFF
Measured Leakage Current (@ Room Temp, 1.2V)		7 μA

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Summary

- **We have developed SH-MobileG1**
  - **Application and dual-baseband single-chip processor for 3G multimedia cellular phone system**
  - **Key features of its architecture have been presented**
  - **One chip integration contributes not only to dynamic but also to leakage current reduction by careful partial power-off control**